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A Review on IEEE-754 Standard Floating Point Multiplier using Vedic Mathematics

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Abstract: ***The fundamental and the core of all the Digital Signal Processors (DSPs) are its multipliers and the speed of the DSPs is mainly determined by the speed of its multiplier. IEEE floating point format is a standard format used in all processing elements since Binary floating point numbers multiplication is one of the basic functions used in digital signal processing (DSP) application. In this work VHDL implementation of Floating Point Multiplier using Vedic mathematics is carried out. The Urdhva Tiryakbhyam sutra (method) was selected for implementation since it is applicable to all cases of multiplication. Multiplication of two no's using Urdhva Tiryakbhyam sutra is performed by vertically and crosswise. The feature is any multi-bit multiplication can be reduced down to single bit multiplication and addition using this method. On account of these formulas, the carry propagation from LSB to MSB is reduces due to one step generation of partial product.***
Keywords: Vedic Mathematics, Urdhva-triyakbhyam sutra, Floating Point multiplier.

I. INTRODUCTION

Multipliers are key components of many high performance systems such as microprocessors, FIR filters, digital signal processors, etc. Performance of a system is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system. Since multiplication dominates the execution time of most DSP application so there is need of high speed multiplier. Furthermore, it is generally the most area consuming. Hence, optimizing the area and speed of the multiplier is a major design issue. However, speed and area are usually conflicting constraints so that improving speed results mostly in larger areas. As a result, a whole spectrum of multipliers with different area-speed constraints has been designed with fully serial multipliers at one end of the spectrum and fully parallel Multipliers at the other end. These multipliers have moderate performance in both speed and area. Binary floating point numbers multiplication is one of the basic functions used in digital signal processing (DSP) application. The IEEE 754 standard provides the format for representation of Binary Floating point numbers in computers. The Binary Floating point numbers are represented in Single and Double formats. The Single precision format consists of 32 bits and the Double precision format consists of 64 bits.

The formats are composed of 3 fields; Sign, Exponent and Mantissa. A typical central processing unit devotes a considerable amount of processing time in implementing arithmetic operations, particularly multiplication operation. Most high performance DSP systems rely on hardware multiplication to achieve high data throughput. Multiplication is an important fundamental arithmetic operation. Performance constraints can also be addressed by applying alternative technologies. A change at the level of design implementation by the insertion of a new technology can often make viable an existing marginal algorithm or architecture.

This project deals with the "Design of high speed floating point multiplier using ancient technique". In this project Vedic Multiplication Technique is used to implement IEEE 754 Floating point multiplier. For calculation of mantissa unit The Vedic sutra is used. A change at the implementation level of design by the insertion of a new technology can often make viable an existing marginal algorithm or architecture. Performance constraints can also be addressed by applying alternative technologies.

II. LITERATURE REVIEW

According to Aniruddha Kanhe [1] Vedic Multiplication Technique is used to implement IEEE 754 Floating point multiplier. The Urdhva-triyakbhyam sutra is used for the multiplication of Mantissa bit. The inputs to the multiplier are provided in IEEE standard 754, 32 bit format. The floating point multiplier is implemented in VHDL and Virtex-5 FPGA is used. Multiplication of two floating point numbers represented in IEEE 754 format is done by multiplying the normalized 24 bit mantissa, adding the 8 bit exponent and resultant is converted in excess 127 bit format, for the sign calculation the input sign bits are XORed. In this paper, propose algorithm is the Vedic Multiplication algorithm for multiplication of 24 bit. The performance of Mantissa calculation Unit dominates overall performance of the Floating Point Multiplier. The Exponent Calculation Unit is implemented in this paper using 8 BIT Ripple Carry Adder consume more delay.

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According to Honey Durga Tiwari [2] a Vedic multiplier and square architecture is proposed based on algorithm of ancient Indian Vedic Mathematics, for high speed and low power applications. This Paper shows how the computational complexity is reduced in the case of Vedic multipliers as compared to the conventional multipliers. The Vedic multiplication formulae, Urdhva tiryakbhyam and Nikhilam, have been investigated in detail. Due to its structure, it suffers from a high carry propagation delay in case of multiplication of large numbers. This problem has been solved by introducing Nikhilam Sutra which reduces the multiplication of two large numbers to the multiplication of two small numbers. The FPGA implementation result shows that the delay and the area required in proposed design is far less than the conventional booth and array multiplier designs making them efficient for the use in various DSP applications.

Jain, Jenil, and Rahul Agrawal et al. [3] this paper presents design of high speed floating point unit using reversible logic. In recent nanotechnology, Programmable reversible logic design is trending as a prospective logic design style for implementation and quantum computing with low impact on circuit heat generation. There are various reversible implementations of logical and arithmetic units have been proposed in the existing research, but very few reversible floating-point designs has been designed. Floating-point operations are used very frequently in nearly all computing disciplines. The analysis of proposed reversible circuit can be done in terms of quantum cost, garbage outputs, constant inputs, power consumption, speed and area.

Gopal, Lenin, Mohd Mahayadin et al. [4] in the paper, eight arithmetic and four logical operations has been presented. In the proposed design 1, Peres Full Adder Gate (PFAG) is used in reversible ALU design and HNG gate is used as an adder logic circuit in the proposed ALU design 2. Both proposed designs are analyzed and compared in terms of number of gates count, garbage output, quantum cost and propagation delay. The simulation results show that the proposed reversible ALU design 2 outperforms the proposed reversible ALU design 1 and conventional ALU design.

Nachtigal, Michael, Himanshu Thapliyal et al. [5] In this work, a new reversible design of single precision floating point multiplier has been proposed based on operand decomposition approach. Furthermore, a new reversible design of the 8x8 bit Wallace tree multiplier has proposed that is optimized in terms of quantum cost, delay, and number of garbage outputs. Wallace tree multiplication consists of three conceptual stages: Partial product generation, partial product compression using 4:2 compressors, full adders, and half adders, and then the final addition stage to generate the product. In this work we perform optimization at each of these three stages.

Dhanabal, R., Sarat Kumar Sahoo et al. [6] presents a design using reversible gates. Reversible gates namely TSG gate performs 1-bit addition with carry. This is the first reversible gate which alone can acts as full adder. Gate is used to perform logical operations like AND, OR. In this works, designing 1-bit alum has also been presented using pass transistor with virtuoso tool of cadence. Based on analysis of the result, this design using reversible gates is better than that using the irreversible gates.

III. PROPOSED METHOD

A. Floating Point Multiplication Algorithm

The multiplier for the floating point numbers represented in IEEE 754 format can be divided in four different units: Exponent Calculation Unit Mantissa Calculation Unit, Sign Calculation Unit, Control Unit.

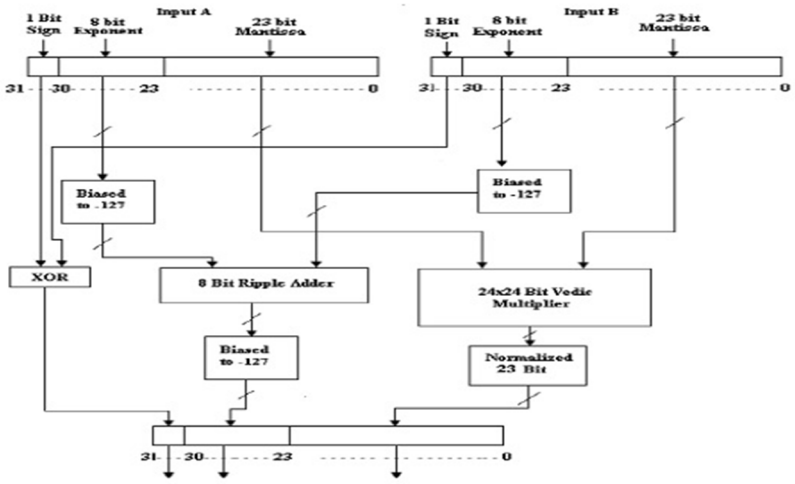

Fig. 1: Architecture for Floating point multiplier.

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1) Multiplying the significand; i.e. (1.M1*1.M2)
2) Placing the decimal point in the result
3) Adding the exponents; i.e. (E1 + E2 – Bias)
4) Obtaining the sign; i.e. s1 xor s2
5) Normalizing the result; i.e. obtaining 1 at the MSB of the results' significand
6) Rounding the result to fit in the available bits.
7) Checking for underflow/overflow occurrence.

B. *Multiplier design*

1) *Vedic Mathematics:* The word 'Vedic' is derived from the word 'Veda' which means the store-house of all knowledge. We must be thankful to Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja to introduce Vedic Mathematics and acknowledge the work of various people regarding Vedic Mathematics . Vedic mathematics is mainly based on 16 Sutras .Vedic Sutras the word 'Vedic' is derived from the word 'Veda' which means the store-house of all knowledge. Vedic mathematics technique is mainly based on 16 aphorisms dealing with various branches of mathematics like algebra, arithmetic, geometry etc. These Sutras along with their brief meanings are enlisted below alphabetically.

a) (Anurupye) Shunyamanyat - If one is in ratio. The other is zero
b) Chalana-Kalanabyham- Similarities and Differences.
c) Ekadhikina Purvena - By one more than the previous one.
d) Ekanyunena Purvena - By one less than the previous one.
e) Gunakasamuchyah - The factors of the sum is equal to the sum of the factors.
f) Gunitasamuchyah - The product of the sum is equal to the sum of the product.
g) Nikhilam Navatashcaramam Dashatah - All from 9 and the last from 10.
h) Paraavartya Yojayet - Transpose and adjust.
i) Puranapuranabyham - By the completion or no completion.
j) Sankalana-vyavakalanabhyam - By addition and by subtraction.
k) Shesanyankena Charamena - The remainders by the last digit.
l) Shunyam Saamyasamuccaye - When the sum is the same that sum is zero.
m) Sopaantyadvayamantyam - The ultimate and twice the penultimate.
n) Urdhva-tiryakbyham - Vertically and crosswise.

2) *Urdhva-Tiryakbyham Sutra:* The multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a multiplication formula which is applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The generation of partial products and their summation is obtained using Urdhava Triyakbhyam explained in fig 2 Since the pat1ial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Thus the multiplier is independent of the clock frequency because it will require the same amount of time to calculate the product. The main advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a increased in processing power is due to higher clock frequency. generally results in its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. By adopting the Vedic multiplier, microprocessors designers can easily handle these problems to avoid catastrophic device.

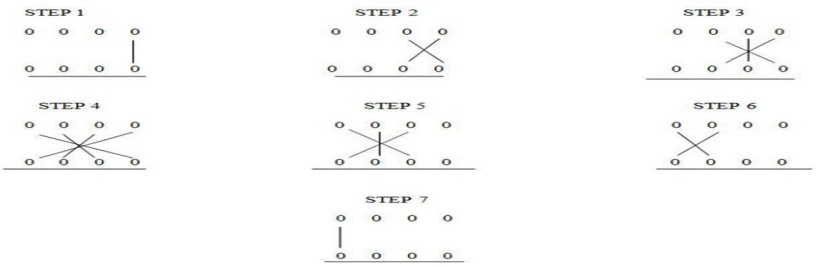

Fig.2 Line diagram of the multiplication.

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The performance of Mantissa calculation Unit dominates overall performance of the Floating Point Multiplier. This unit use unsigned multiplier for multiplication of 24x24 BITs. The ancient Multiplication technique is chosen for the implementation of this unit. The Vedic multiplication system is based on 16 Vedic sutras which describes simple natural ways of solving a whole range of mathematical problems. The Urdhva- triyakbhyam sutra is suitable for this purpose out of these 16 Vedic Sutras. In this method the partial products are generated simultaneously which itself reduces delay and makes this method fast. Consider the numbers A and B where A = p2p1p0 and B = q2q1q0. The LSB of A is multiplied with the LSB of B:

s0=p0q0;

Then p0 is multiplied with q1, and q0 is multiplied with p1 and the result are added together as: c1s1=p1q0+p0q1;

Here c1 is carry and s1 is sum. Next step is to add c1 with the multiplication results of p0 with q2, p1 with q1 and p2 with q0.

c2s2=c1+p2q0+p1q1 + p0q2;

Next step is to add c3 with the multiplication results of p1 with q2 and p2 with q1. c3s3=c2+p1q2+p2q1;

Similarly the last step c4s4=c3+p2q2;

Now the final result of multiplication of A and B is c4s4s3s2s1s0.

IV. CONCLUSION

The paper shows the efficient use of Vedic multiplication method in order to multiply two floating point numbers .This paper presents an implementation of a floating point multiplier that supports the IEEE 754- 2008 binary interchange format. Based on the discussion made above it is very clear that a multiplier is a very important element in any processor design and a processor spends considerable amount of time in performing multiplication and generally the most area consuming. Hence, optimizing the speed and area of the multiplier is a major design issue. An improvement in multiplication speed by using new techniques can greatly improve system performance.

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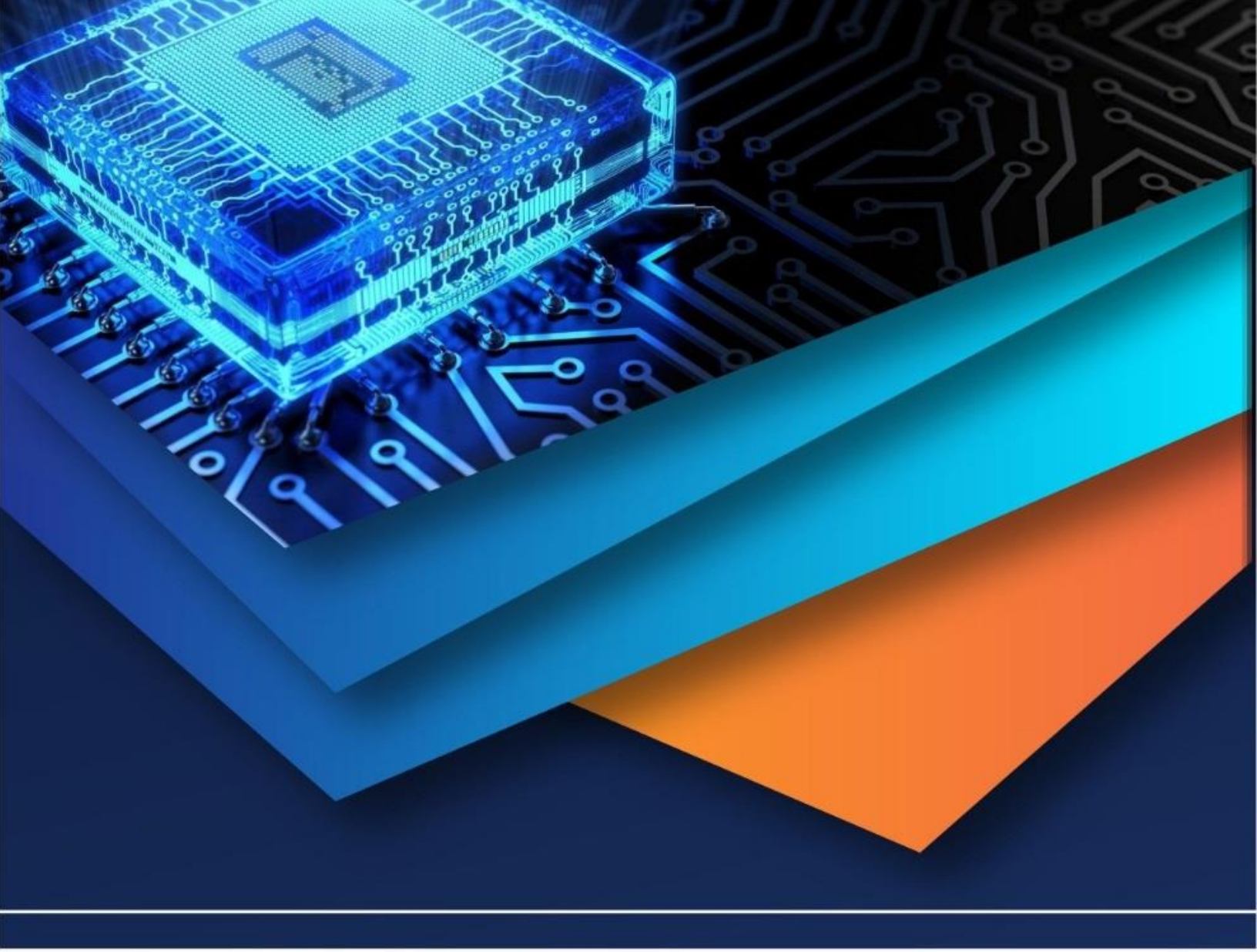

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