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Low Power and Fast Full Adder by Exploring New XOR and XNOR Gates

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Abstract: ***In this project, novel circuits for FULL ADDER are proposed using new XOR or XNOR gates. The conventional design of XOR or XNOR gates shows that the not gate in the schematic has drawbacks. So by investigating advanced XOR or XNOR gates we proposed the schematic design. The proposed schematics are optimized in terms of speed, delay, power and power delay product. We developed six novel hybrid full adder schematics based on exploring new XOR or XNOR gates. Each designed schematics have their specifications of energy consumption, delay, power delay product. To simulate the performance of the proposed designs, we use mentor graphics, tanner tool. The simulation yields a 45-nm CMOS innovation model that focuses on the proposed plans having best speed and power other than the plan of any full adder. The proposed Full Adders has 2-28% increment in consumption of energy and power delay product compared to other design schematics. The proposed hybrid full adders are investigated with voltage 1.8V, speed ,size of transistors, area, power consumption and delay.***
Keywords: Full adder(FA), XOR-XNOR,Simulation

I. INTRODUCTION

In today's world, nowadays electronic systems assume a pivotal part in everyday life. Digital Gadgets, e.g., microprocessors, communication devices, and signal processors, are in the group of electronic frameworks. As the demand for electronic systems increases, the usage of circuits are restricted to consume low power and area consumption. Therefore, as their is growth in population and technology the interest for the versatile gadgets like cell phones, tablets, and PCs have increased a lot ,so the designers to meet the above requirement ,designs the circuit which consumes low energy consumption and area with the increase of speed. As the efficiency of many digital applications are to perform arithmetic operations, such as adder circuits ,multipliers circuits and dividers schematics. AS the technology is developed the chip density for the design of circuit is increased. So plenty of transistors are doped into the single chip.

Schematics of Full adder are made as full-swing and non full-swing types. The result of the full adder is driven by the Standard CMOS ,complementary pass-transistor logic (CPL) , transmission gate (TG) , transmission function, and hybrid pass logic with static CMOS. In a full swing family the FA are most important. Non full-swing type consists of 10T and 8T . In this undertaking, we mimic the XOR or XNOR (XOR/XNOR) and both XOR and XNOR (XOR–XNOR) gates and give advanced schematics to the two. Additionally, we attempt to determine the issues that are available at examined schematics. Afterward, with every one of these new XOR/XNOR and XOR–XNOR schematics, we develop new six FA architectures.

In this project we are designing the arithmetic circuits of redundant stored uni bit transfer representation and numeral system of residues**.** To process digital systems of higher speed we use the residue number system because which aids, parallel, modulus, error -tolerance, and carry bound sums. Using RNS system we develop the sum of parallel-digit along periodic delay,it does not depend on the length of variable in operations. The carry propagation is bounded to inside the modules,where as the other inter module limits the speed of arithmetic operation of carry propagation. Hence ,the carry free term of redundancy arithmetic is necessary. The carry free property is limiting to real time application.

In this project we are designing a full adder of less power and less voltage. During recent times we identified that the circuits designs of low power play a crucial role in critical technology ,which has a huge demand of portable consumer electronics products in recent years.So a lot of enhanced models came into picture while designing simple logical arithmetics with the help of pass transistor and transmission gates.Hence,to design a CMOS mini transistor pass network XOR-XNOR gate, wholly related for Vt reduction in metal oxide semiconductor transistors, we use a formal design procedure. The proposed new schematic can operate within the applied condition whenever the power supply voltage is reduced, and this is considered to be continued until it is given to the initial design step of sizing the MOS transistors.so to overcome this , by usage of our XOR-XNOR gate. A less transistor count FA is proposed.

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Streamlining the W/L proportion of semiconductors is a way to deal with declining the PDP of the design along with forestalling the issues came about because of decreasing the supply voltage. The productivity of numerous computerized applications applies to the presentation of the number-crunching circuits, like adders, multipliers, and dividers. Because of the key part of expansion in every one of the number juggling tasks, numerous endeavors have been made to investigate good addition structures, for example, carry circuits like select, skip, look ahead adders and condition additions. Full adder is considered the basic square of these circuits and is at the focal point of consideration.

Considering level of yield voltage, FA designs can be partitioned into full-swing and non full swing classes. Standard CMOS, complementary pass-semiconductor logics(CPL) , transmission gate(TG) , transmission functions, 14T (14 transistors) and hybrid pass logic with static CMOS output FA (HPSC) . Full Adders are pivotal in the full-swing category. Non full-swing family consists of ten transistors,9transistors and 8 transistors.

In this proposal, we assess the number of models of XOR or XNOR (XOR/XNOR) and simultaneous XOR and XNOR (XOR–XNOR) gates and give designs of these. Additionally, we attempt to eliminate the issues present in the examined designs. Thereafter, with the proposed XOR/XNOR and XOR–XNOR circuits, we develop six new full adder circuits.

II. LITERATURE SURVEY

In this project we are designing the arithmetic circuits of redundant stored uni bit transfer representation and residue number system. The buildup number framework is appropriate for executing rapid computerized handling gadgets since it upholds parallel, modular, fault - tolerant, and convey limited math. The RNS framework can perform digit-equal expansion with a little and steady delay, which is autonomous of the operand length. The convey proliferation is confined to inside the modules, whereas the other leftover intramodular convey engendering limits the speed of number juggling operation. Therefore, the convey free property of excess number-crunching can be utilized the carry free property is restricting to continuous application. In this task we will talk about proposed model of high-radix excess RNS dependent on the put away unibit move portrayal for modulo 2n+1 that improves the force postpone item execution of ordinary repetitive RNS. An assortment of repetitive portrayals have been introduced. One is twofold number system(BSD),which perform expansion with convey spread chain that are restricted to single digit position .A crossover SD portrayal which restricts the greatest length of convey engendering chain to any ideal value. In expansion ,deduction and duplication circuits are planned in proposed framework.

In this undertaking we are planning a low voltage low force CMOS full viper. As lately we recognized that the low force plan of VLSI circuits play a crucial part in basic innovation ,which has a tremendous interest of compact purchaser gadgets items in late years.so in such manner numerous imaginative plans came into picture for planning essential rational capacities utilizing pass semiconductor and transmission entryways have showed up as of late. These plans depended to without including formal plan procedures. Hence, a formal plan system for understanding a negligible semiconductor CMOS pass network XOR-XNOR cell, which is completely made up for edge voltage drop in MOS transistors, is introduced. The proposed new cell can dependably work inside the specific limits when the force supply voltage is scaled down, as long as this is viewed as proceeded with it is given to the measuring of the MOS semiconductors during the underlying plan step.so to defeat this A low semiconductor tally full viper cell utilizing the new XOR-XNOR cell is introduced.

In this venture we propose a low intricacy full adder configuration including higher figuring speed, lower working voltage, and lower energy consumption. In this plan interaction we utilize low force plans of the XOR AND entryways pass semiconductor and transmission doors. In traditional we utilize 16T where as in proposed model we utilize 10T.To over come the sub threshold current spillage we are planning proposed model. The proposed configuration has decreased limit misfortune issue, higher speed, low influence utilization and better commotion resistance over the 10T full snake with practically identical execution. When contrasted and customary and improved full viper the force utilization is diminished undeniably and region is reduced. Energy saving might be upto40% might be achieved. The plan in both speed and energy utilization turns out to be more critical as of the snake increments. we additionally clarify how restrictive XOR AND are utilized to understand an overall full viper circuit dependent on pass transistor. The execution of the full snake is assessed and reenactment results are gotten from leather treater apparatus.

In this undertaking we propose CMOS full adders for energy proficient math applications. Here we present two fast and low force full snake cells planned with an option inner rationale construction and pass semiconductor rationale styles that lead to have a diminished force postpone product. We did an examination against all customary full adders having revealed a low PDP, in terms of speed, power utilization and area. Here all full adders are planned with a 45nmCMOS technology, and we tried utilizing a testbench permitted to gauge taken from all full viper inputs, besides the current gave from the force supply.

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Which display a normal PDP of 80% just with 40% of relative area. Many papers have been distributed in regards to the advancement of low-power full-adders, attempting various choices for the rationale style , differential course voltage switch, complementary pass-semiconductor rationale, twofold pass-semiconductor rationale, swing reestablished CPL , and half and half styles, and the rationale structure used to fabricate the snake module. The inward rationale structure has been received as the standard design in the greater part of the upgrades produced for the 1-bit full-adder module.

For arithmetic circuits, we first provide area and power-delay performances of low-voltage full adder cells in several CMOS logic styles. Also shown is a revolutionary hybrid full adder circuit. The suggested complete adder's sum and carry generating circuits are constructed using hybrid logic types. The pass logic circuit that creates the intermediate XOR and XNOR outputs has been enhanced to solve the switching delay problem in order to function at ultra-low supply voltage. The transistor is scaled in a methodical and elegant manner for low power-delay product. At 0.18-m CMOS manufacturing technology, the circuits are tuned for energy efficienc. Not only does the suggested hybrid full adder have full swing logic and balanced outputs, but it also has good output drivability. The area efficient arrangement compensates for the increase in transistor count of its corresponding CMOS output stage. Although its power-delay performance is equivalent to CMOS and worse to CPL, its area-efficient architecture makes it an excellent candidate for designing large tree structured arithmetic circuits when overall performance and area efficiency are important cost function factors.

III. TEST AND EVALUATION

The two input signal A,B are given to transistors. the signal B is given to P2 and signal A is given to P3.The signal B is given to N2 and P4 and the signal a is given to N2 and N3.The N3 is connected to P4.The signal B is given to N4 and P6 and the signal A is given to P5 and P6.

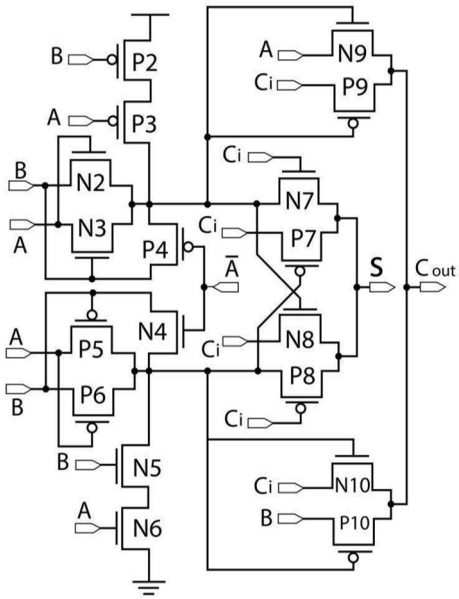

FIG a:Hybrid Full Adder-20 Transistor

The N4 is connected to N5.The signal B is given to N5 and the signal A is given to N6.The transistors P4 and N4 are shorted together and the out is A_{bar}. The signal A is given to N9 and C_i is given to P9.The N2 and N3 transistors are shorted together and output is given N7 and C_i is given to N7, C_i is given to P7.the N2 and N3 transistors are shorted together and output is given N7 and N8. The P5 and P6 transistors are shorted together and output is given P7 and P8 C_i is given to N8,P8.the output to N2 and N3 is given to N9 and P9 and output of P5 and P6 is given to N10 and P10.The signal C_i and B is given to N10 and P10.The output of N7 and P7 and output of N8 and P8 are shorted together and the output is sum. The output of N9,P9 and N10,P10 are sorted together and output is carry. The circuit is simulated in 45nm technology and result are obtained.

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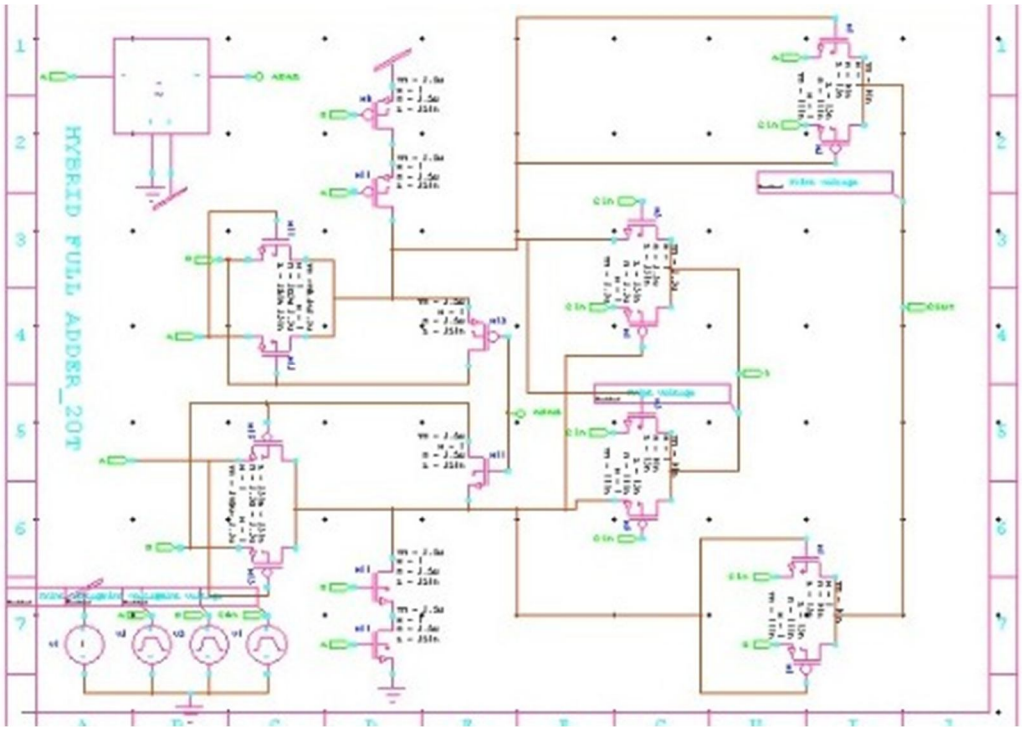

FIG b:Schematic Of Hybrid Full Adder-20 Transistor

The above figure shows the schematic of hybrid full adder -20 transistors which is combinations of number of PMOS and NMOS logic is designed in 45nm technology .It is designed with tanner S-EDIT Tool.

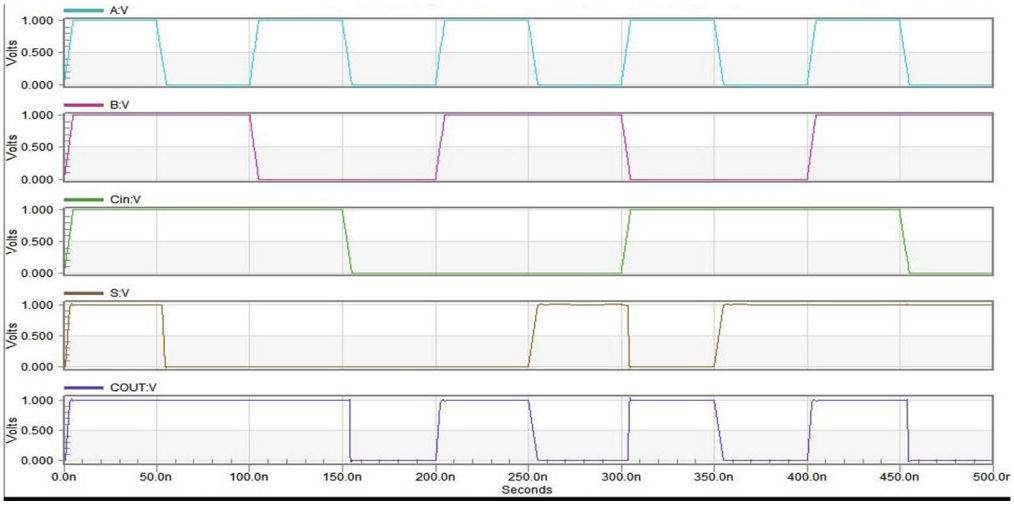

FIG c:Simulation Of Hybrid Full Adder-20 Transistor

The above figure shows the simulation results of Hybrid Full Adder-20 Transistor.It is simulated using CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis) Tool.Wave forms are analyzed using W-EDIT(wave form editor).
From the above simulation figure ,given that A=100nm ,B= 200nm and C= 300nm . let A=0 ,B = 0 , C = 0 then the sum is '0' and carry also '0' , if A = 0 , B = 0 ,& C= 1 then the sum is '1' and the carry will be '0' ,likely if A = 0 , B = 1 ,& C = 0 then the sum is '1' and the carry will be '0' , if A0= 0 , B= 1 ,& C = 1 then the sum is '0' and the carry will be '1' , if A= 1 , B = 0 ,& C= 0 then the sum is '1' and the carry will be '0',if A = 1 , B= 0 ,& C = 1 then the sum is '0' and the carry will be '1', if A = 1, B = 1 ,& C= 0 then the sum is '0' and the carry will be '1', if A= 1, B = 1 ,& C = 1 then the sum is '1' and the carry will be '1'

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Power Results

VV1 from time 0 to 5e-07
Average power consumed -> 6.315571e-07 watts
Max power 4.031336e-05 at time 1.54624e-07
Min power 4.691323e-11 at time 5e-08
```

FIG d :Power Analysis Of Hybrid Full Adder-20 Transistor

The above figure shows the power analysis of Hybrid Full Adder-20 Transistor. It analyzed by using tanner tool. The average power consumed around 6.31 e-007 watts. Max power 4.03e-05 Minimum power consumed around 4.69e-11 watts. For above simulation have done with 5 VDD.

```
Measurement result summary
   tdealy           =    48.4324n
```

FIG e:Delay Analysis Of Hybrid Full Adder-20 Transistor

The above figure shows the delay analysis of Hybrid Full Adder-20 Transistor. It analyzed by using tanner tool. The time delay is 48.432n.For above simulation have done with 5 VDD.

```
Measurement result summary
   pdp              =305.8782
```

FIG f:PDP Analysis Of Hybrid Full Adder-20 Transistor

The above figure shows the PDP analysis of Hybrid Full Adder-20 Transistor. It analyzed by using tanner tool. The PDP is 305.87.For above simulation have done with 5 VDD.

The input signal A is given to inverter which consist of P1 and N1 transistors.Carry signal C_i is given to inverter which consists of P2 and N2 transistor.The signal A is given to P3,P2 and signal B is given P2,N4.The output of P3,P2 are shorted together and is given to N4,the N4 is connected to N3.The signal A is given to N3 and signal B is given to N2.The output of P3,P2 is given to inverter which consists of P4 and N5.The output of inverter is given to N6,N7,N8,P7.

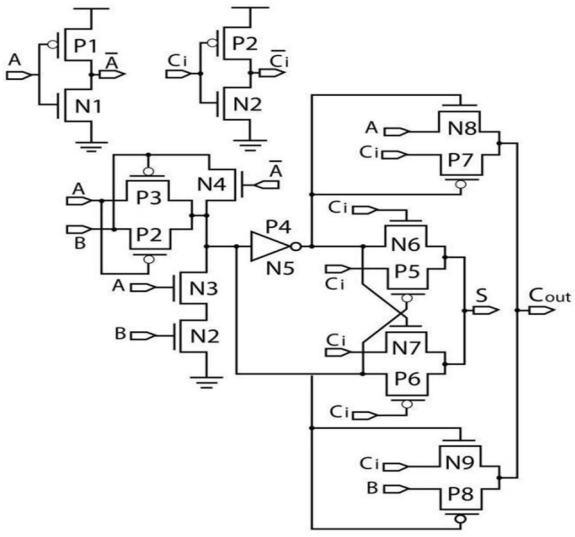

FIG g: Hybrid Full Adder 17 Transistor

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The signal C_i is given to N6,P5,N7,P6,N9,P7.The input of inverter is given P6 ,P5,N9 and P8.The output of transistors N6,P5 and N7,P6 are shorted together .The output is sum.The output of N8,N7 and N9,P8are shorted together and the output is carry.The circuit is simulated in 45nm technology and result are obtained.

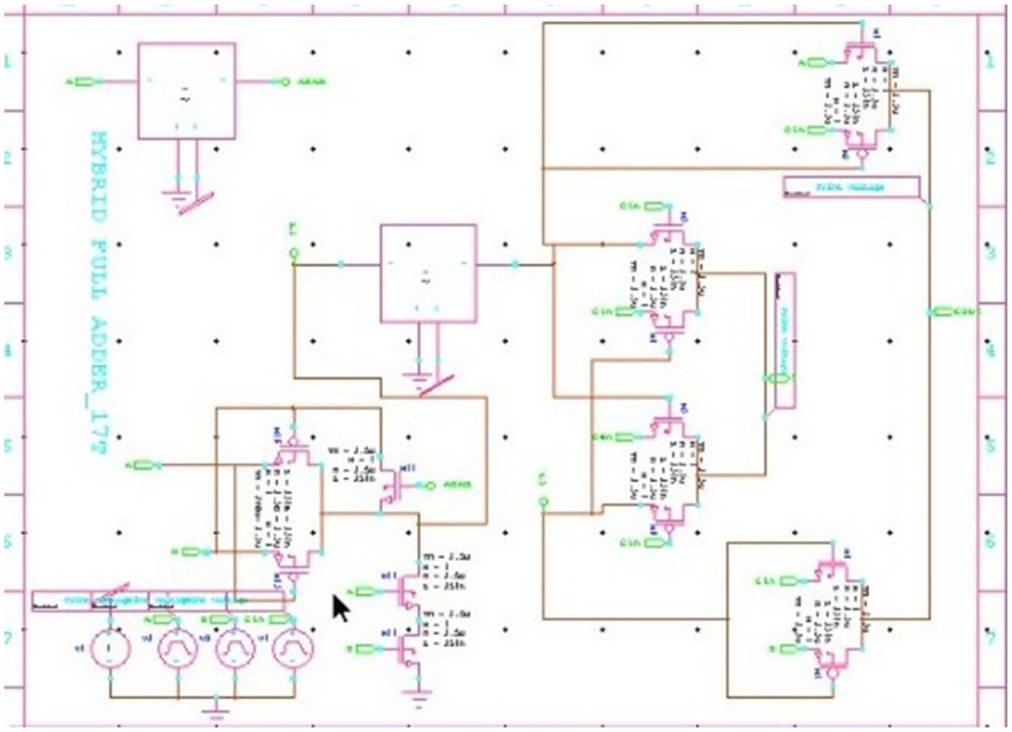

FIG h:Schematic Of Hybrid Full Adder 17 Transistor

The above figure shows the schematic of hybrid full adder -17 transistors which is combinations of number of PMOS and NMOS logic is designed in 45nm technology .It is designed with tanner S-EDIT Tool.

IV. TEST METHOD AND OUTPUT

A. Proposed Methodology Graphs

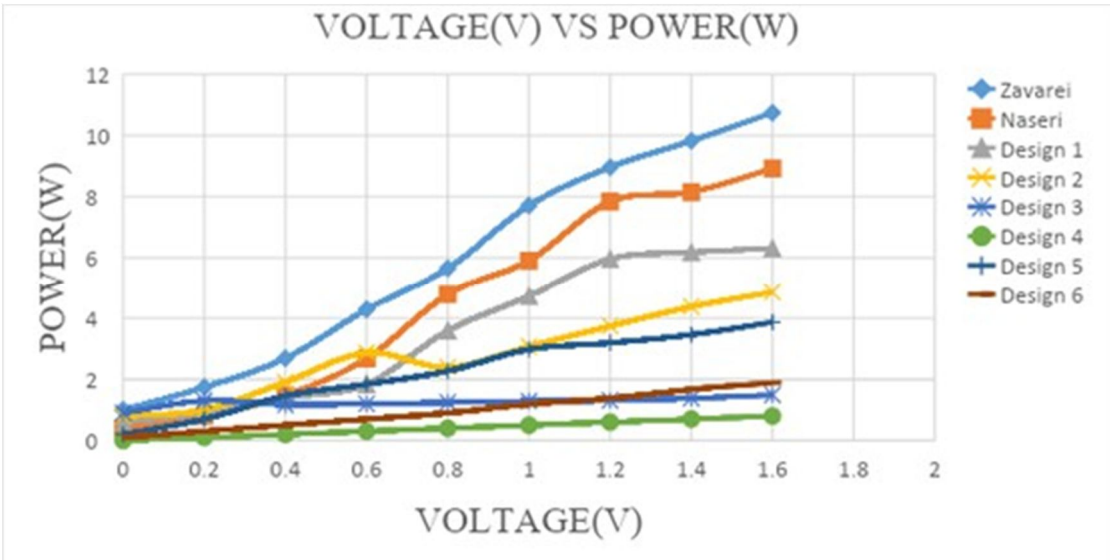

Fig:6.1a Simulation Results Of Full Adder,Power Vs Vdd

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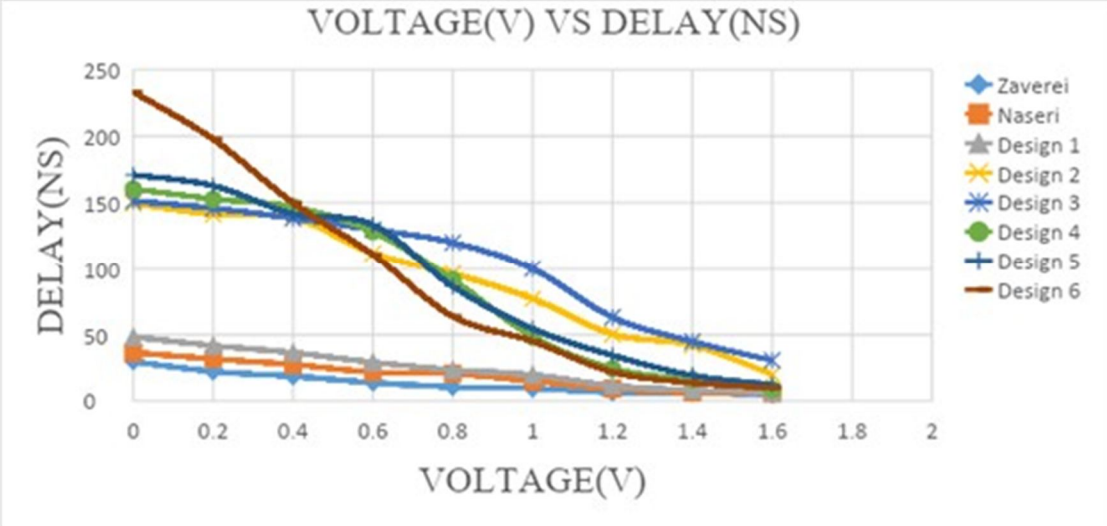

Fig:6.1b Simulation Results Of Full Adder,Delay Vs Vdd

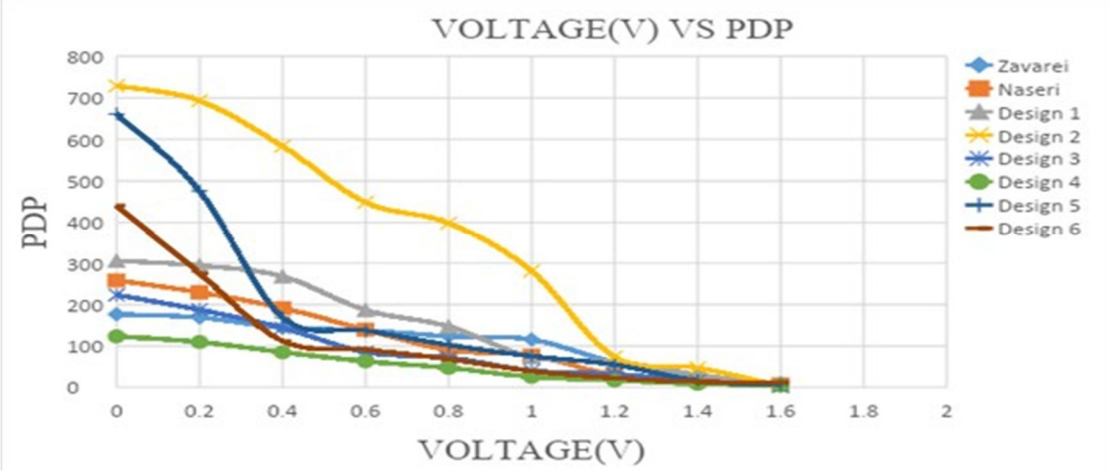

Fig:6.1c Simulation Results Of Full Adder,PDP Vs Vdd

V. CONCLUSION

In this undertaking we assessed XOR-XNOR schematics .The simulations depicts that the NOT doors in circuit is hindrance and another disservice is positive feedback. Because of feedback the delay, output capacitance and power utilization are expanded. Then we developed XOR-XNOR circuits, that might not have the above recorded drawbacks. By utilizing these XOR-XNOR gates, we developed three new FA circuits for different calculations. After reproduction of FA circuits in different ways, the outcomes show that this schematics has a generally excellent exhibition in all outputs. Simulation outputs tell us that the proposed FA schematics decrease PDP up to 23% examination with other FA circuit designs. Given circuits have good speed and power .

VI. FUTURE WORK

Low power efficiency has also become increasingly essential for high digital systems such as microcomputers, digital signal processors (DSPs), and other applications. As chip density and operation speed increase, increasingly sophisticated chips with increasing clock frequencies are designed. Low power design is also essential to minimise power into high-end case of high integration density and, as a result, enhance operating speed. In the that work, one- low-power hybrid FA (full adder) electronics circuit approach is constructed, and simulations that used an EDA tool has been accomplished.

Parameters are calculated, and their comparison is carried out in compliance with a variety of factors using a traditional full adverbs Full adders nowadays have a wide range of options.

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As a result, the power consumption and delay must be reduced. As has been shown, this may be accomplished using a low-power hybrid FA (full adder), and a comparison of the low-power full hybrid adder with other traditional adder circuits is made. The power consumption was reduced by using a low-power hybrid full adder use, power delay product, and delay are all terms that can be used to describe how something is used.

The reduction of power dissipation will be a focus of future effort.& space by lowering the number of transistors in use put into action implementing the low power hybrid full adder.

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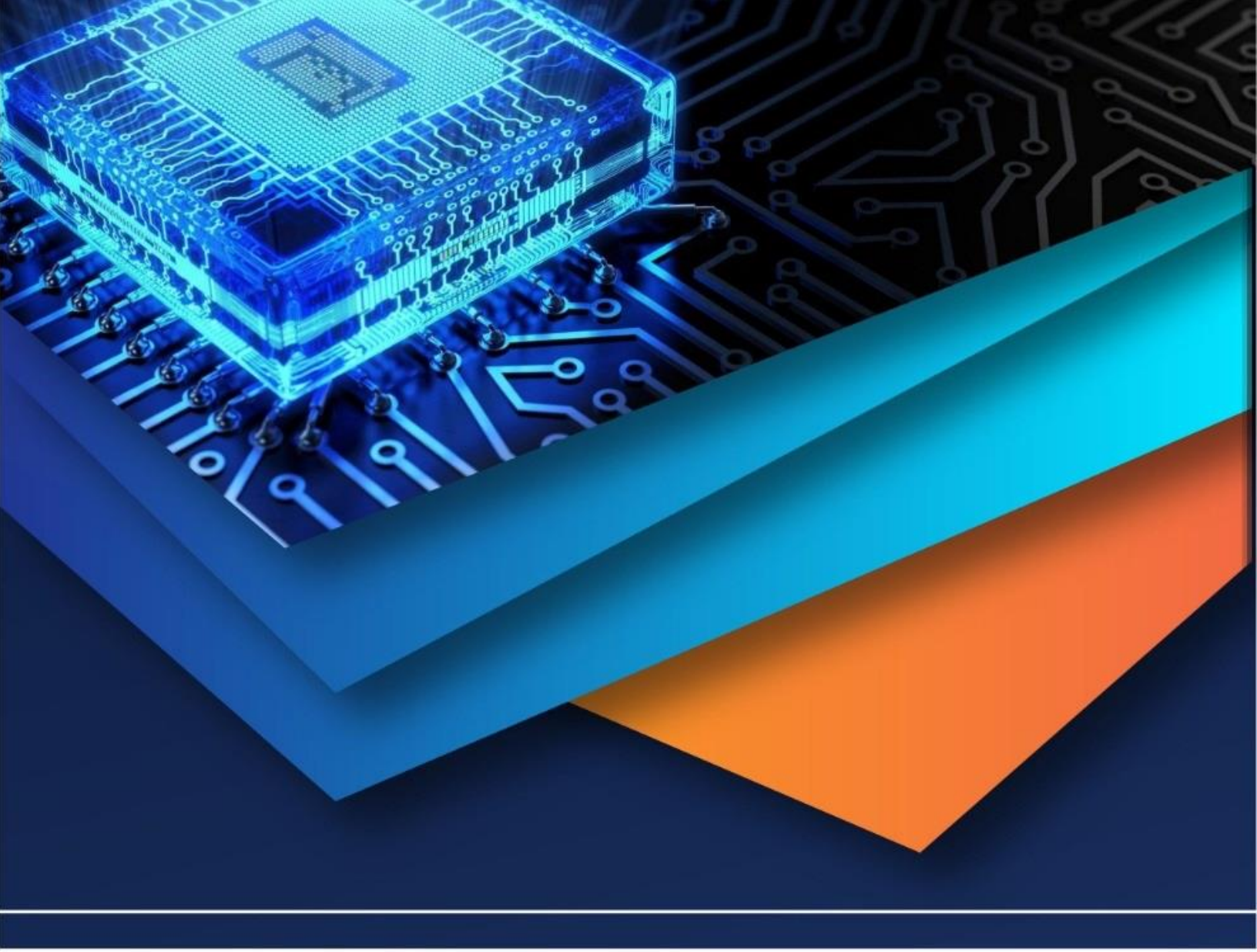

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