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Contention Mitigation based Level Shifter Architecture

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Abstract: ***Energy efficiency is one of the most important issues that needs to be solved in the current system on chip design. To overcome this issue, many circuits inside the chip run at low power. However there are some blocks like memories that run at relatively higher voltages. This means, modern day SOC contains different voltages running through it. The problem arises when two blocks operating at different voltages want to communicate with each other. This problem is solved by using Level Shifters as an interfacer between the blocks. The function of Level Shifter is to convert voltage level of input signal to that of the output. In this paper a cross coupled architecture of Level Shifter is proposed which operates between 1.5v and 5v. The speciality of this architecture is there is less contention between pull up network and pull down network, which reduces the rise and fall delay significantly. The proposed design is simulated at different operating conditions and the functionality is checked.***
Keywords: Level Shifter, System on Chip, Process, Temperature, Voltage,

I. INTRODUCTION

The Circuit design branch of chip design industry has advanced so much that a typical chip contains a billion transistors , millions of circuits are designed to get required functionalities. In addition to this, the low power requirement is met by reducing the voltage level of each circuits with the minimum value supported by them. Hence a modern SOC contains different power rails running through it. This is possible only with the assistance of Level Shifter cells, which act as translators when two circuits operating at different voltage level communicate with each other. Thus an SOC has thousands of Level Shifters in them, a small improvement in the design of this cell will significantly improve the chip's performance. This paper attempts to do the same by describing a cross coupled architecture which prevents contention between pull up and pull down network. The paper is organised as follows: The first section discusses about various challenges faced by multi voltage system design. Section2 discusses the influence of operating conditions on the performance of level Shifter. Then a conventional cross coupled structure is presented followed by a proposed architecture in section 3. Section 4 contains the simulation results and waveforms. At last section 5 wraps up the paper by including conclusion and future scope.

A. Multi Voltage System Design Challenges

Level-shifter are the most commonly used multi voltage systems. There are multiple challenges that can be of striking proportions when we proceed to implement. Some of the challenges are listed below:

1) *Level-shifters for Voltage Translation:* The level shifters designed should be in an advanced manner as the adaptive voltage scaling technique comes into the picture.
2) *Characterisation:* Digital characterisation of level shifter libraries are way harder than single voltage systems as the functional blocks operate at different voltages. The characterisation for different voltages is required which takes nearly double the time as single supply libraries.
3) *Static Timing Analysis:* There has always been a problem in multi-level systems in order to choose the voltage domain to separately do PnR and STA for multi-level blocks.
4) *Board Level Complexity:* The boards require multiple voltage sources and providing them with any unforeseen consequence is challenging.
5) *Floor Planning, Power Planning, Grids:* Multi power domains require detailed and complicated oor planning because the power grids are much more complex.
6) *Power Sequencing:* Complicated sequencing with reset pins is harder to design as the power switch designs to control involve complicated algorithms.

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II. INFLUENCE OF OPERATING CONDITIONS ON THE PERFORMANCE OF LEVEL SHIFTERS

A. Process

Firstly, about process, the variations are because of the manufacturing biases during which the production device may have variations in temperature, pressure and concentration of doping. The ICs that are produced, are in batches of 40-250 wafers. Therefore, the process variations occur in every chipset. The process parameters vary throughout the chip and hence we get different transistor lengths throughout the chip. As a result, the smaller transistor is faster and propagation delay is lesser. Based on this, the parasitic extraction results in the three RC corners- min RC, nom RC and max RC.

Process can be any of the three following cases:

1) *Strong Corner:* Higher dopant concentration or smaller transistor lengths. This causes the fastest transistors and corresponds to min RC. The strong process is a critical point for hold time failures.
2) *Nominal Corner:* Most of the transistors result in this process and follow the nom RC corner. These render to the ideal planned value of dopant concentration.
3) *Weak Corner:* Lower dopant concentration or larger transistor lengths. This causes the slowest transistors and corresponds to max RC. The weak process is a critical point for determining setup time failures.

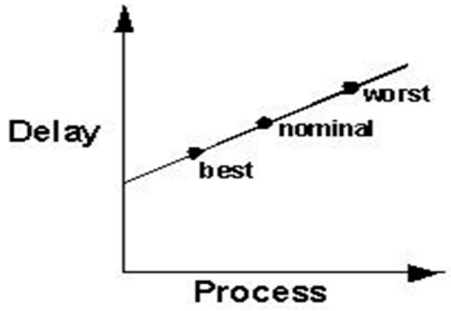

Fig. 2.1 Design corner variation with process

B. Temperature

The variation of temperature is unescapable in everyday operations of designs. Usually we consider linear scaling effects for temperature, but for the ultra-low-level processes such as submicron silicon processes, we require calculations that dwell into non-linearity. An operating chip can have temperature variations throughout the its functioning. We relate this to the dissipation of power in the MOS transistors. Most of the power consumption is due to the internal powers such as leakage powers, short circuit currents and internal switching. The dissipated power tends to rise the temperature of the immediate around regions. The mobility of a transistor also depends on the temperature. In semiconductors, we know that as temperature increases, the conduction also increases up to -50 °C, beyond which conduction pours down. As the electrons move slowly, the propagation delay increases and hence devices tend to mess up.

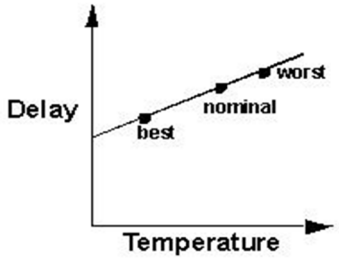

Fig. 2.2 Design corner variation with temperature

Also, another important parameter is the variation of threshold effect with temperature. Threshold voltage decreases as the temperature increases. Conversely, a lower threshold voltage has a higher current passing ability and has a lower delay. In the figure 2.2, we observe the same as explained above.

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C. Voltage

The supply voltage varies from the specified value as day passes. Although the calculation is extremely detailed, the operability conditions vary a lot too, which causes a deviation from the expected calculation. The power supply to a cell determines the point at which the cell saturates. The delay is in sync with the delay that the cells show. Therefore, the power supply inflects the propagation delay in a cell. Also, a finite drop in voltage occurs due to the intrinsic resistance of the metal wires. A higher supply voltage charges the load capacitance quicker and in doing so shows up a lower delay for the cell. Along with the resistive property and mutual capacitance offered by the metal lines, there is also a self-induced inductance that prevents any sort of rapid change in the supply rails thereby causing an additional drop.

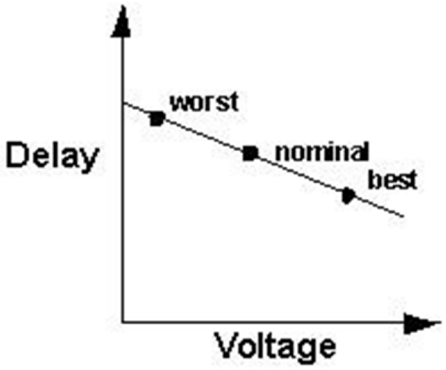

Fig. 2.3 Design corner variation with supply voltage

III. LEVEL SHIFTER ARCHITECTURE.

In this section the architectures of Level Shifter is discussed in great detail.

A. Conventional Cross coupled Level Shifter architecture

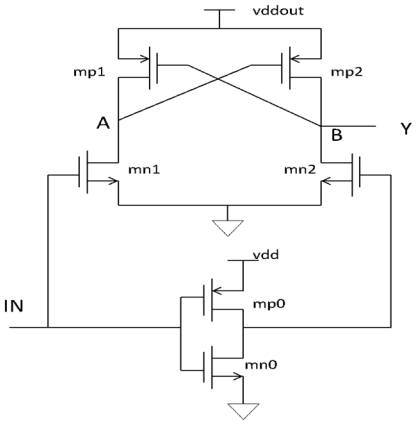

Fig. 3.1 Cross Coupled architecture

Fig 3.1 shows a typical cross coupled dual cascode voltage switch logic based Level Shifter architecture design. This design is also referred to as Dynamic Level Shifter design. It consists of transistors of two different voltage domains. mp0 and mn0 are rated at the input voltage level, while other transistors are rated at output voltage level. Transistors mn1 and mn2 are often called as legs of Level Shifter, these transistors are responsible for pulling down netA and netB to ground respectively. Transistors mp1 and mp2 form the cross coupled structure which provide positive feedback and are responsible for deriving the functionality. When input is low, mn2 turns ON, which drives netB to ground, thus getting the required functionality. NetB turns mp1 ON, which will drive netA to VDD, which then turns OFF mp2. When input transitions from low to high, mn1 is ON and mn2 is OFF, netA is pulled down which turns ON mp2, which then drives output node to VDD. The circuit seems to be absolutely perfect until one notices the contention between the pull up network and the transistor legs during transition. This contention leads to static power dissipation and maximum delays.

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B. Contention Mitigated Level Shifter Architecture.

The conventional Cross Coupled Level Shifter achieves the functionality with great success, but it was limited because of the contention between pull up and pull down network, which led to increase in rise and fall delay and also huge power consumption. The design presented in figure 3.2 overcomes this problem. In this design two pmos transistors are stacked in the pull up network. Transistors mp3 and mp4 whose gates are connected with the input and inverted input respectively, can mitigate the contention upto certain level. This is possible because when input is low, mn1 and mp4 are OFF, while mn2 and mp3 are ON. It is observed that either of the two transistors are ON at once. This will reduce the power consumption significantly and also reduce the delay. However mp2 and mp1 are not completely turned OFF, but the current flowing through them is comparatively less.

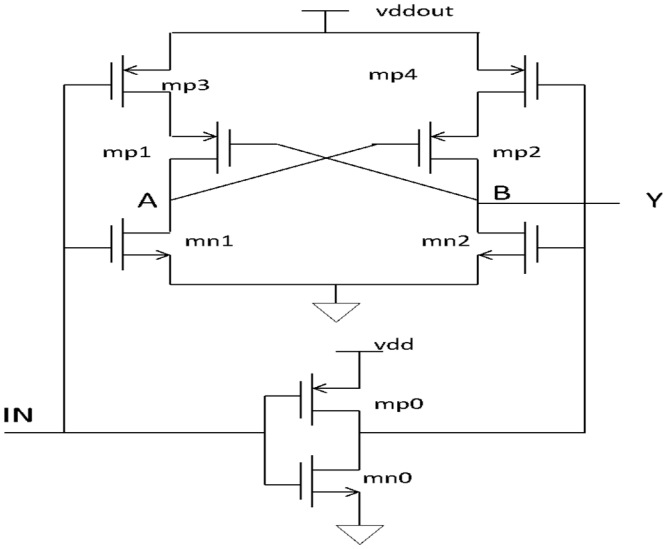

Fig. 3.2 Contention mitigated Level Shifter Architecture

IV. IMPLEMENTATION AND RESULTS

In this section, lets implement and simulate the design of contention mitigated Level Shifter that can upshift the signal of voltage level 1.5v to 5v. The design is created using 150 micro meter CMOS Technology. The functionality is checked and the delay and power consumed is measured. The Tool used for design and simulation is Cadence icfb and Cadence Spectre respectively. The simulation is performed at different operating conditions. For our convention, lets call level shifter as LVLUP_5V.

A. Implementation of LVLUP_5V

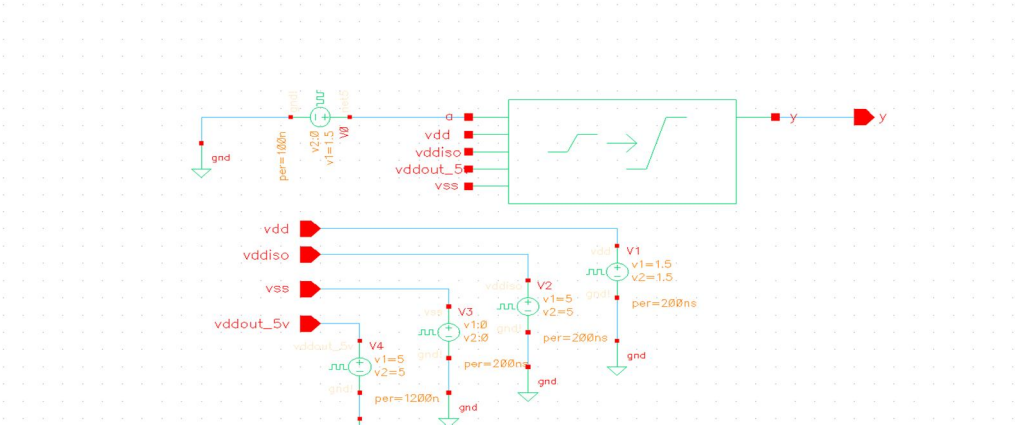

Fig. 4.1 Test circuit for a LVLUP_5V

Figure 4.1 shows the test circuit for a LVLUP_5. The input is driven by 100ns period with pulse width of 50ns. Pins vdd and vddout_5v are the voltage pins, and are driven by constant 1.5v and 5v DC voltage respectively. The Transient response at the output is captured in figure 4.2.

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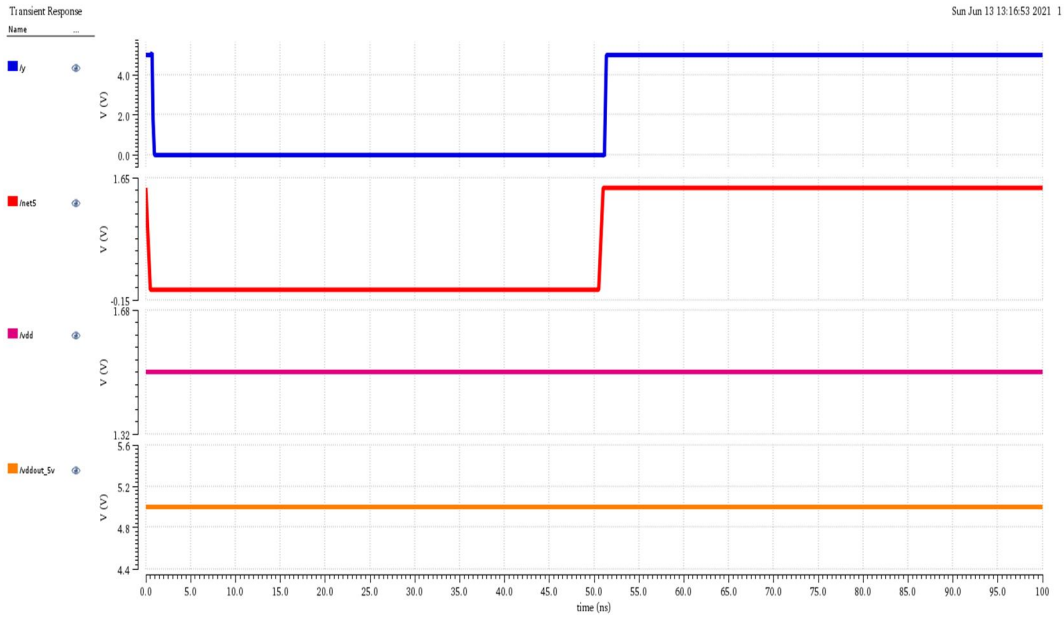

The red waveform is input signal with DC voltage level of 1.5v, the blue waveform is output signal, with DC voltage level of 5v. The Pink and orange are waveforms of voltage supply vdd and vddout_5v respectively.

B. Results

The circuits of design in figure 3.1 and 3.2 are simulated at different Process, Temperature and Voltage levels. The fall delay, rise delay and power consumed by the circuit is measured. Table 4.1 contains measurement data for level shifter architecture without contention mitigation and Table 4.2 contains measurement data for level shifter with contention mitigation circuitry.

P_T_V	Rise delay (ns)	Fall delay (ns)	Power consumed (uw)
N_25_1.5_5	0.884	1.194	10.75
S_25_1.5_5	0.724	0.820	9.99
W_25_1.5_5	1.11	2.30	13.71
N_25_1.65_5.5	0.809	1.16	13.20
S_25_1.65_5.5	0.660	0.795	12.22
W_25_1.65_5.5	1.02	2.04	15.83
N_25_1.35_4.5	0.977	1.499	9.455
S_25_1.35_4.5	0.801	0.939	8.33
W_25_1.35_4.5	1.25	4.93	7.85

Table 4.1 Results of Cross coupled Level Shifter without contention mitigation

P_T_V	Rise delay (ns)	Fall delay (ns)	Power consumed (uw)
N_25_1.5_5	0.842	0.823	7.55
S_25_1.5_5	0.683	0.683	7.98
W_25_1.5_5	1.058	1.030	7.18
N_25_1.65_5.5	0.762	0.758	9.26
S_25_1.65_5.5	0.618	0.634	9.76
W_25_1.65_5.5	0.959	0.939	8.80
N_25_1.35_4.5	0.940	0.928	6.05
S_25_1.35_4.5	0.764	0.761	6.40
W_25_1.35_4.5	1.182	1.1924	5.791

Table 4.2 Results of Contention Mitigated Level Shifter

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From Measurement data, it can be observed that The rise and fall delay values increases as thr process varies from Strong(S) to Weak(W). Also the delay increases as voltages increase. From comparision of the two tables, it is clearly visible that the delay and power consumption has significantly lesser for Contention Mitigated Level Shifter. The highest rise delay and fall delay from Table 4.1 are 1.25ns and 4.93 respectively observed for W_25_1.35_4.5, while the delay measured for the same PTV in Table 4.2 are 1.182ns and 1.192ns respectively.

V. CONCLUSION

Multiple supply voltage technology requires the use of level shifters on signals that move from one voltage level to another. If there is no level shifter, the signals across the voltage levels will not be sampled correctly. The level shifter is added to ensure that modules operating at different voltages will work properly when integrated into the SoC. In this paper an architecture of Dynamic Level Shifter that could mitigate the contention mitigation between pull up and pull down network was discussed. The Level Shifter could translate signals from 1.5v voltage domain to 5v voltage domain successfully. The functionality and performance of the design was checked by simulating the design at various operating conditions. The implementation for the same is performed and the results and waveforms were drawn. In the end the comparision between conventional cross coupler Level Shifter and Contention Mitigated Level Shifter was done and it was observed that proposed design took less time for both fall and rise transition and also consumed less power compared with conventional cross coupled Level Shifter.

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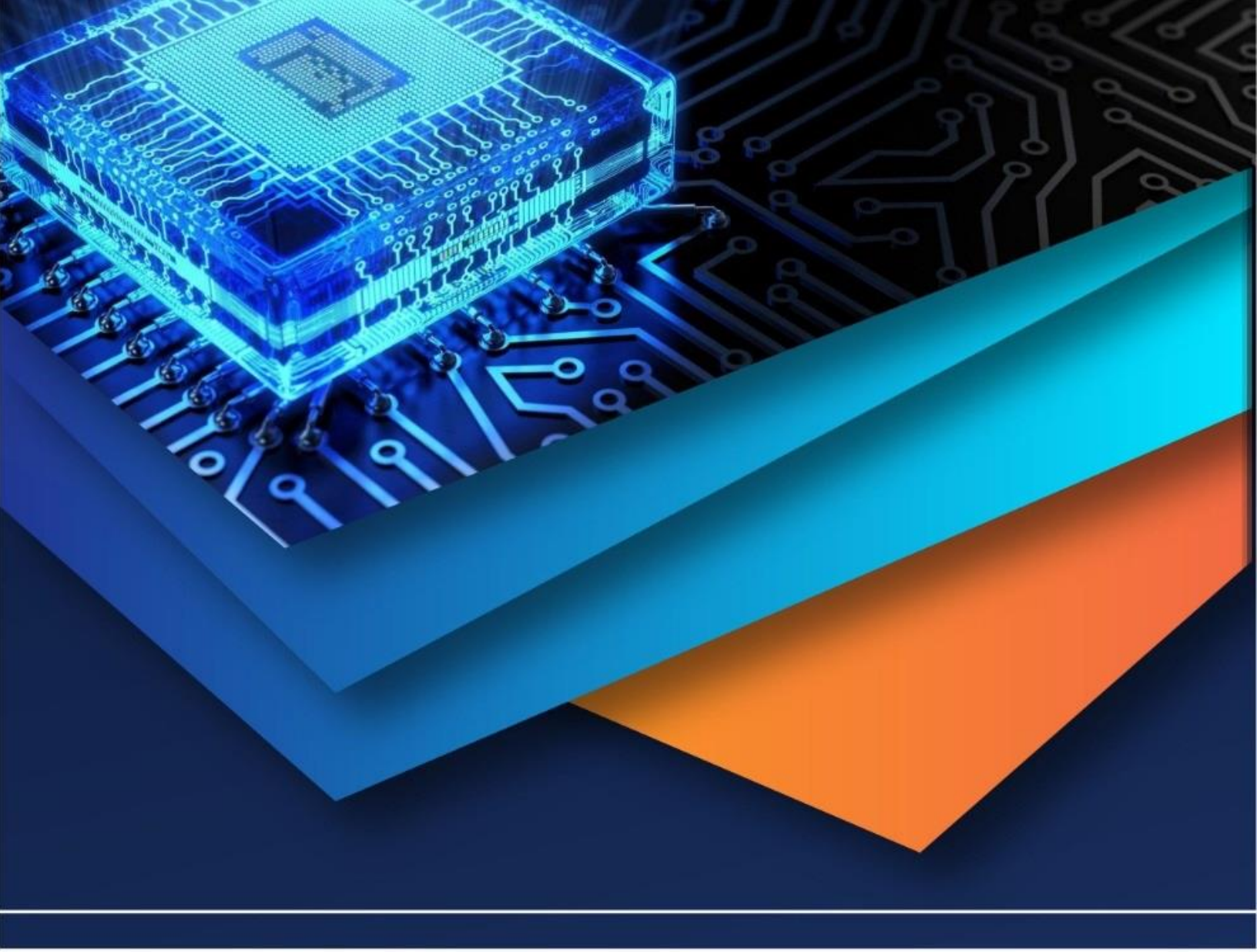

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