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Performance Analysis of TFET and VDSTFET for Low Power Application using the Work Function Engineering

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Abstract: We report a design of TFET which is quite different from conventional TFET. The structure of VTFET is similar to MOSFET but the conducting mechanism is completely different. Vertical TFET is designed perpendicular to the horizontal plane. The switching and carrier transportation mechanism of VTFET is based on the mechanism of the band to band tunneling through a potential barrier and vertical TFET is based on tunneling perpendicular to the device rather than a mechanism like thermionic emission unlike in MOSFET. We have designed a model for the two-dimension structure of V-TFET which consists of the dual-source and single drain. The channel among the drain and gate region is extraordinarily thin. We have plotted the transfer characteristics of V-TFET according to device parameters using TCAD. The comparison of VTFET with DSVTFET is done by using Silvaco TCAD and the effect of source doping, and work function on transfer characteristics of the device is examined by using silvaco TCAD simulations. The proposed device produces a low-off current.
Keywords:- Ambipolar current, Dual Source Vertical TFET (DSVTFET), Lateral TFET (LTFET), Band to Band Tunneling(BTBT), Work Function.

I. INTRODUCTION

With the consistent downscaling of the MOSFET, the performance of MOSFET has been declined because of the reduction in the dimensions of channel length, oxide thickness, and other dimensions at the nanometres scale. Scaling of the transistor at nanometre level results in an increase in leakage current and dominance of short channel effects like Surface scattering, Impact ionization, and Hot carrier Injection which is a very severe problem in circuit designing, To address the challenges to the continued scaling of transistors, the smaller transistors must also become "better" in terms of energy efficiency [7, 8]. To solve this issue, a new experimental transistor is introduced called TFET which is one of the most optimistic devices in the history of semiconductor devices which has the potential to outperform MOSFETs. TFET offers better characteristics as compared to MOSFET, especially in low-power application devices. Due to the capacity of providing subthreshold swing less than 60 mv/decade and a higher Ion/Ioff ratio TFET has an edge over MOSFET for low power applications.TFETs are more energy-efficient than MOSFET. Although TFET has low ON current which is one kind of downside in digital design because it creates delay which reduces the speed of circuits. The switching speed of TFETs is better than MOSFET because the carrier transportation phenomena are BTBT. The TFET is biased in such a way that it forms a structure of reverse biased P-I-N. The only arrangement that differentiates the structure of a TFET is the type of doping in the drain region source region is opposite in a TFET. But In conventional MOSFET channel and drain doping are identical. A basic structure of an n-type TFET is shown in Figure.1. A TFET is called n-type TFET if the drain region is doped with n+ and the source region is doped with p+.
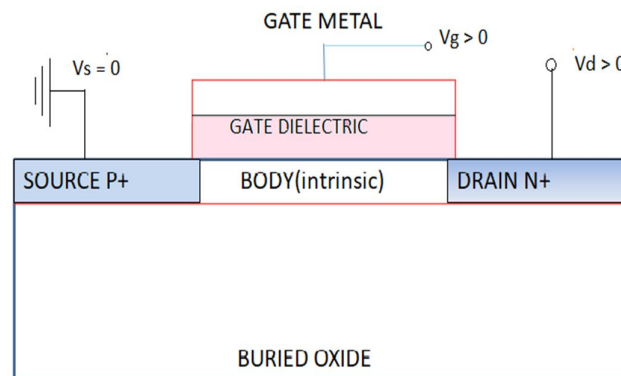

Fig. (1) N-Type TFET STRUCTURE

The channel is intrinsic or lowly doped with respect to drain and source of semiconductor and it is kept isolated from the gate terminal by using dielectric like conventional MOSFET. When the drain is doped with an n-type impurity and opposite to that source is doped as p-type then it is called as N TFET and the majority carrier in the channel are electron which results in conduction when a sufficient amount of the gate voltage is applied. Because of the opposite doping of drain and source, TFET exhibits an ambipolar nature. TFET is a symmetric device. In n-type TFET an electron as a majority carrier can exhibit a p-type nature with the dominant contribution of holes in current transportation whenever negative biased is applied to the gate terminal.

Working:-TFET works on the principle of quantum band-to-band tunneling (BTBT). BTBT injects carriers from the valence band into the conduction band through the forbidden bandgap.The representation of energy Band diagrams of an n- TFET is shown in Figure 1(b). The gate voltage controls the conducting state of TFET, When the applied gate potential is very low or near about zero, the TFET exhibits in the OFF-state. There is a significant gap between the conduction band in the channel region and the valence band in the source. As a result, BTBT can not occur and the TFET is considered to be in the OFF-state and negligible amount of current flow across the channel. When the applied gate potential is increased, the established electric field modulates the carrier density below the gate, this results in the down push of the conduction band in the channel region. When a sufficient amount of voltage is applied to the gate, there is band bending at the source interface in such a way that the valence band in the source and the conduction band in the channel get aligned, as shown in Figure 1(b), As a result, there is a clear path for band to band tunneling and electron in valence band started to tunnel into to the conduction band in the channel.
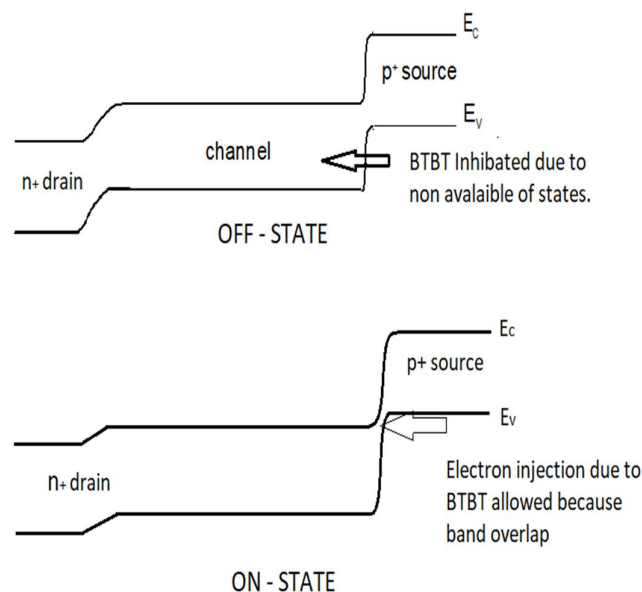

Fig.1(b).Energy Band diagram of N -TFET On and OFF state

II. DEVICE MODEL AND PARAMETERS

In this paper, we proposed DVTFET which has the same mechanism as BTBT like LTFET(Conventional TFET) but the direction of tunneling is different. In TFET (LTFET) tunneling takes place parallel to the Si-oxide interface but in VTFET tunneling occurs perpendicular to the oxide silicon interface. This paper introduces U-shaped TFET and implements TFET results in steeper subthreshold slope with improved drain current characteristics. U shaped Vertical TFET provides a better area for effective tunneling which also improves drain current flow. In comparison to the conventional TFET, the U-shaped Vertical TFET consists of U-shaped Vertical dual source with an effective thinner channel length up to 8nm which meritoriously doubles the tunneling area and improves the drive current. It is also observed and examined that drain doping also enhances the on-current of TFET. This device is fabricated using silicon material which can further scalable and simulated following Moore's Law [8-10], A narrow spacing between the drain and gate region is introduced so that symmetric

device structure is obtained which can eliminate the problem of the short channel effects like Drain induced barrier lowering, Hot Carrier effect. We have examined the V-DSTFET device with the conventional TFET and channel and transfer characteristics between drain voltage and work function are examined by using TCAD simulations. The drain and source length are kept at 18 nm.
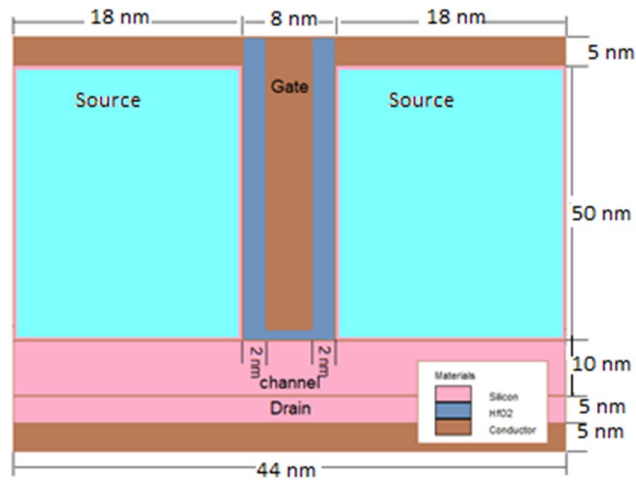
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Fig.2. (a) Planner structure of proposed Dual Source Vertical Tunnel Field Effect Transistor.

Table.1. Design parameters of proposed Dual Source TFET

Source Doping (N_A)	10^{20} /cm3
Drain Doping (N_D)	10^{19} /cm3
Channel Doping (N_C)	10^{17} atoms/cm3
Gate Length (L_G)	8 nm
Drain Height(H_D)	5 nm
Source Height(H_S)	50 nm
Channel Height(H_C)	10 nm
Source Length (L_{source})	18 nm
Drain Length (L_{drain})	44 nm
Gate Oxide Thickness(t_{ox})	2 nm
Gate Work Function	3.8 ev

The model properties for the dual-source vertical TFET (DSVTFET) are the same as that of conventional VTFET except that using dual-source and having a different direction of tunneling.
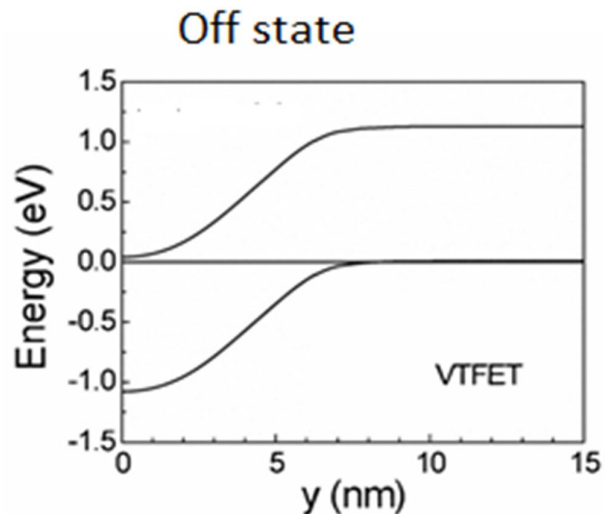

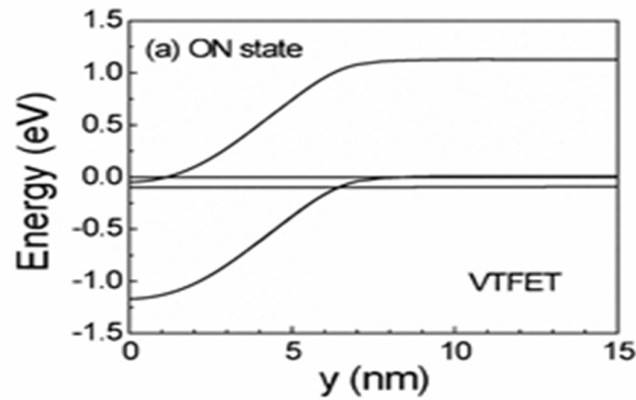Fig.3.(b) Energy Band diagram of Vertical TFET for OFF state

Fig.3(c) Energy Band diagram of Vertical TFET for ON state

Figures 3(b) and 3(c) show the energy band diagram of the VTFET in Figure 2. At the OFF state, the tunnel barrier spacing is extremely thin, but still, there is no overlapping between the valence band of drain and the conduction band of source, Hence BTBT cannot occur. At ON state, there is an overlap between the conduction and valence bands of source and drain. As a result, there will establish current flowing across the channel. But that is different from the Lateral TFET, in which there is already overlapping of bands at the OFF state, but there is no amount of tunneling current across the junction because of the thickness of the barrier height.

III. SIMULATION RESULT AND PERFORMANCE

All the results have been analyzed and obtained by using SILVACO TCAD tool. The mathematical equation of subthreshold slope is given below:-

$$AVSS = \frac{(V_{th}-V_{off})}{\log(I_{vth})-\log(I_{voff})}$$

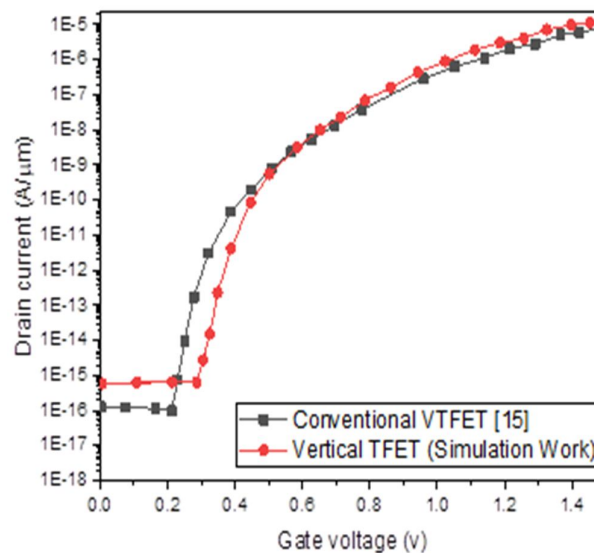#### A. Comparison of DSVTFET with Conventional VTFET

Fig.3(a). Simulated drain current outcome of VTFET compared with the Conventional VTFET.

The model properties for the dual-source vertical TFET (DSVTFET) are similar to that of conventional VTFET except that using the dual-source region instead of using single-source region which provides better symmetry to suppress the ambipolar current

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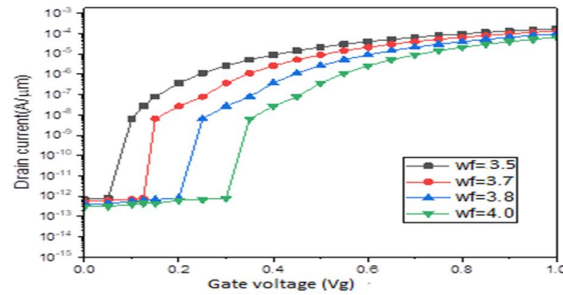
B. Work Function Engineering of DSVTEFT

Fig.3(b). Transfer characteristics of N-type Dual Source VTFET by varying the value of work function.

It is observed that the threshold voltage of TFET is adjusted optimized for better performance, The drain current increases when the work function decreases and it is clearly shown in Fig.3(b) that graph is shifted upwards when the value of the work function is set to be 3.5 eV and the optimum threshold is obtained 1.5V.
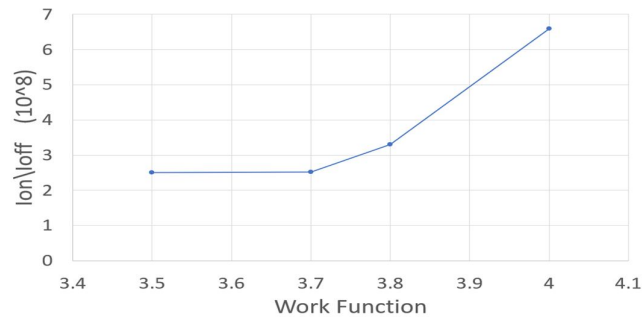

Fig.3(d). Transfer characteristics between work function and I_{on}/I_{off} for Dual-source VTFET

Table.2. Performance comparison for different WF in n-type Dual-source VTFET.

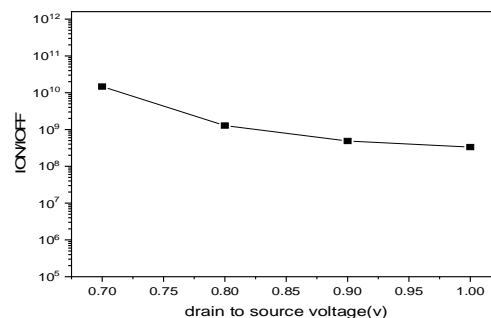| Wf	V_T (v)	Subvt (mv/decade)	I_{off} (A/µm)	I_{0n} (A/µm)	I_{on}/I_{off}
3.5	.15	12.77	$6.82 * 10^{-13}$	$1.74 * 10^{-4}$	$2.52 * 10^{8}$
3.7	.25	12.77	$5.31 * 10^{-13}$	$1.35 * 10^{-4}$	$2.50 * 10^{8}$
3.8	.35	12.77	$2.89 * 10^{-13}$	$9.89 * 10^{-5}$	$3.33 * 10^{8}$
4.0	.45	12.77	$9.85 * 10^{-15}$	$6.67 * 10^{-5}$	$6.69 * 10^{9}$

Fig.3(d).Transfer characteristics between V_{DS} and I_{on}/I_{off} for n-type dual-source V-TFET

IV.   CONCLUSION

In conclusion, we have analyzed the basic principle of TFET and analyzed the performance of DSVTFET by using work function variations and plotted transfer characteristics. Results show the dependency of the I_{on}/I_{off} current with work function and it increases by decreasing work function. The Dual-Source VTFET exhibits a comparatively high current at low supply voltages (V_{GS} = 0.5 V and V_{DS} = 0.8 V). We obtained the optimum threshold value of TFET for the maximum I_{on}/I_{off} ratio by using TCAD simulations.

REFERENCES

[1]   Choi, Woo Young, et al. "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec." IEEE Electron Device Letters 28.8 (2007): 743-745.

[2]   Gopalakrishnan, Kailash, Peter B. Griffin, and James D. Plummer. "I-MOS: A novel semiconductor device with a subthreshold slope lower than kT/q." Digest. International Electron Devices Meeting, IEEE, 2002.

[3]   Khatami, Yasin, and Kaustav Banerjee. "Steep subthreshold slope n-and p-type tunnel-FET devices for low-power and energy-efficient digital circuits." IEEE Transactions on Electron Devices 56.11 (2009): 2752-2761.

[4]   Kao, Kuo-Hsing, et al. "Direct and indirect band-to-band tunneling in germanium-based TFETs." IEEE Transactions on Electron Devices 59.2 (2012): 292-301.

[5]   W. V. Devi, B. Bhowmick and P. D. Pukhrambam, "N+ Pocket-Doped Vertical TFET for Enhanced Sensitivity in Biosensing Applications: Modeling and Simulation," in IEEE Transactions on Electron Devices, 67.5 (2020): 2133-2139.

[6]   Semiconductor Industry Association (SIA), International Technology Roadmap for Semiconductors (ITRS), 2015.

[7]   Hoefflinger, Bernd. "ITRS 2028—International roadmap of semiconductors." CHIPS 2020 VOL. 2. Springer, Cham, 2016. 143-148.

[8]   K. K. Bhuwalka, J. Schulze and I. Eisele, "Scaling the vertical tunnel FET with tunnel bandgap modulation and gate workfunction engineering," in IEEE Transactions on Electron Devices, 52.5 (2015) : 909-917.

[9]   E. Ko, H. Lee, J. Park and C. Shin, "Vertical Tunnel FET: Design Optimization With Triple Metal-Gate Layers," IEEE Transactions on Electron Devices, 63.12 (2016): 5030-5035.

[10]   Bhuwalka, Krishna Kumar, et al. "Vertical tunnel field-effect transistor." IEEE Transactions on Electron Devices 51.2 (2004): 279-282.

[11]   W. Li and J. C. S. Woo, "Vertical P-TFET With a P-Type SiGe Pocket," in IEEE Transactions on Electron Devices, 67.4 (2020):1480-1484.

[12]   K. Vanlalawpuia and B. Bhowmick, "Investigation of a Ge-Source Vertical TFET With Delta-Doped Layer," in IEEE Transactions on Electron Devices, 66.10 (2019): 4439-4445.

[13]   N. Paras and S. S. Chauhan, "Optimization of Design Parameters for Vertical Tunneling Based Dual Metal Dual Gate TFET," 2019 International Conference on Advances in Computing and Communication Engineering (ICACCE), 2019, pp. 1-5, doi: 10.1109/ICACCE46606.2019.9079988.

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