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Power Analysis of Sequential Circuits Using Multi-Bit Flip Flops

Yarramsetti Ramya Lakshmi[1], Dr. I. Santi Prabha[2], R.Niranjan[3]
[1]*M.Tech,* [2]*Professor, Dept. of E.C.E.*
University College of Engineering, JNTUK, Kakinada, India-533003
[3]*Member of Technical Staff, Seerakademi, Hyderabad*

Abstract: **In today's VLSI technology, power is the major issue with shrinking technology. Clock will play important role in the integrated circuits. In this paper, Multi-bit flip flop technique has been introduced to reduce clock power. The idea behind this technique is that clock power savings can be achieved by using multi-bit flip flop cell with optimized design. Recent works have been proposing methods using multi-bit flip flops in standard cell based designs, where single-bit flip flops are replaced by multi bit flip flop cells during logic & physical synthesis. In this paper a comprehensive comparison between conventional flip flop and MBFF implementations of an industrial 90nm design has been done. Sequential circuits has been designed using single-bit flip flop and multi-bit flip flop.**

Keywords: ***Multi-bit Flip flop, Dynamic Power reduction, Synthesis, Single-bit Flip flop, clock network***

I. INTRODUCTION

Several lower power design techniques have played an important role in the design flow. Clock gating methodology is used for the register bank to replace the multiplexers and it can avoid the operation of reloading the same data value. The clock gating technique could reduce the dynamic power consumption efficiently. The multi-V_{th} concept is aimed at using multi-V_{th} cell with satisfying performance to reduce leakage consumption, and replace lower V_{th} (LVT) cells by high V_{th} (HVT) ones, if there is room for slack. Multiple Supply Multiple Voltage Design of different voltages are used for core logic, base on satisfy performance or functional requirement to adjust operating voltage for each domain, even shut off this domain.

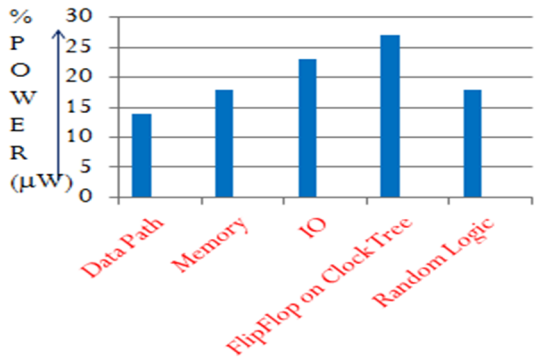

Fig 1: ASIC chip power distribution.

Various approaches to minimize clock network including buffer sizing, register placement optimization and applying multi-bit registers or register banks or multi- bit flip-flops (MBFFs).
Synopsys Design Compiler supports users to synthesis their design with multi-bit flip-flop methodology. In the next section, we briefly overview the multi-bit flip-flop conceptions. Section III presents how to use Synopsys Design Compiler and Synopsys's multi-bit flip-flop cell library to synthesis netlist. Section IV presents experiment results are shown. Finally conclusions are presented in Section V.

II. MULTI-BIT FLIP FLOP CONCEPT

In this section, Multi-bit Flip flop concept is explained. Before that, we will review about single-bit flip-flop.

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A. Single-Bit Flip Flop (SBFF):

It has two latches (Master latch and slave latch). The latches uses two clock phase signals to perform operations. These clock phase signals are opposite in order to have better delay. Hence there are cascaded inverters in the clock path. Fig 2 shows an example of single-bit flip-flop.

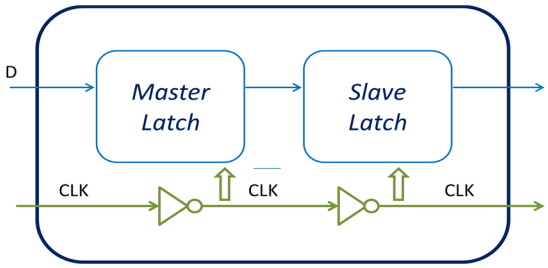

Fig 2: one-bit Flip flop before merging

B. Multi-Bit Flip Flop(MBFF):

Fig 3 shows an example of dual-bit Flip flop. As shown in figure cascaded inverters used to generate the opposite clock phase signals used by the master and slave latches. As the process technology shrinks beyond the value, even a minimum number of inverter/buffer can still drive multiple flip-flops. By merging more number of 1-bit flip-flops with one multi-bit flip-flop (MBFF) will reduce the number of inverters.

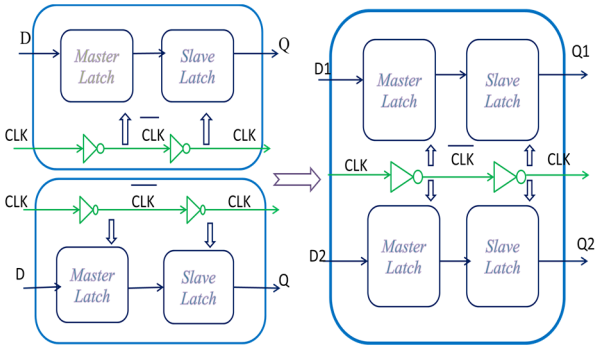

Fig 3: Dual-bit Flip flop after merging

By combining one or more SBFF cells with MBFF cells results in optimized area and transistor-level layout by sharing part of the circuitry. In conjunction with area and power savings at the cell level, Multi-bit Flip flop cells has following advantages:

A gate-level net list with MBFFs has a reduced of clock sinks in clock tree and dramatically reduces clock dynamic power.
Lower power consumption due to fewer clock sinks.
Smaller area and delay, due to shared clock drivers.
Reduced clock skew in sequential gates

As shown in Fig 4 Dual-bit Flip flop has two data input pins, two data output pins, one clock pin and reset pin. As shown in the truth table of dual-bit flip-flop cell. At positive edge of ck, the value of Q1,Q2 will pass to D1,D2. At negative edge of ck Q1 and Q2 will keep original value.

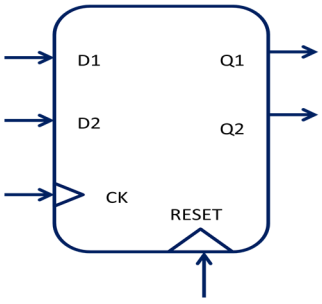

Fig 4: Dual-bit flip flop cell

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CK	D1	Q1	D2	Q2
↑	L	L	L	L
↑	L	L	H	H
↑	H	H	L	L
↑	H	H	H	H
↓	X	D1	X	D2

Table1: Truth table of Dual-bit Flip flop

III. IMPLEMENTATION PROCESS

Fig 5 shows the ASIC Design flow with MBFF optimization. Figure 6 shows Synthesis stage with MBFF optimization.

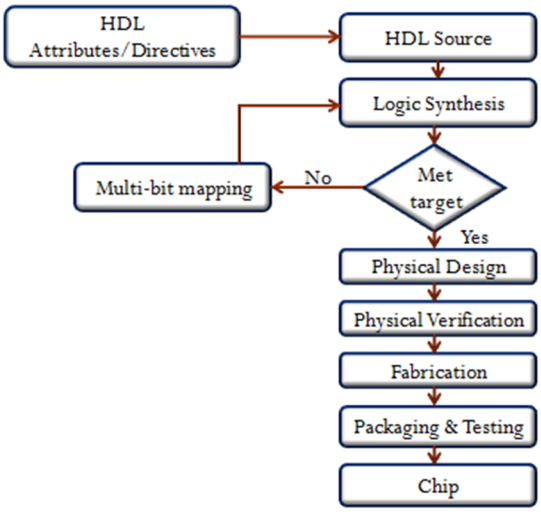

Fig 5: ASIC Design flow using MBFF methodology

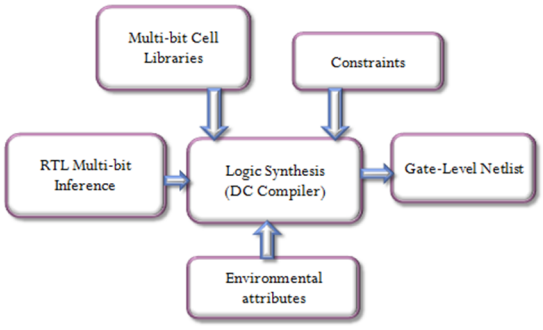

Fig 6: Synthesis flow for MBFF methodology

In the section, use of Design Compiler and Synopsys 's multi-bit flip-flop to implement ASIC design has been introduced.

A. Features of Multi-Bit Flip Flop Library

Multi-bit component is a group of cells with identical functionality with same clock and set/reset condition. Design Compiler can invoke multi-bit flip-flop cell library to replace the original single-bit flip-flop structure. Multi-bit flip-flop cell library must have some feature as following:

The D input pin has to be labeled as "bundle".

The flip-flop's function has be marked as "ff_bank"

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Fig 7 shows a part of Faraday's multi-bit flip-flop cell library.

```
bundle(D) {
  members(D1, D2);
  nextstate_type : data;
  direction : input ;
  pin(D1) {
```

```
ff_bank(IQ, IQN, 2) {
  next_state : "D";
  clocked_on : "CK";
}
```

Fig 7: Library requirement in Multi-bit flip flop

B. Inferring Multi-Bit Components

Design compiler uses multi-bit inference for all bused registers, multiplexers and three state circuits. There are two methodologies for inferring multi-bit components. First methodology involves directing multi-bit inference from the HDL source. The directives for verilog are *infer_multibit* and *dont_infer_multibit.* dc_shell variable controls multi-bit inference by using *hdlin_infer_multibit [default_none | default_all].*Second methodology involves directing multi-bit inference from a mapped design.

C. Script Execution Flow

Fig 8 show execution flow of commands in script using Design Compiler.

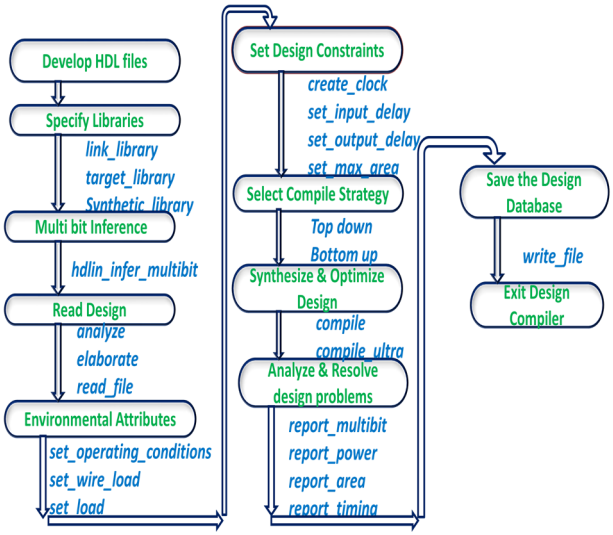

Fig 8: Command execution flow

D. Sequential Circuits

In this paper, multi-bit flip flop technique implemented on sequential circuits. In this paper, single-bit flip flops and multi-bit Flip flop are analyzed. Shift Resisters such as serial-in serial-out register ,Universal shift register and Counters such as Ring counter are implemented for SBFF and MBFF.

IV. EXPERIMENTAL RESULTS

The analysis of sequential circuits are designed using MBFF and implemented using Synopsys's Design Compiler. The simulation results of SISO register, Universal Shift Register and Ring Counter, RAM are shown in the figure. Table shows power ratio for sequential circuits before and after merging Flip flop.

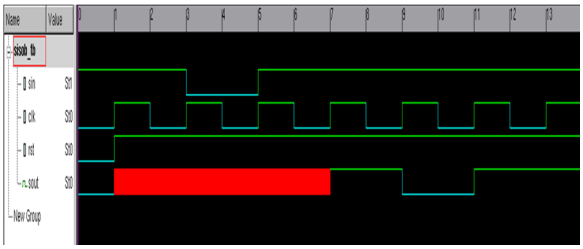

Fig 9: Simulation result for SISO

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Fig 10: Simulation result for Universal shift register

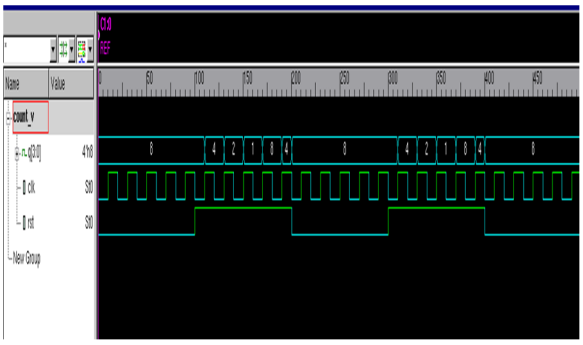

Fig 11: Simulation result for Ring Counter

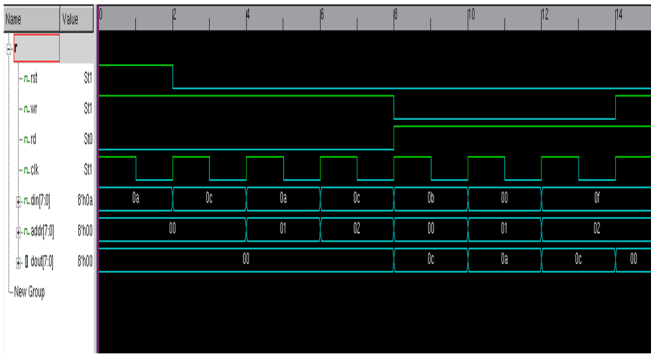

Fig 12: Simulation result for 8 x 256 RAMS

Design	Before Merging(µW)			After Merging(µW)			Power Ratio(%)		
	4-bit	8-bit	16-bit	4-bit	8-bit	16-bit	4-bit	8-bit	16-bit
Shift Register	8.7383	35.5830	69.8213	8.7893	19.1368	22.5414	0.5	46.22	67.72
Universal Shift Register	41.3916	56.3426	116.2324	21.7907	34.6197	39.7866	47.35	38.55	65.77
Ring Counter	10.9288	10.8144	11.7284	9.3983	8.9635	1.3952	14.00	17.12	88.10
8x256 RAM	1240.4			995.3192			19.75		

Table 2: Comparison result for Power

V. CONCLUSION

In this paper, we have implemented ASIC design with Synopsys Design Compiler and Synopsys's multi-bit flip-flop. Single bit flip flop and Multi-bit flip flop cells are implemented for Sequential Circuits to achieve low power using Synopsys Design Compiler with Multi-bit Cell Library. Experimental results indicate that Multi-bit flip-flop is very effective and efficient method in lower-power designs. This methodology to implement real ASIC project in the future.

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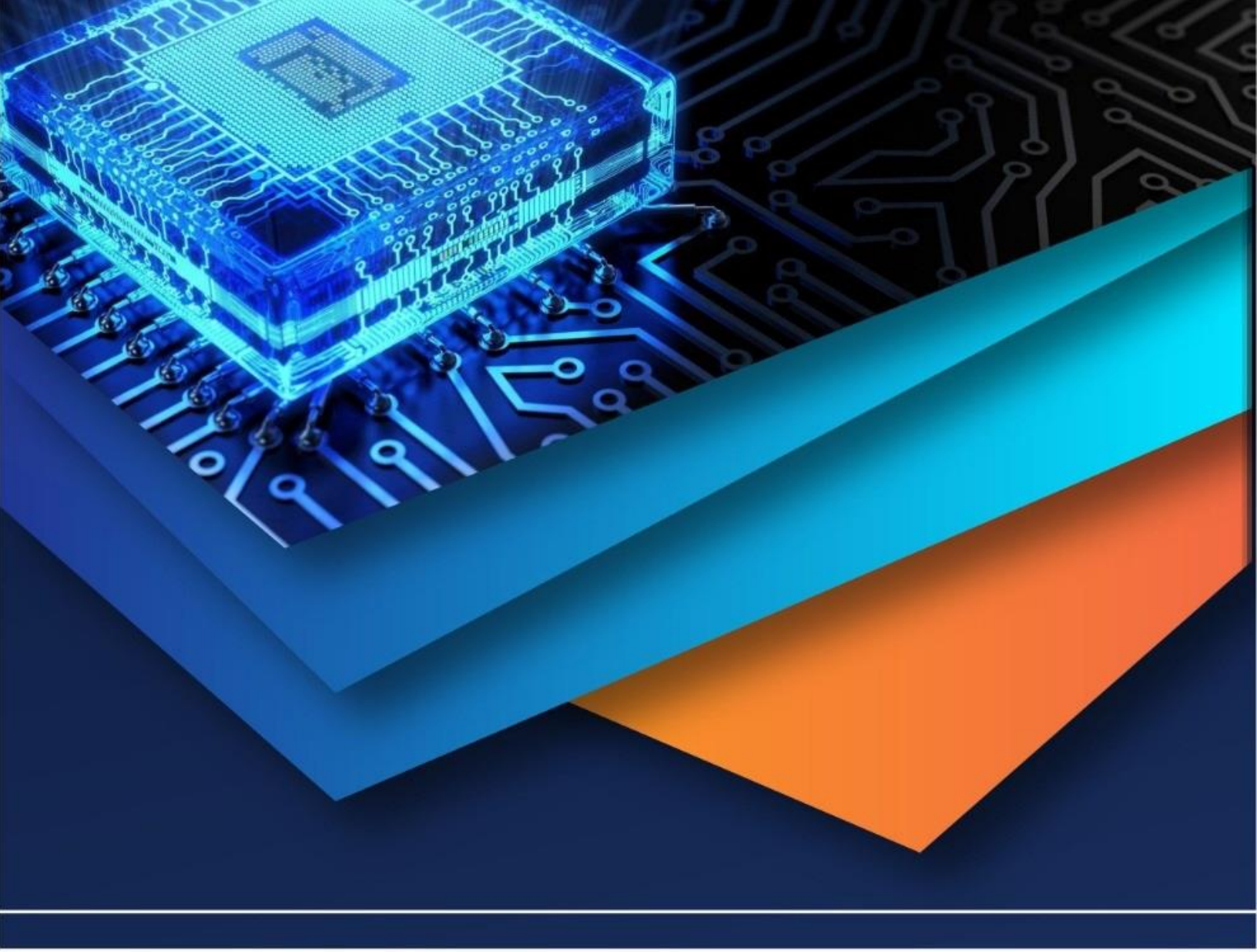

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