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Verification of Dual Port RAM using System Verilog and UVM

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Abstract: ***Verification process place a prominent role in the field of SoC and ASIC design. Several verification methodologies are there apart from those Universal Verification Methodology (UVM) is advanced and it is widely used by the industries due to its special features. UVM provides reusable and well-structured verification components by using System Verilog class library. In this work, Dual Port RAM is considered as Design Under Test (DUT). System Verilog and UVM verification environments are developed to verify the DUT. Assertion and cover group coverage are set up with a goal of achieving 100% from both the environments.***

Keywords: ***Verification, System Verilog, Testbench, Environment, UVM.***

I. INTRODUCTION

In ASIC applications higher priorities are given to multi-port memories due to usage of on chip shared memory concept in the systems. To reduce the complexity of the design developments done over multi-port, as a result multi-port SRAM compiler are developed to achieve high speed and high level of integration [5]. Overall chip performance can be increased due to parallel operations done by using multi-port RAM. Recent works are done with multi-processor system come up with an added feature in which Dual Port RAM takes a higher priority. DPRAM have an advantage over single port RAM, with the same number of cycles it can perform multiple Read\Write operations at the same time [1]. Dual Port RAM consist of two ports port A and port B. Both ports have an ability to perform Read\Write or Read only or Write only, these operations are controlled by clock [10].

In simple words we can define a verification, it is the process of checking the design which is working correct or not with respect to the expected result. Verification plan has to be made to describe what needs to verify, how to verify and what are all the features to be covered in verification. System Verilog (SV) is a standard hardware description language and it is also used for verification. It is extended from improvement to IEEE 1364 verilog-2001 standard. It inherits the features from Verilog HDL, VHDL, C and C++. System Verilog is used to design and implement electronic circuits, they are going to verified by generating the testcases using OOPs concepts [11]. Rapid growth in the chip manufacturing process leads to integrate million number of transistors on a single chip. Difficulty in verification arises and overall, it slows down the chip design. Apart from the entire design cycle 70 to 80 percent of the time consumed by functional verification. To avoid the gap between production of product and time to market, it is necessary to use verification methodology with an effective environment. Reusability is one of the criteria of effective verification process. VMM\UMV and many of VIPs are some of verification methodologies for reuse, so that verification environment can be built quickly [19]. Most of the IC design manufacturing industries adopted UVM verification methodology to avoid complexity in verification and to achieve verification in an effective manner. UVM is extended version of OVM and it also supports some features of VMM. Reusability is the key factor in UVM, this can be achieved by using call-back function, overloading of the factory mechanism and inheritance property of UVM class [12]. Dual Port RAM is considered as DUT for verification.

This paper is divided into sections as fallows: In section 2, describing the DPRAM in a simple way and the objectives of the work. Section 3, is about System Verilog verification environment and also simulation results of DPRAM in System Verilog environment. Section 4, talk about UVM verification environment of DUT and its simulation results. Section 5, conclusion of the work is discussed.

II. DUAL PORT RAM

Dual Port RAM (DPRAM) is a type of random-access memory, it permits to perform multiple write or reads takes place at the same time on both ports or it almost near. Transaction can be done synchronously or asynchronously. Both ports have separate clock, enable and control signals for the transactions. To the single memory, they have ability to access locations. Each port has address, data input, data output, enable signals and control signals. Block diagram of Dual Port RAM is shown in figure 1.

A. Objectives

1) The proposed verification environment will be implemented by using OOP concepts.
2) The functionality of the design is verified using System Verilog and UVM.
3) Generation of multiple Test Cases to analyze the design.
4) Achieve 100% Coverage and Assertions.

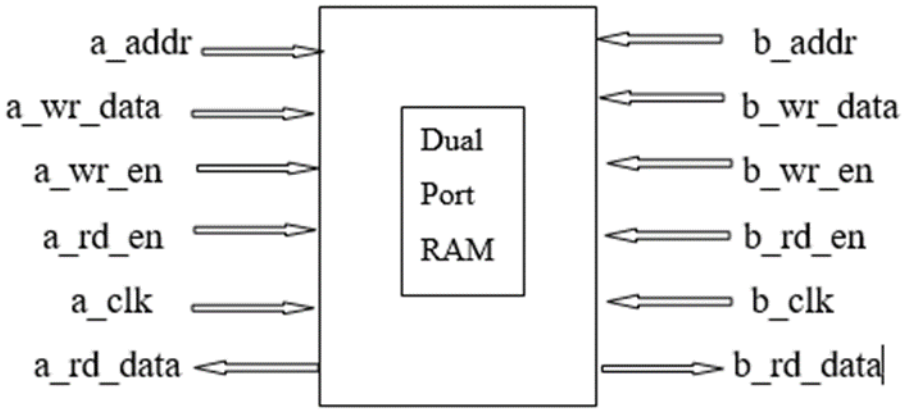

Fig.1. Block diagram of DPRAM

III. SYSTEM VERILOG ENVIRONMENT

A. System Verilog Verification Environment

System Verilog verification environment of DUT is illustrated in figure 2. We developed verification environment in such a way that to cover all the objectives.

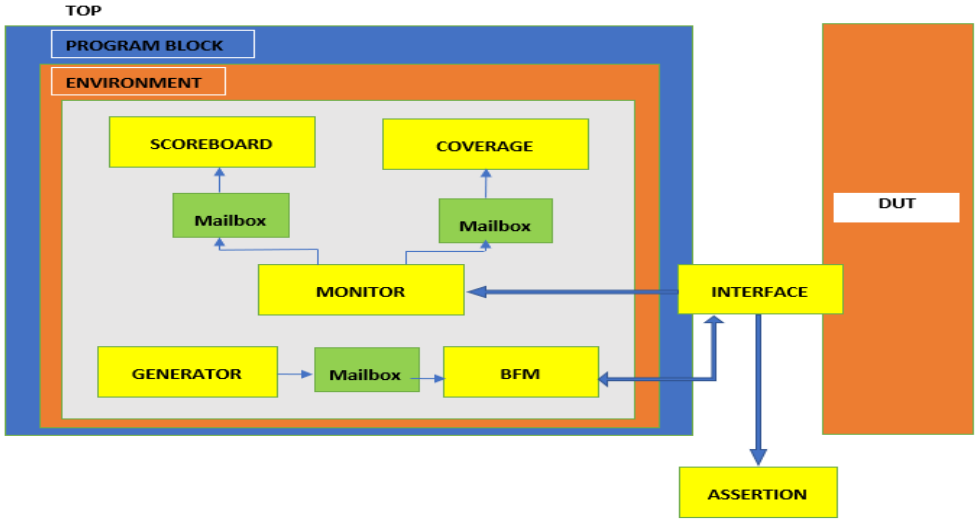

Fig.2. System Verilog verification environment.

1) Generator: Stimulus is generated randomly and these are driven by Bus Functional Model (BFM) it's nothing but a driver.
2) Functional coverage: Coverage is a measure of how much scenario\features covered. In SV coverage is achieved by using cover group, it consists of cover points and bins. Each variable is associated with bins if all the bins are covered then only, we can achieve complete coverage.
3) Assertion: Design behaviour is verified by using assertions and it can be used to check particular conditions. There are two types of assertions immediate assertion and concurrent assertion. In immediate assertion, at current simulation time only it will check for the condition. While in concurrent assertion, over multiple clock cycles it examines the sequence of conditions.

B. Testcases

We considered four testcases

1) Both ports are trying to write data to same location
2) Both ports reading data from same location
3) Mixed read and write
4) Writing data to both ports and reading data in a crossed version.

C. Simulation Results

All the testcases are verified results of Dual Port RAM of fourth testcase is shown below.

1) Transcript window results

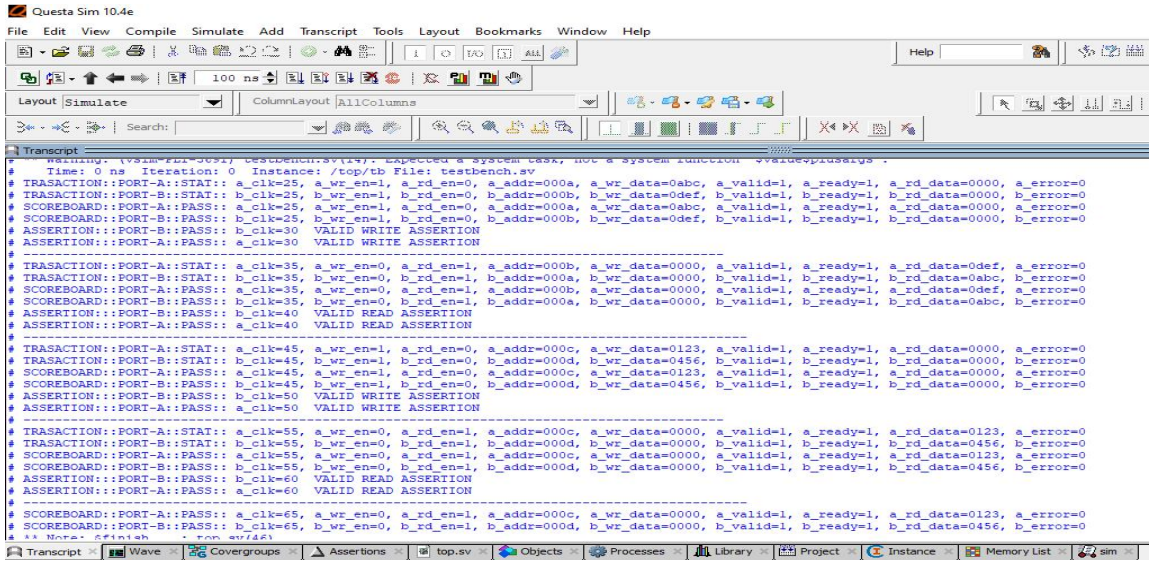

Fig.3. Transcript window results of DPRAM.

2) Waveform

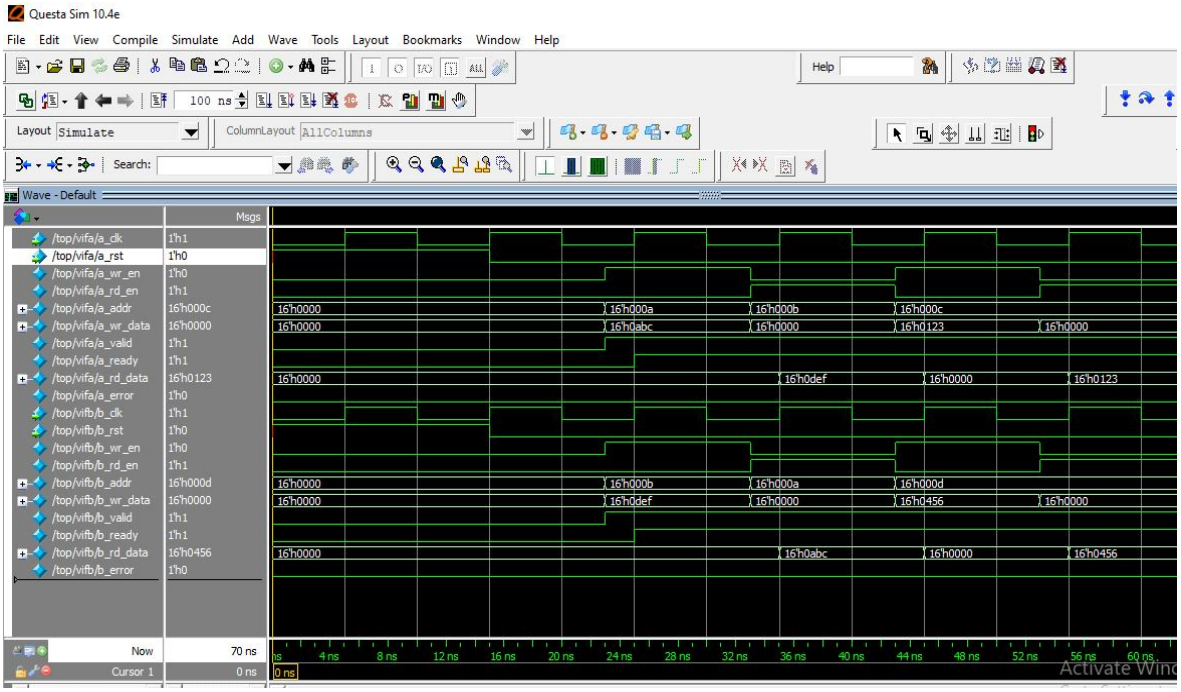

Fig.4. Waveform results.

3) Coverage output

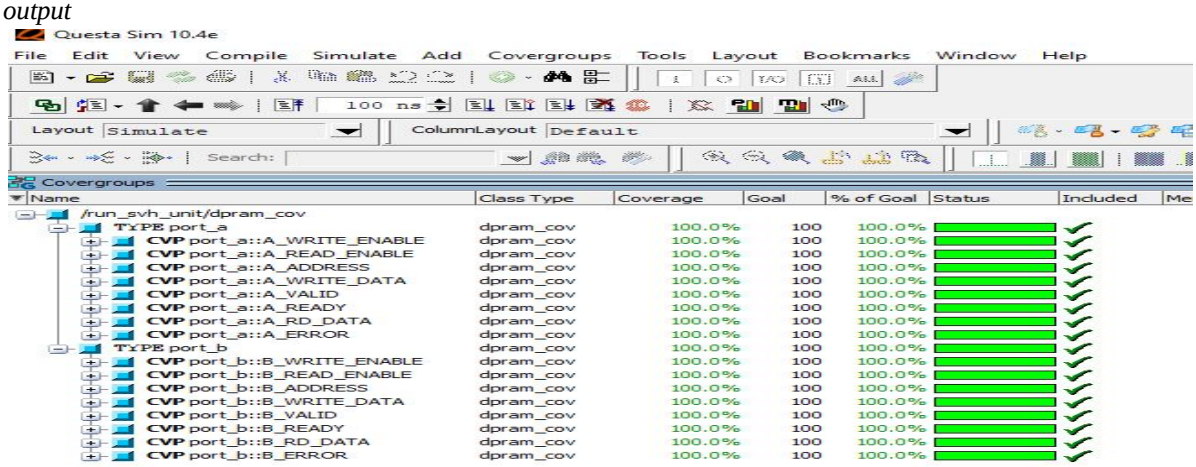

Fig.5. Results of coverage.

4) Result of total coverage and assertion

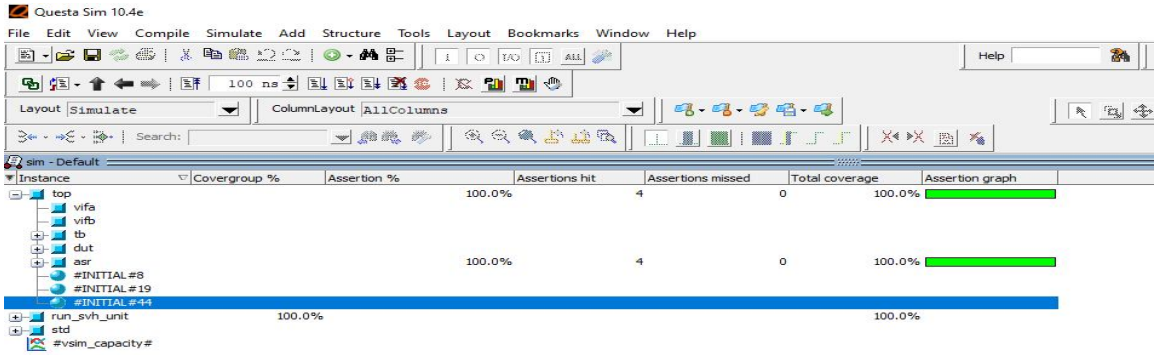

Fig.6. Total coverage and assertion result.

IV. UVM VERIFICATION ENVIRONMENT

UVM verification methodology is one of the advanced and broadly used verification methodologies. It claims reusability criteria standard which is achieved by its library classes. These classes can be inherited uvm_component, uvm_object, uvm_sequence is few of them. Verification environment is developed in such a way that to achieve complete coverage and assertion. UVM verification environment is shown in figure 7.

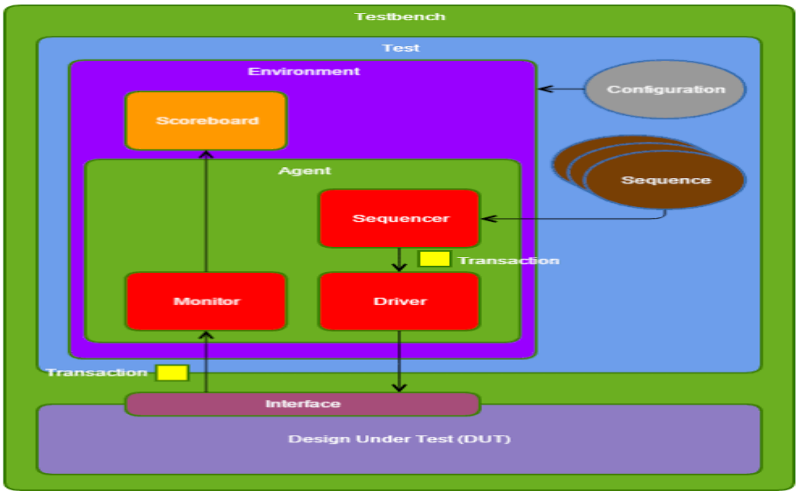

Fig.7. UVM verification environment

As stimulus is generated in the generator in SV, in UVM we have uvm_sequencer it consists of uvm_sequence_item and uvm_sequence. Agent generates the pin level activity which are defined by sequence item. These data packets are driven to\from the driver in a sequence through the routing mechanism of uvm_sequencer. TLM (Transaction Level Modeling) is meant for communication purpose; this can be done through implementing the methods which are transaction based. TLM interface class defines the methods which are defined for communication, those are put(), get(), peek(), try_put(), can_put(), try_get(), can_get(), transport(), nb_transport() and analysis.

A. Simulation Results

The results of Dual Port RAM are given below

1) Waveform results

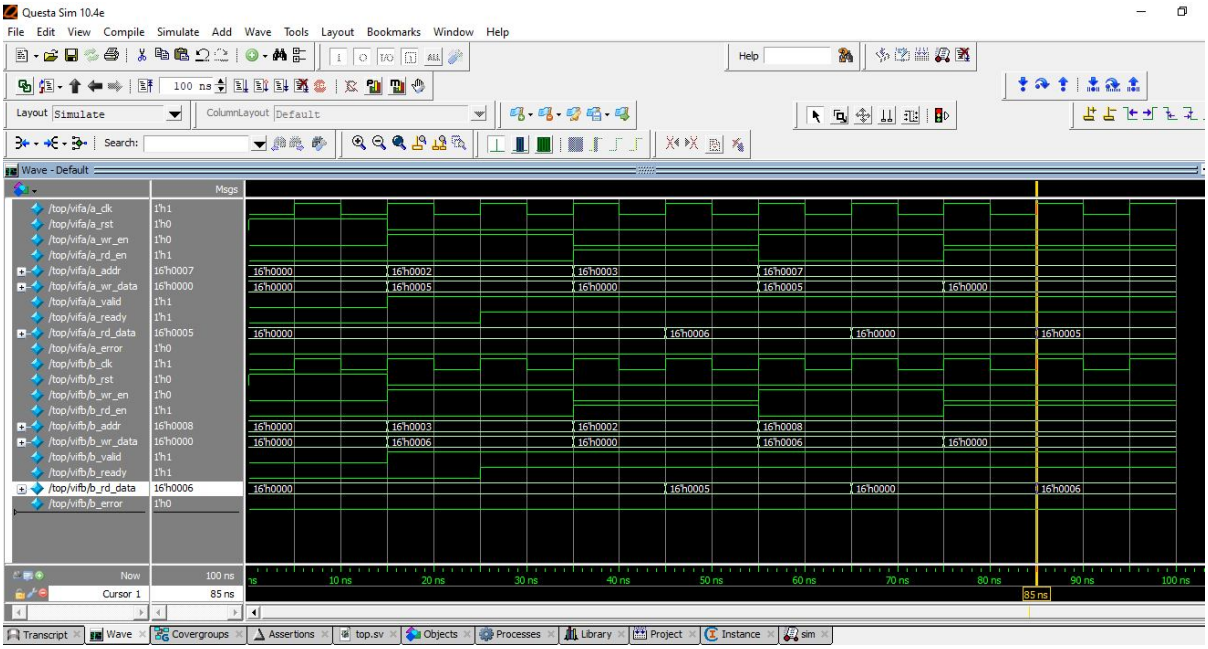

Fig.8. waveform results of DPRAM.

2) Total Coverage and Assertion Result

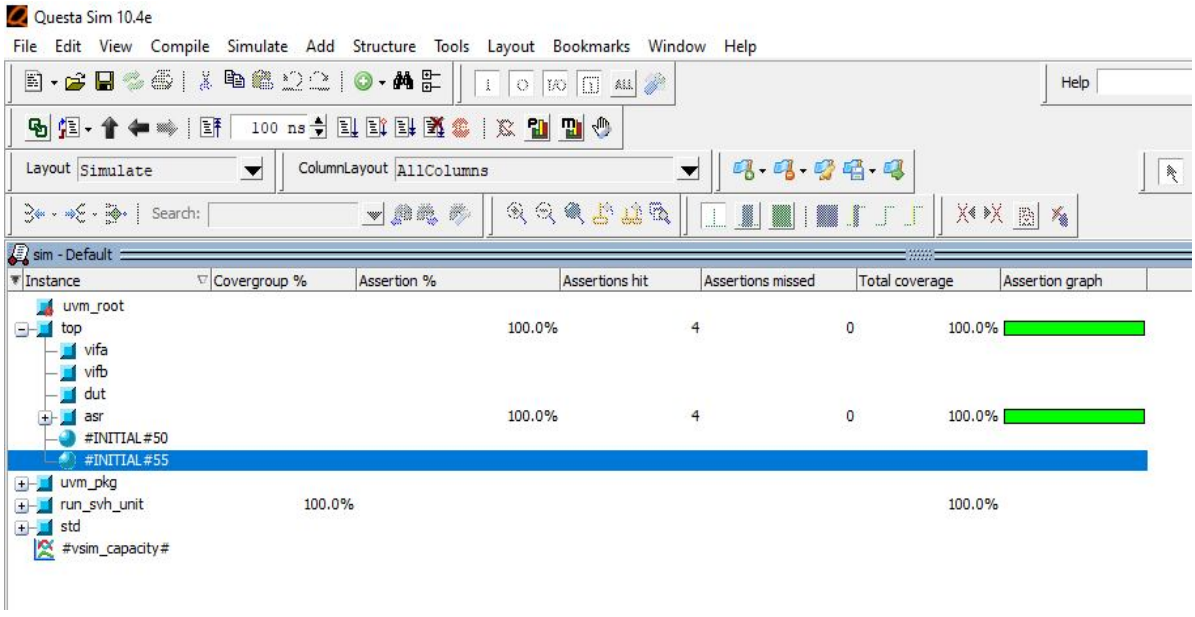

Fig.9. Result of total coverage and assertion

V. CONCLUSION

System Verilog and UVM Verification environments are developed by using OOPs concepts. Different classes are created for monitor, generator, scoreboard, driver and so on. All the testcases are tested in both the environments. Objectives are covered, from both the environments 100 % cover group coverage and 100% assertion is found for DPRAM. Therefore, the overall coverage achieved is 100% for verification of DPRAM which is considered as DUT in System Verilog and UVM verification environments.

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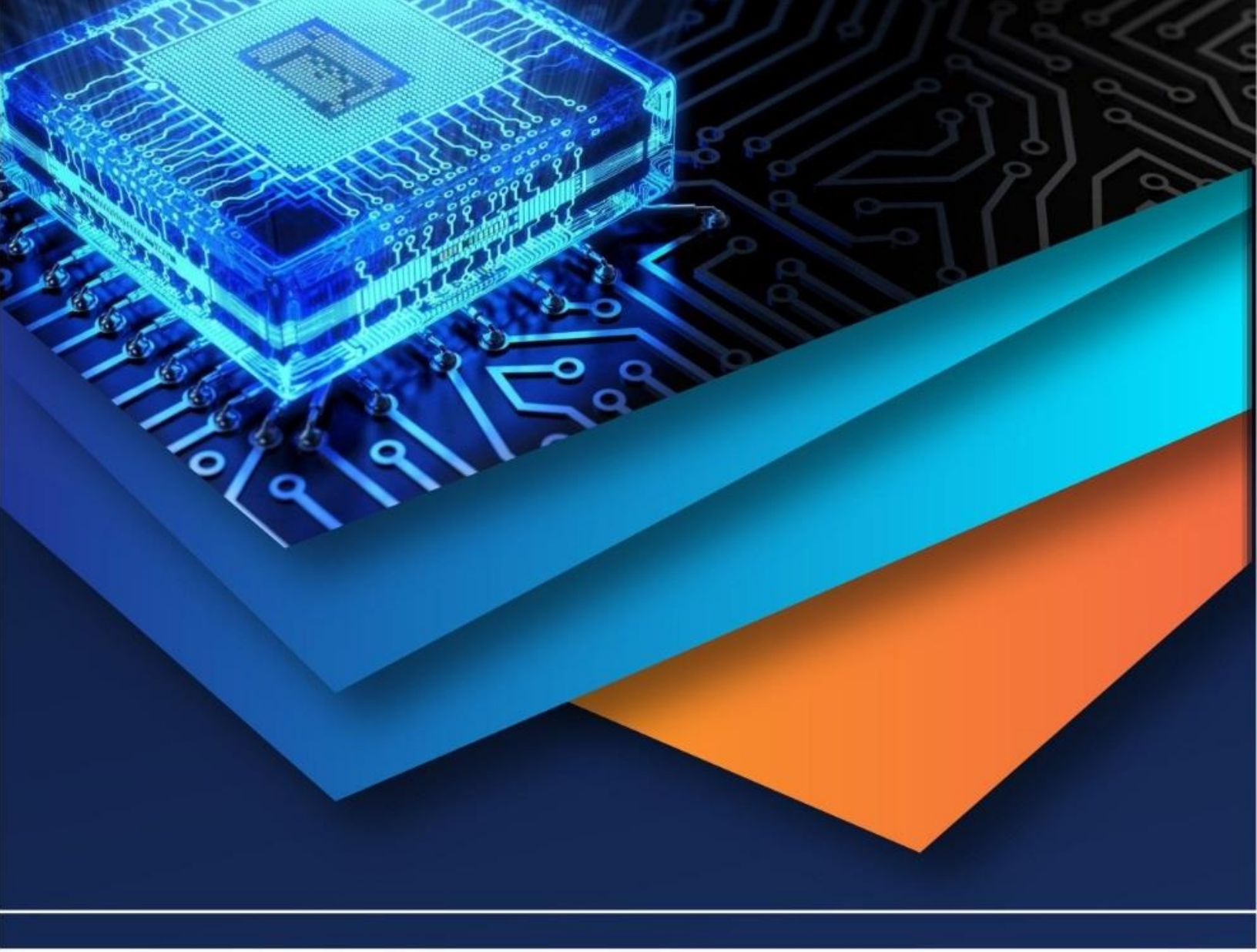

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