iJRASET
International Journal For Research in Applied Science and Engineering Technology



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 9 **Issue:** VI **Month of publication:** June 2021

DOI: https://doi.org/10.22214/ijraset.2021.36031

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 9 Issue VI June 2021- Available at www.ijraset.com

Implementation of 7-Level and 31-Level Cascaded H-Bridge Multilevel Inverters with Reduced Number of Semiconductor Switches

CH. Sajan[1], M. Navya Sri[2], Mohd Abdul Wasi[3], N. Sathish[4], K. Bhargav Prasad[5]
[1]*Assosiate Professor,* [2, 3, 4, 5] *UG Students, Department of Electrical and Electronics Engineering, Jyothishmathi Institute of Technology and Science, Nustulapur, Karimnagar, TS, India*

Abstract: ***Multilevel inverters are widely used because of its increased power rating with reduced harmonics and electromagnetic interference. The proposed 7-level cascaded H-Bridge inverter is symmetrical in nature and uses equal sources of DC voltage. Whereas 31-level cascaded H-Bridge inverter is asymmetrical in nature and uses unequal sources of DC voltage. The PD-PWM modulation technique was used here to achieve switching sequence. The proposed idea was validated through simulation and the results provide better efficiency, fewer low order harmonics and lower switching losses. The proposed topology is simulated using MATLAB / SIMULINK.***

Keywords: ***Multilevel Inverters (MLI), Cascaded H-Bridge (CHB), Pulse Width Modulation(PWM), Level Shifted PWM (LS-PWM), Phase Disposition(PD), Total Harmonic Distortion (THD).***

I. INTRODUCTION

The utilization of renewable energy sources is increasing to provide the increasing demand of electricity due to urbanization. solar energy produces dc power which must be converted into ac for further applications. Conversion of dc power to ac is completed using inverters. The cascaded H bridge multilevel inverter converts dc power to ac power with less THD. This study will help the planning engineer in selecting the acceptable multilevel inverter for required application. Multilevel inverters are classified as current source inverter and voltage source inverter. just in case of multilevel current source inverter, it had been observed that if there's short within the circuit, the fault current are going to be very high further damaging the equipment's connected within the circuit. Therefore multilevel voltage source inverters are mostly used [1].Multilevel voltage source inverters area unit classified into 3 main classes as (a)Cascaded H-Bridge(CHB) multilevel inverter, (b)Neutral point Clamped(NPC) multilevel inverter and (c) Flying Capacitor(FC) multilevel inverter.CHB MLI is usually used because it offers excessive output voltage, reliability, electricity ranges and ease of control.

II. CASCADED H-BRIDGE MULTILEVEL INVERTER

The CHB MLI are most superior and essential approach of power electronic converters that analyses output voltage with number of dc sources as inputs. As compared to NPC and FC MLI, The CHB multilevel inverters needs less number of dc sources and it reaches high-quality of output voltage that is almost identical to sine wave. By increasing the output levels the THD in output voltage are often reduced. In CHB MLI the needed AC output voltage obtain by arranging the number of DC supply. The number of H-Bridges were connected in cascade to supply CHB MLI [2].

III. PROPOSED TOPOLOGY FOR 7-LEVEL INVERTER

The advantage of the proposed system for 7-level is to reduce number of semiconductor switches on comparing to the conventional seven-level CHB MLI. The conventional topology uses twelve switches and 3 DC sources. In the proposed system, the semiconductor switches are reduced to six. Figureure.1 shows the proposed system for 7-level CHB MLI. Switches S1, S2, S3 and S4 within the full bridge works in bi-directional operation whereas switches S5 and S6 are accustomed to control the input voltage so as to get the required output voltage level in unidirectional operation. The switching sequence for the proposed topology is as shown in Table.1.

©IJRASET: All Rights are Reserved

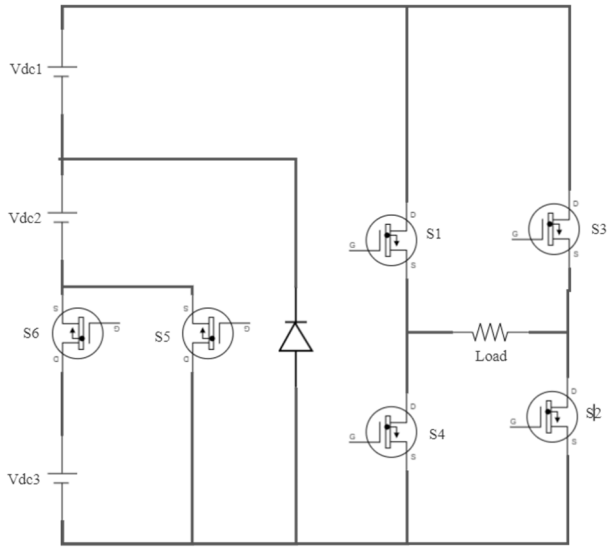


Figure 1. Proposed topology of a 7 level MLI

Vo	S1	S2	S3	S4	S5	S6
3vdc	1	1	0	0	0	1
2vdc	1	1	0	0	1	0
1vdc	1	1	0	0	0	0
0	1	1	1	1	0	0
-1vdc	0	0	1	1	0	0
-2vdc	0	0	1	1	1	0
-3vdc	0	0	1	1	0	1

Table 1.Switching Sequence for 7-level Inverter

IV. PROPOSED TOPOLOGY FOR 31-LEVEL INVERTER

Thirty one level asymmetrical MLI consists of 1 cell of H-bridge with four main switches, four auxiliary switches and 4 diodes. It is having four separate DC sources for thirty one level MLI. For H-bridge having four switches S5, S6, S7 and S8 within which one combine of switches operate for positive half cycle i.e. switch S5 and S6 and different combine of switch operating for negative half cycle i.e switch S7 and S8 with four separate dc sources Vdc, 2Vdc, 4Vdc and 8Vdc. The circuit diagram for proposed 31-level inverter is shown in Figureure.2. There are thirty-one modes of operation for this topology so as to come up with thirty one level output. The switching states of 31-level CHB MLI are shown in Table.2.

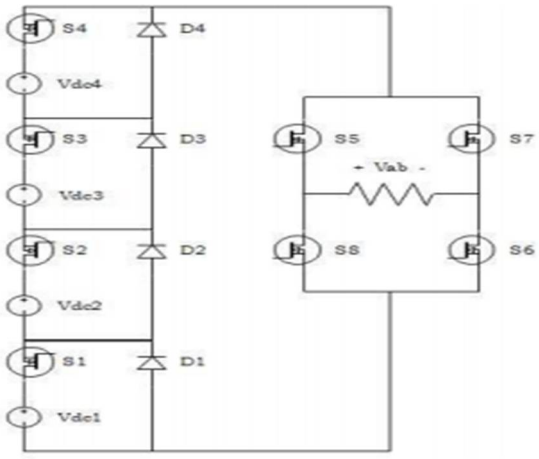


Figure 2. Proposed topology of a 31 level MLI

©IJRASET: All Rights are Reserved

Table 2. Switching Sequence of proposed 31-level MLI

Vo	G1	G2	G3	G4	G5	G6	G7	G8
15Vc	1	1	1	1	1	1	0	0
14Vdc	0	1	1	1	1	1	0	0
13Vdc	1	0	1	1	1	1	0	0
12Vdc	0	0	1	1	1	1	0	0
11Vdc	1	1	0	1	1	1	0	0
10Vdc	0	1	0	1	1	1	0	0
9Vdc	1	0	0	1	1	1	0	0
8Vdc	0	0	0	1	1	1	0	0
7Vdc	1	1	1	0	1	1	0	0
6Vdc	0	1	1	0	1	1	0	0
5Vdc	1	0	1	0	1	1	0	0
4Vdc	0	0	1	0	1	1	0	0
3Vdc	1	1	0	0	1	1	0	0
2Vdc	0	1	0	0	1	1	0	0
Vdc	1	0	0	0	1	1	0	0
0	0	0	0	0	1	1	1	1
-Vdc	1	0	0	0	0	0	1	1
-2Vdc	0	1	0	0	0	0	1	1
-3Vdc	1	1	0	0	0	0	1	1
-4Vdc	0	0	1	0	0	0	1	1
-5Vdc	1	0	1	0	0	0	1	1
-6Vdc	0	1	1	0	0	0	1	1
-7Vdc	1	1	1	0	0	0	1	1
-8Vdc	0	0	0	1	0	0	1	1
-9Vdc	1	0	0	1	0	0	1	1
-10Vdc	0	1	0	1	0	0	1	1
-11Vdc	1	1	0	1	0	0	1	1
-12Vdc	0	0	1	1	0	0	1	1
-13Vdc	1	0	1	1	0	0	1	1
-14Vdc	0	1	1	1	0	0	1	1
-15Vdc	1	1	1	1	0	0	1	1

V. MODULATION TECHNIQUES

A. Multicarrier PWM (MCPWM) Techniques

To control and to come up with prime quality output waveform of multilevel converter, appropriate modulation schemes are needed. Various modulation techniques are shown in Figure. 3. Among these modulation techniques, a vital family of modulation technique, MCPWM stands out as a result of it offers simplicity and straightforward to implement switching waveforms.

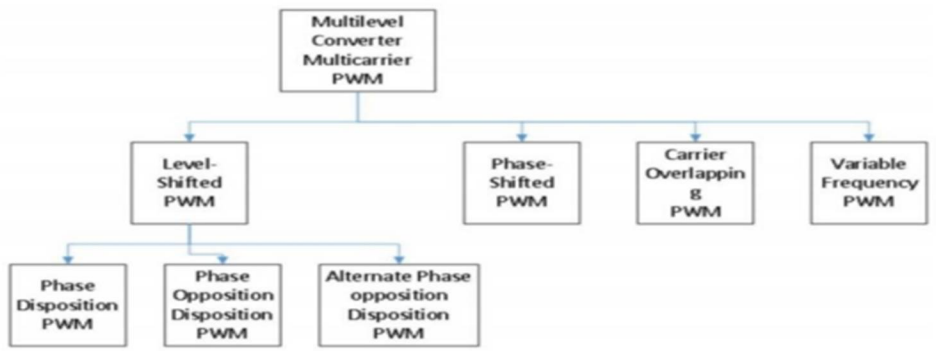


Figure 3. Various modulation techniques

©IJRASET: All Rights are Reserved

B. Level Shifted PWM (LS-PWM)

In the LS-PWM strategies all the carrier signals use triangular wave, cover the entire extent range of generated inverter output voltage with same amplitude and frequency [4]. They're classified primarily based on the position of various carrier signals. For generation of n level, n-1 carrier signals ar needed. The LS-PWM strategies ar utilized in the dominant of inverters wherever power balancing isn't needed. The classification of level shifted PWM techniques ar as follows:

C. Phase Disposition (PD) PWM

In Phase Disposition (PD) PWM, the required number of carrier waveforms are (m-1) for waveforms of m level. All the carriers are in same phase and to get the output voltage, these are compared with the reference waveforms. PWM output is high if the carrier wave is below the reference signal and contrariwise [6].

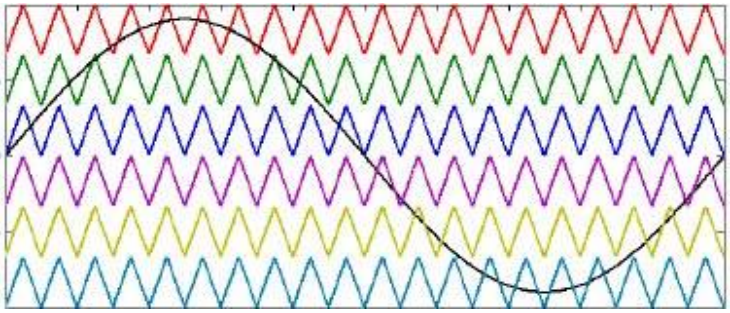


Figure 4. Phase Disposition(PD) PWM

D. Phase Opposition Disposition (POD) PWM

In phase Opposition Disposition(POD) PWM, the above zero reference carrier waveforms have equal phase and below the zero reference carrier waveforms are phase shifted by 180 degrees. At the carrier frequency, the harmonics that are terribly dominant are placed [7, 8].

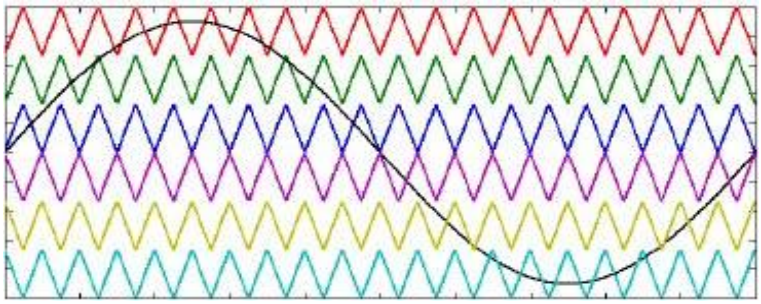


Figure 5. Phase Opposition Disposition PWM

E. Alternate Phase Opposition Disposition (APOD) PWM

In Alternate phase Opposition Disposition (APOD) PWM, the required numbers of carrier waveforms are (m-1) for waveforms of m level and with the adjacent carrier wave, all carrier waves are out of the phase by 180 degrees [8]. There's no harmonics encountered at the carrier frequency and round the carrier frequency, harmonics that are terribly dominant are treated as sidebands.

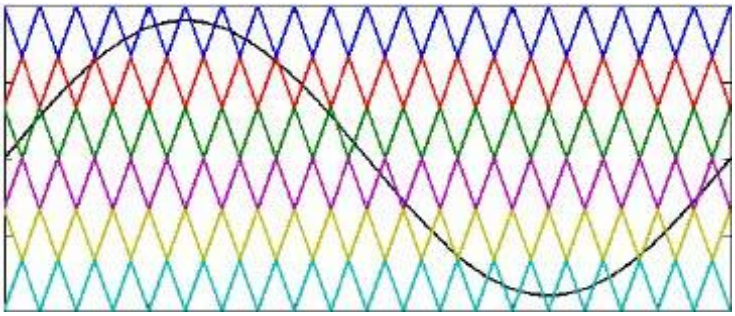


Figure 6. Alternate Phase Opposition Disposition PWM

©IJRASET: All Rights are Reserved

VI. SIMULATION & RESULTS

A. Simulation of 7-level CHB MLI

Three dc sources and 6 semiconductor switches (IGBTs) are chosen for simulating of CHB MLI which is seven levels and it's applied in Level shift PDPWM technique. The simulation of 7-level CHB MLI is shown in Figure. 7(a). According to the switching sequence, staircase output of 7-levels is obtained. The time values were set for the carrier signals and in keeping with the carrier disposition, output were values were set. The waveforms regarding output voltage, Current and PDPWM waveforms are given in Figure 7(b) and corresponding THD is observed by FFT analyzer is shown in Figure. 7(c).

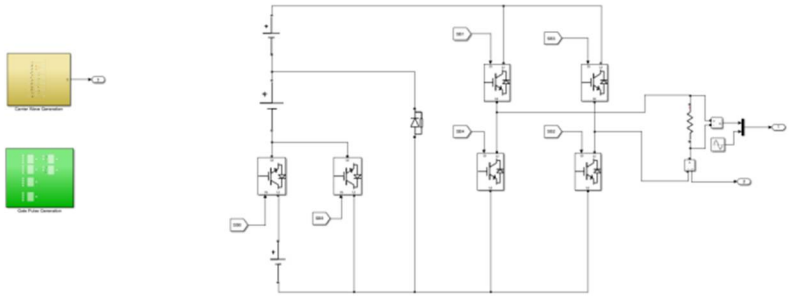


Figure 7(a). Simulation of single phase seven level cascaded H-bridge MLI

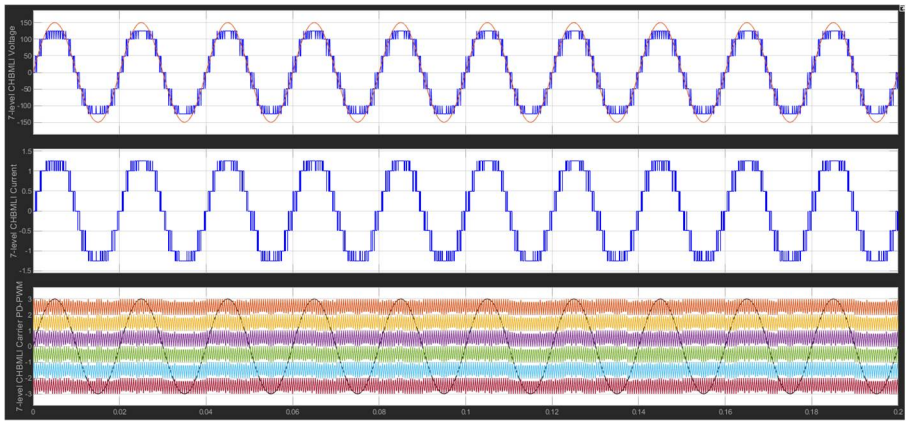


Figure 7(b). Output voltage, current and PDPWM waveforms of seven level cascaded H-bridge MLI.

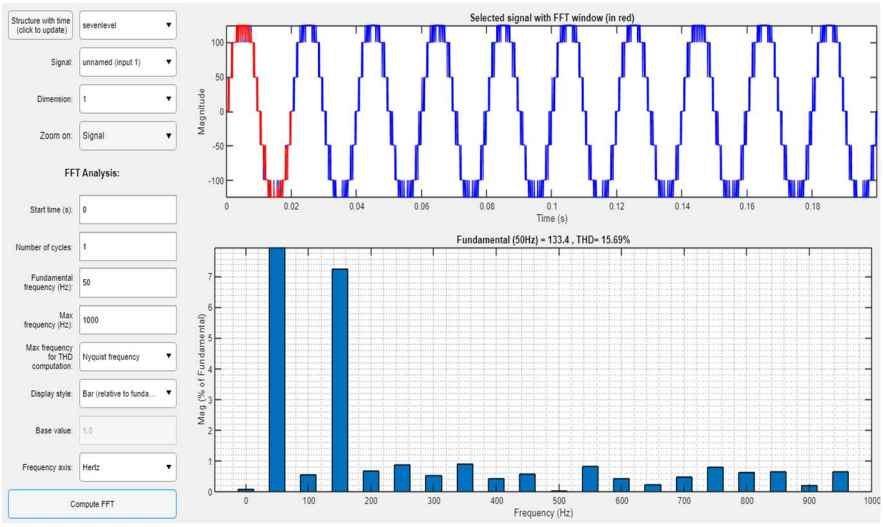


Figure 7(c). FFT analysis of seven level cascaded H-bridge MLI

©IJRASET: All Rights are Reserved

B. Simulation of Thirty-One Level CHB MLI

Four separate dc sources with diodes and semiconductor switches (IGBTs) and 4 main semiconductor switches (IGBTs) ar chosen for simulating of CHB MLI that is 31 levels and it's distributed in Level shift PDPWM technique. The simulation of 31-level CHB MLI is depicted in Figure. 8(a).According to the switching characteristics, staircase output of 31 levels is obtained. The time values were set for the carriers and consistent with the carrier disposition, output values were set. The waveforms relating to output voltage, Current and PDPWM waveforms are given in Figure 8(b) and corresponding THD is observed by FFT analyzer that is given in Figure.8(c).

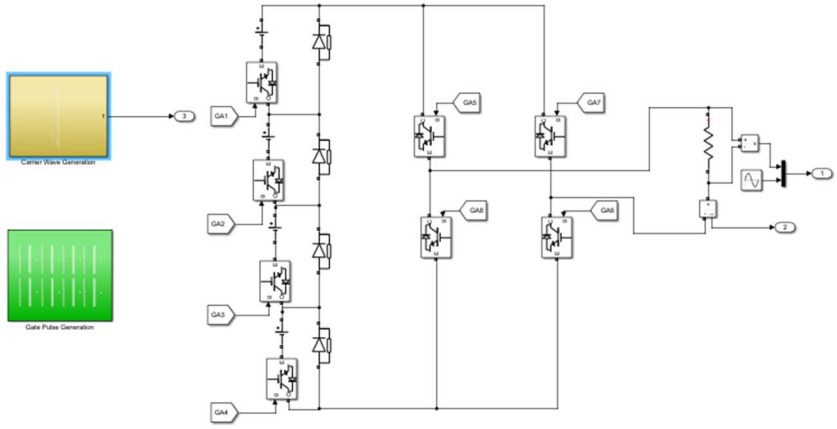


Figure 8(a). Simulation of single phase Thirty One level cascaded H-bridge MLI

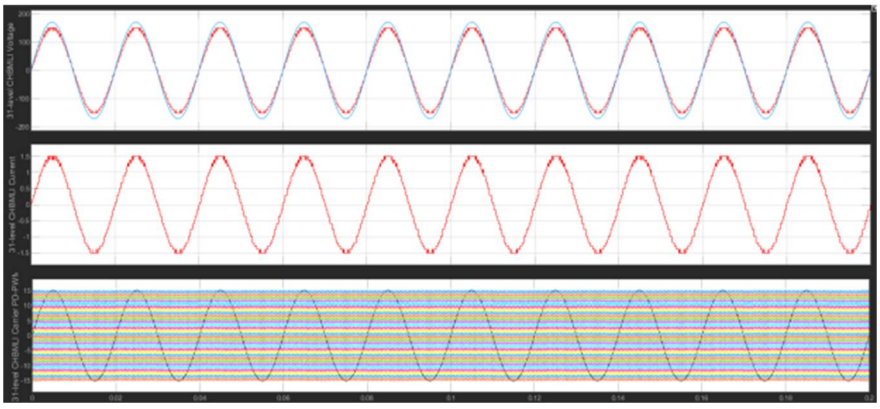


Figure 8(b). Output voltage, current and PD PWM waveforms of Thirty-one level cascaded H-bridge MLI

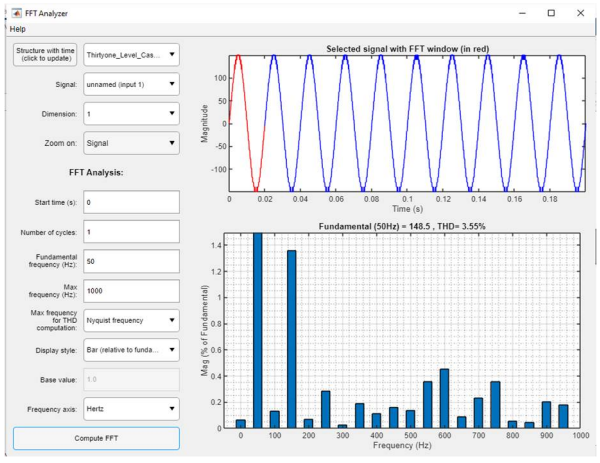


Figure8(c). FFT analysis of Thirty-one level CHB MLI

©IJRASET: All Rights are Reserved

Table 3. Analysis of Cascaded H-bridge MLI for 7 & 31 levels

Multilevel Inverter	No. of Semiconductor switches	THD%
7-level CHB MLI	6	15.69
31-level CHB MLI	8	3.55

The implementation can be done for 15-levels and 21-levels where the number of semiconductor switches are 7 and 8 respectively

VII. CONCLUSION

The CHB MLI for 7 and 31 level multilevel inverter with minimized number of semiconductor switches for multicarrier PWM technique i.e Phase Disposition PWM (PDPWM) has been implemented. CHB MLI are used extensively due to their high quality output voltage waveforms in comparison with Neutral Point Clamped and Flying Capacitor MLI methods. DC voltage sources are associated in series arrangement. This paper gives THD Of 15.69% for 7-level CHB MLI and 3.55% for 31-level CHB MLI and therefore the AC output waveform nearly looks like a sine wave for 31-level. The proposed inverters are used in integration of Renewable Energy Sources, FACTS, Hybrid Electric Vehicles, Power Quality improvements. The Simulation results are shown in Figure 7(b), Figure 8(b).

REFERENCES

[1] EbrahimBabaei, Member, IEEE, Sara Laali, Student Member , IEEE, and Zahra Bayat "A single phase cascaded multilevel inverter based on a new basic unit with reduced number of power swithes. "

[2] MariuszMalinowaski, Senior Member, IEEE, K.Gopakumar, Senior Member, IEEE, Jose Rodriguez, Senior Member, IEEE, and Marcelo A.Perez, Member IEEE "A Survey on Cascaded Multilevel Inverters".

[3] M. A. Chulan and A. H. M. Yatim, "Design and implementation of a new H-bridge multilevel inverter for 7-level symmetric with less number of switches," in Power and Energy (PECon), 2014 IEEE International Conference on, pp. 348-353, 2014

[4] D.Mohan Sreejith B.Kurub ,A Comparative Analysis of Multi Carrier SPWM Control Strategies using Fifteen Level Cascaded H – bridge Multilevel Inverter International Journal of Computer Applications (0975 – 8887) Volume 41– No.21, March 2012

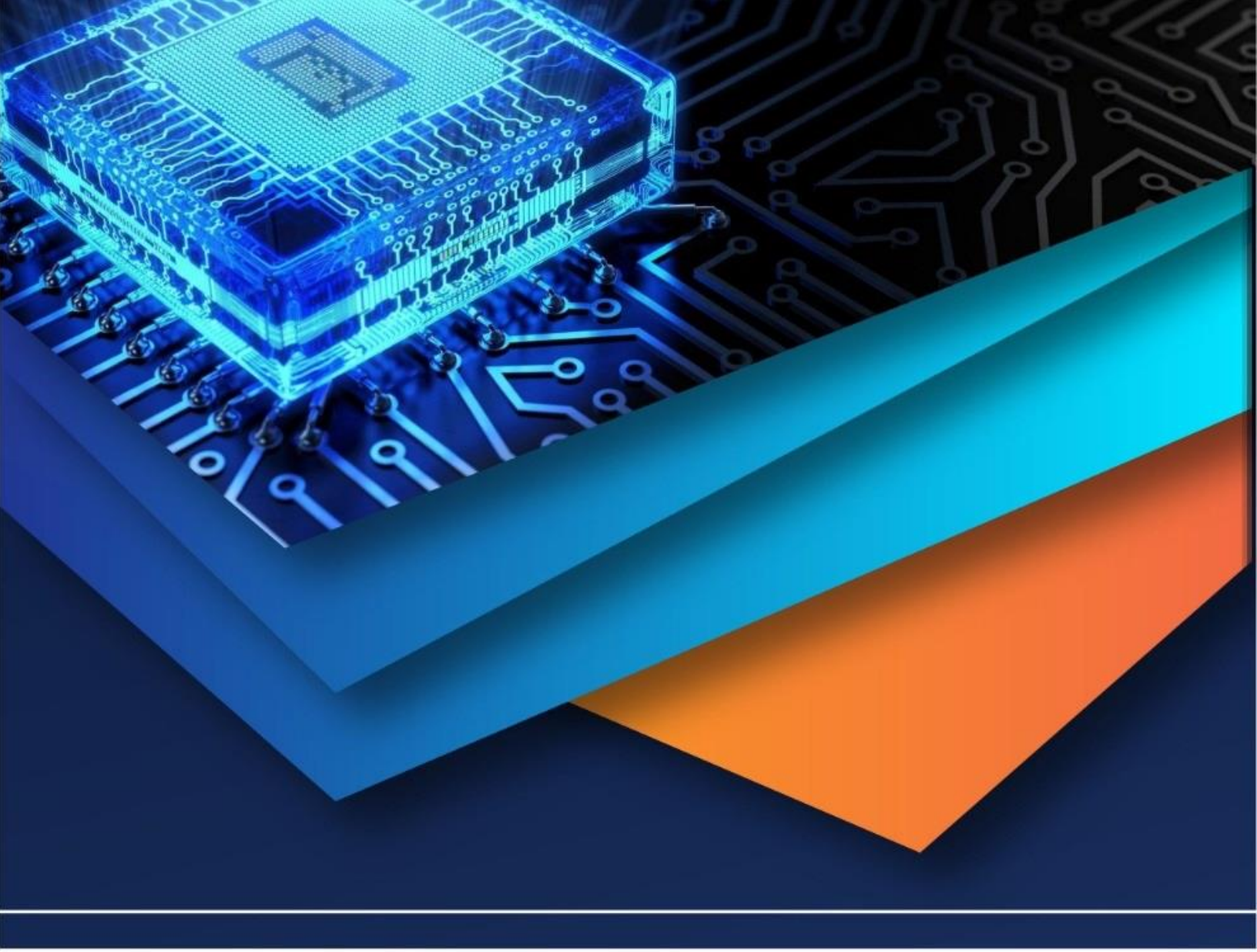
[5] S. Umashankar, T. S. Sreedevi, V. G. Nithya, and D. Vijayakumar , A New 7-Level Symmetric Multilevel Inverter with Minimum Number of Switches , Hindawi Publishing Corporation ISRN Electronics Volume 2013

[6] M. M. Harin, V. Vanitha, and M. Jayakumar, "Comparison of PWM Techniques for a three level Modular Multilevel Inverter," Energy Procedia, vol. 117, pp. 666-673, 2017.

[7] A. António-Ferreira, C. Collados-Rodríguez, and O. Gomis-Bellmunt, "Modulation techniques applied to medium voltage modular multilevel converters for renewable energy integration: A review," Electric Power Systems Research, vol. 155, pp. 21-39, 2018.

[8] W. Subsingha, "A Comparative Study of Sinusoidal PWM and Third Harmonic Injected PWM Reference Signal on Five Level Diode Clamp Inverter," EnergyProcedia, vol. 89, pp. 137-148, 2016.

©IJRASET: All Rights are Reserved



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Call : 08813907089 (24*7 Support on Whatsapp)