iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 3 **Issue:** XII **Month of publication:** December 2015

DOI:

www.ijraset.com

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Volume 3 Issue XII, December 2015
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Design Techniques For Low Power Implicit Pulse Triggered Circuits

Smt.A.Rajani[1], A.Yamini[2]
[1]Assistant Professor, [2]PG student, Department of ECE
University college of Engineering, Kakinada, A.P

Abstract - In Integrated circuits, the portion of the on chip power is covered by clock distribution network, flip-flops and latches. Flip flops and latches absorb large amount of power due to redundant transitions and clocking system. In this paper low power flip-flops are presented. The single edge triggered conditional data mapping flip-flop(CDMFF) and clocked pair shared flip-flop(CPSFF) are explained and compared with proposed flip-flop. The proposed flip-flop uses the double edge triggering technique by reducing the frequency to half. These flip-flops are simulated in HSPICE of 0.18µm CMOS technology with a power supply of 1.8V and a frequency of 50MHZ.
Keywords : Power; Flip-flops; CMOS circuit; CDMFF; CPSFF.

I. INTRODUCTION

In a synchronous digital system, the clock signal is used to specify a time reference for the movement of data within that system. Flip-flops are the primitive storage elements used in all types of digital circuit designs. The clock system, consists of the clock distribution network and sequential elements are one of the power consuming components in a VLSI system. It score for 30% to 60% of the total power dissipation in a system. As a result, reducing the power utilized by flip-flops will have a deep crush on the total power consumed. Conventional master slave flip flops are built up of two stages and are characterized by hard edge property. But pulse triggered flip flops lower the two stages into one stage and are characterized by soft edge property. Now a days pulse triggered flip flops have been expressed as an substitute to the conventional master-slave. Pulse triggered flip-flops can be distinguish into two types, implicit-pulsed and explicit-pulsed flip-flops. Caution must be paid to decrease the clock load when designing a clocking system. This paper is presented as follows: section II consists of techniques used in the flip-flops. Section III discusses the working of existing flip-flops succeed by proposed flip-flop in section. Section V presents the simulation results followed by conclusion in section VI.

II. TECHNIQUES USED IN FLIP-FLOPS

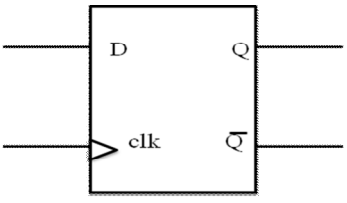
Power utilization in the conventional CMOS digital circuit can be classified into three types (i) Static power (ii) Dynamic power and (iii) Leakage power . Although the static power has an significant part of total power, the dynamic power is also powerful in the total consumption. The dynamic power is calculated using the equation

$$P_d = C_{eff} V^2 f \qquad (1)$$

where *f* the frequency *C* the capacitance and *V* the supply voltage.

A. Single Edge Triggering

The output of D flip-flop depends on the state of the D input at the moment of a positive edge at the clock pin (or negative edge if the clock input is low).



Volume 3 Issue XII, December 2015
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Figure 1: Single edge triggered flip-flop

The advantage of the D flip-flop is that the signal on the D input pin is taken at the moment, the flip-flop is clocked and subsequent changes on the input will be ignored until the next clock event.

B. Double Edge Triggering

Both positive and negative edges are used to sample the D input at different clock edges, and the appropriate sample is selected for the Q output by a clocked multiplexer (MUX). The double edge triggering uses only half of the frequency of single edge triggering with same data throughput.

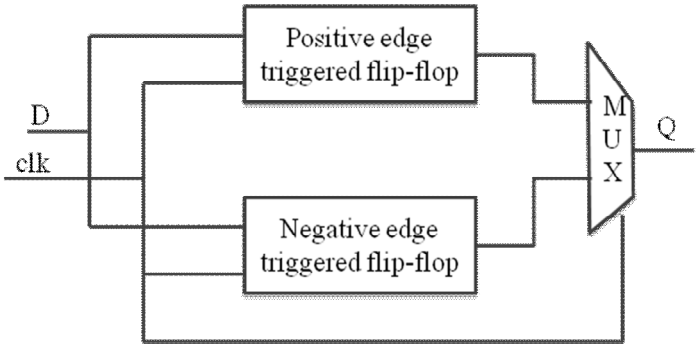

Figure 2: Double edge triggered flip-flop

As the frequency decreases, simultaneously power also

decreases.

C. Implicit Pulse Flip-Flops

In implicit type flip-flop, the pulse generator is a built in logic & there is no need for an external circuitry. Implicit flip-flop consists of 2 parts. a)clock distribution network b)latch for storage.

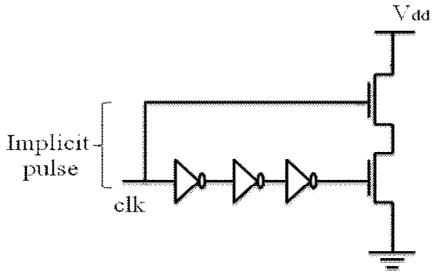

Figure 3: Implicit pulse flip-flop

It is more power efficient as pulses are produced internal to the circuit.

D. Reducing Clock Load Capacity

The clock load is reduced by minimizing the number of clocked transistors and the clock transistors consumes 100% switching activity. So, it necessary to reduce the power consumption consumed by clocked transistors.

III. WORKING OF EXISTING TECHNIQUES CDMFF AND CPSFF

A. Conditional Data Mapping Flipflop(CDMFF)

Conditional data mapping technique is employed in the circuit to map the inputs to outputs as control signals. Conditional data mapping flip-flop (CDMFF) has only seven clocked transistors. Redundant clocking capacitance occurs in CDMFF.

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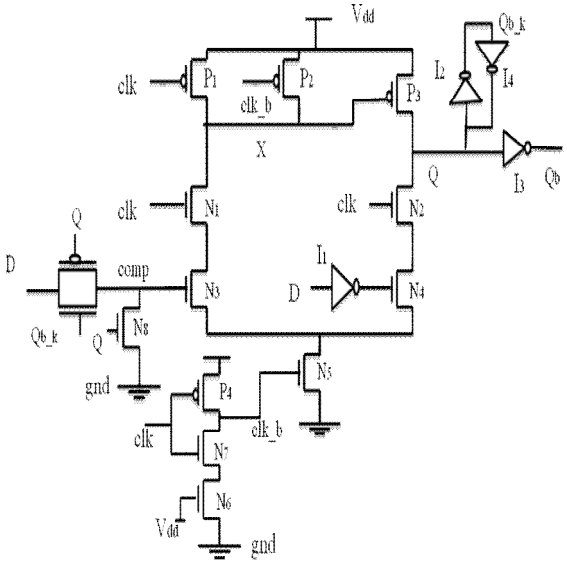

Figure 4 : Conditional data mapping flip-flop

Initially when clk is low, node X is precharged to high. This circuit operates when clk and clk_b are high and it is evaluation period. Assume the previous state outputs for Q = 0, Q_{b_k} = 1 and D = 1, so that the node X is discharged to gnd through N_1, N_3 and N_5 and make P_3 ON pulling the output Q=1. The output remains high during evaluation period and also for clk = 0 and D = 0, since all pull up and pull down paths are deactivated. When the flip-flop goes to evaluation period, and D = 0, the output Q is pulled down to 0 through N_2, N_4, and N_5. When the flip-flop goes to evaluation period and the D input is low, the node X is not connected to V_{dd} or gnd. So, the floating node exists. If a nearby noise occurs, discharges the node X as PMOS transistor P_3 will be ON and a glitch will appear on output node Q.

B. Clocked Pair Shared Flip-Flop (CPSFF)

Clocked pair shared flip-flop reduces the number the clocked transistors but eliminating the two PMOS precharge transistors with a single PMOS transistor which is always ON.

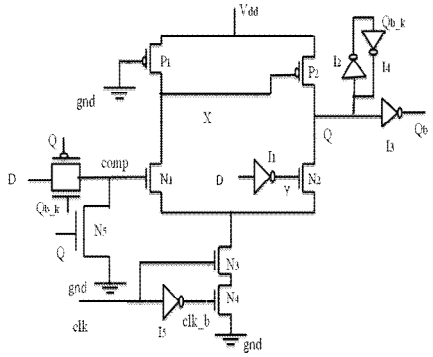

Figure 5: Clocked pair shared flip-flop

When clk and clk_b are at logic 1, circuit operates. Assume the previous state outputs for Q = 0, Q_{b_k} = 1 and D = 1, N_5 OFF and N_1 is ON. The gnd voltage will pass through N_3, N_4 and N_1 by making P_2 ON pulling the output Q =1. When Q = 1, Q_{b_k} = 0 and D = 0, N_5 ON and N_1 is OFF, then Q = 0 through N_2, N_3 and N_4. This flip-flop depends on previous output Q and Q_{b_k} in addition with clk and data input. When D = 1, N_5 is idle. When D = 0, transmission gate is idle. In high frequency operation the transmission gate and N_5 will acquire incorrect initial conditions due to feedback of input.

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IV. PROPOSED TECHNIQUE

A. *Implicit Pulse Dual Edge Triggered Flip-Flop*

In this, clock branch sharing scheme (N1, N3) (N2, N4) are joint by the first stage and second stage. A split path (node X does not drive NMOS N6 of the second stage, which is used in the output discharging path) is used to ensure the correct functioning after merging. The advantage of this sharing is reflected in reducing the number of transistors required to implement the clocking branch. Before the circuit goes to evaluation period, node X precharges to high, as the PMOS is connected to gnd. During evaluation period assuming the previous state outputs Q = 0, Q_{b_k} = 1 and D = 1, N_1, N_3 are ON. Node X discharges to gnd through N_7, N_5, N_3, N_1. So, X goes to low and P_2 is ON the outputs are Q = 1 ,Q_{b_k} = 0.

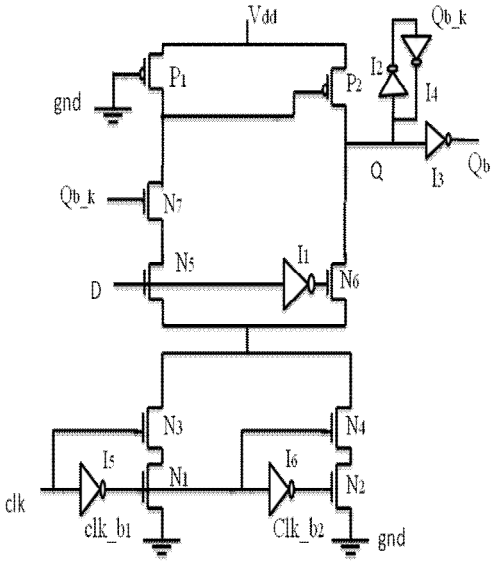
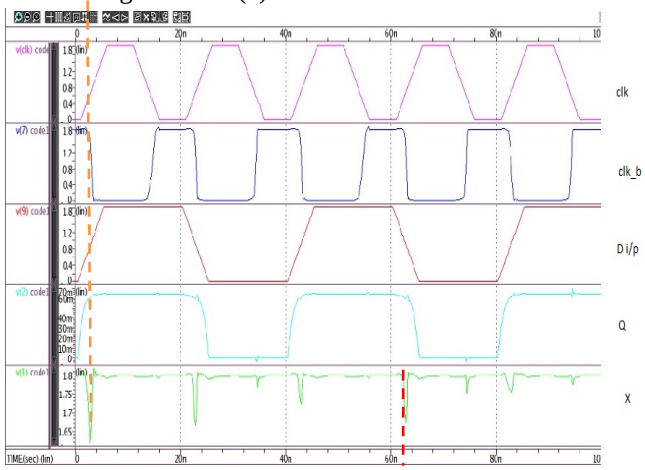


Figure 6: Double edge triggered flip-flop

Again when the circuit goes to evaluation period, Q = 1, Q_{b_k} = 0 and D = 0, N_2, N_4 are ON. The output Q is pulled down to 0 i.e Q = 0, Q_{b_k} = 1. An inverter is placed after Q, providing protection from direct noise coupling.

V. SIMULATION RESULTS

The simulation results were performed with a voltage of 1.8v and frequency of 50MHZ. For the simulation results, X-axis is time period in nano seconds (ns) and Y-axis is voltage in volts (v).



clk is high & data is high Q is high

Node X is floating

Figure 7 : Waveforms of CDMFF

Volume 3 Issue XII, December 2015
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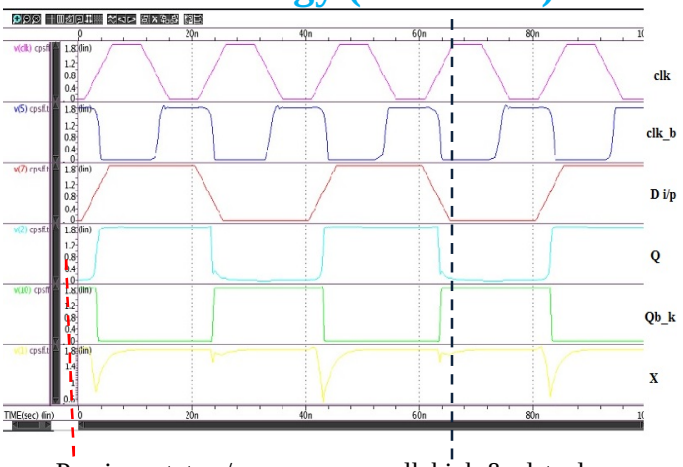

Figure 8 : Waveforms of CPSFF

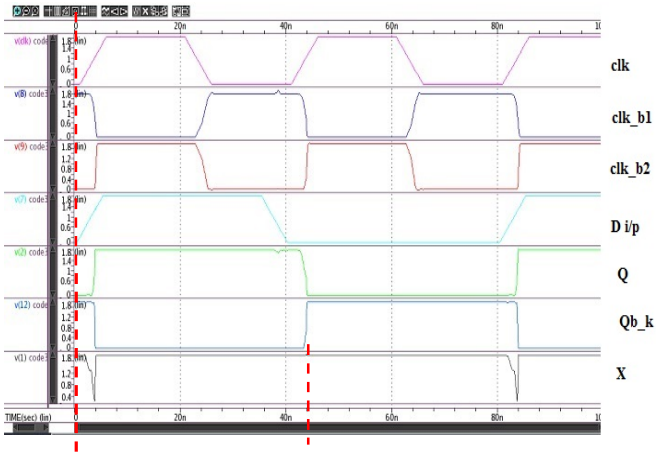

Figure 9 : Waveforms of Double edge triggered flip-flop.

Table 1: Comparison in terms of power

Power (uW)	100MHZ	50MHZ	25MHZ
CDMFF	202.4125	136.1937	128.8094
CPSFF	176.3897	127.9494	117.7126
DET	158.4481	106.4735	102.3993

In this bar diagram, X-axis is frequency in mega hertz (MHZ) and Y-axis is power in micro watts (uW).

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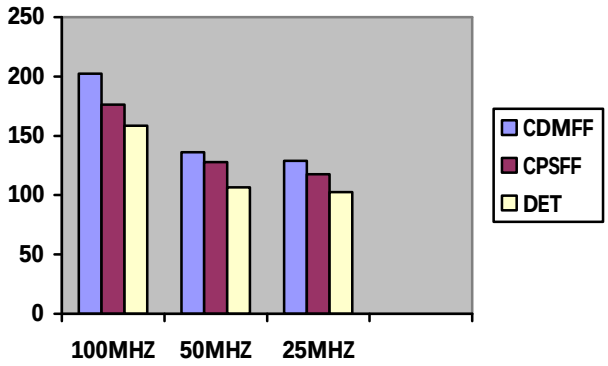

Figure 10 : Power analysis of flip-flops at different frequencies

From the above comparison, the power decreases as the frequency decreases.

Table 2: Comparison in terms of delay (TPD)

TPD (pS)	100MHZ	50MHZ	25MHZ
CDMFF	223.0081	985.5619	1557.4208
CPSFF	53.6805	167.5739	972.8790
DET	35.8686	133.5619	497.1721

In below bar diagram, X-axis is frequency in mega hertz (MHZ) and Y-axis is delay in Pico seconds (pS)

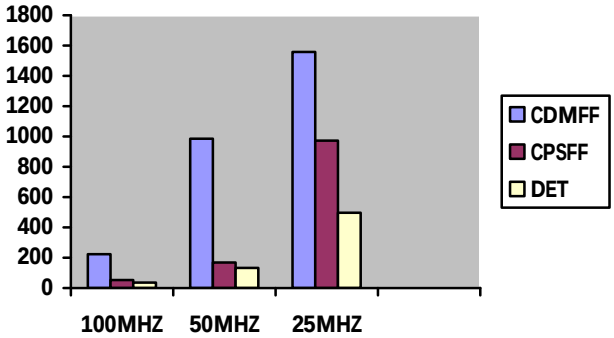

Figure 11: Delay analysis of flip-flops at different frequencies

It is observed that, as the frequency decreases, the delay increases.

Table 3: Comparison in terms of power delay product (PDP)

PDP (fJ)	100MHZ	50MHZ	25MHZ
CDMFF	67.7117	737.534	1164.5675
CPSFF	57.7799	209.3834	631.8902
DET	34.8762	77.5325	115.87653

Volume 3 Issue XII, December 2015
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In the below bar diagram, X-axis is frequency in mega hertz (MHZ) and Y-axis is power delay product in femto Joules(pJ)

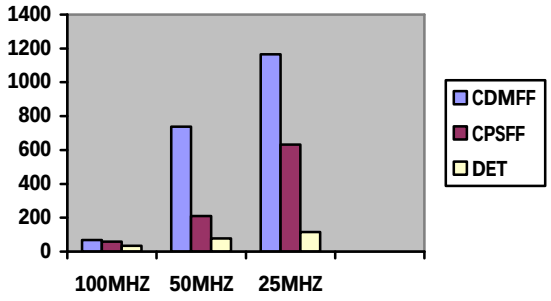

Figure 12 : Power delay product analysis of flip-flops at different frequencies.

As the frequency decreases, the power delay product increases but the DET has less than the other two circuits.

VI. CONCLUSION

The design of Single edge and dual edge circuits are outlined and are simulated. It is observed that the as the frequency decreases power decreases and the delay, power delay product increases. The proposed design has achieved low power and better power delay product than the existing architectures.

VII. ACKNOWLEDGEMENT

I express my profound sense of gratitude to my guide Smt. A. Rajani Assistant Professor, JNTU Kakinada for her systematic guidance and valuable advices. I would like to express my sincere gratitude to Dr.A.M.Prasad, Professor, Head of the Department and Dr.K.Babulu, Professor, course coordinator, for providing me with all necessary facilities for the work.

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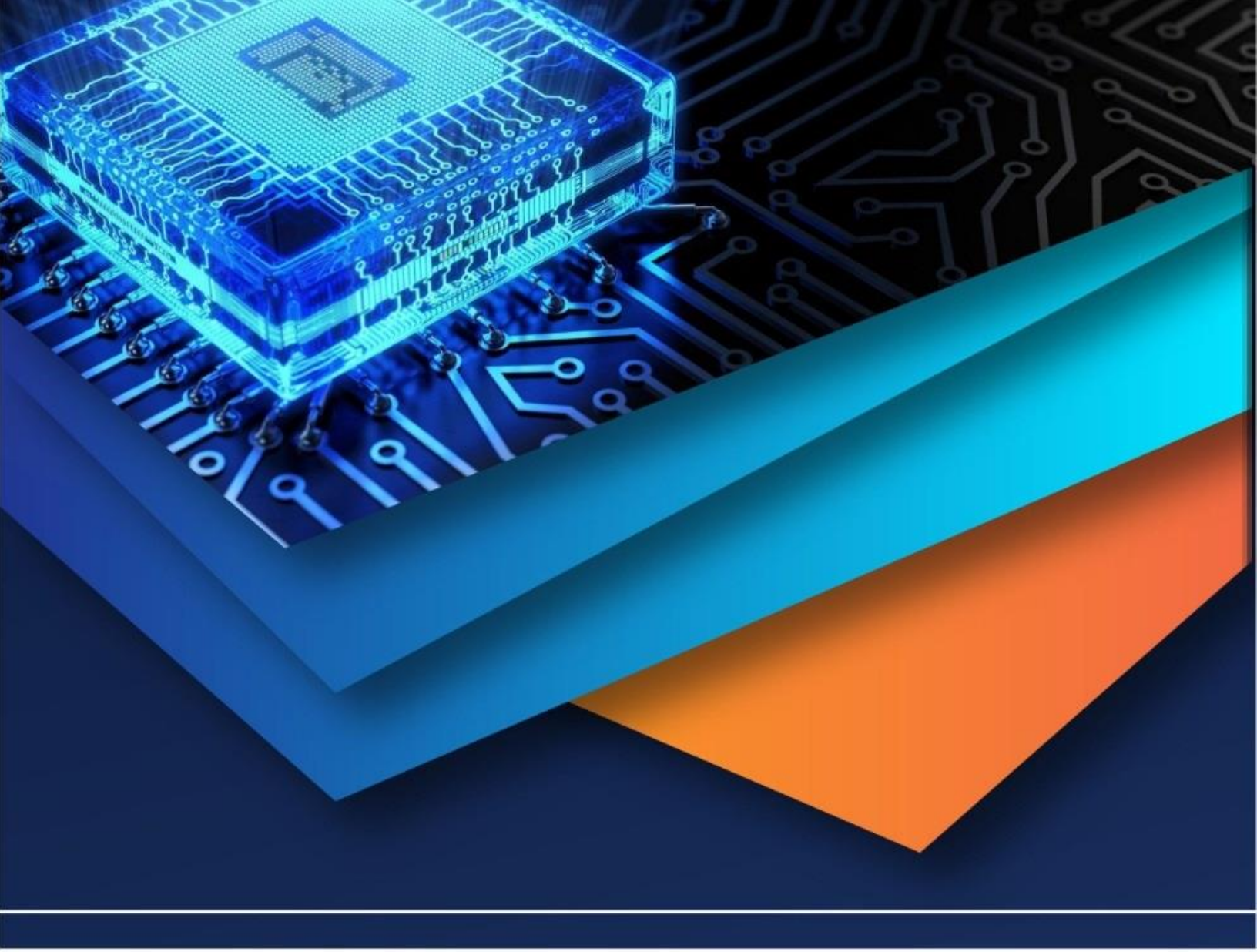

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