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Design of Five Port Router for 3x3 Mesh Network Using Verilog

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Abstract: ***With technological advancements, a large number of intellectual property (IP) cores can be integrated into a single chip. As a result, communication between these cores is critical. Such communication is achieved using Network on Chip (NoC) technology. NoC is an on-chip packet-switched network with IP cores connected to the network via interfaces, and packets are sent to their destinations via a multi-chip routing path. A router is the essential component of the NoC architecture, it must be designed efficiently to build a competitive NoC architecture. Verilog is used to design the router which supports five parallel connections. It uses store and forward type of flow control, round-robin arbitration, and deterministic XY routing. The building blocks of the router are FIFO, arbiter, and crossbar. The proposed architecture of the five port router is targeted to the Spartan 6 XC6SLX45 FPGA design platform and simulated in Xilinx ISE 14.5 software.***
Keywords: Network on Chip, Mesh topology, Router, XY routing, Verilog.

I. INTRODUCTION

Moore's law states that every two years, the number of transistors on an integrated circuit will double. A rapid progress in Very Large Scale Integration (VLSI) in the past recent years has resulted in the fabrication of millions of transistors on a single silicon chip [4]. On a single chip, more complicated systems are constructed. System on Chip (SoC) refers to a single chip on which all the components of a system are integrated. Due to the increase in the number of transistors on the chip, multicore architecture has been introduced. This architecture increases the performance without affecting the frequency. The system is integrated by adopting IP cores. As the complexity of a chip increases, the number of IP cores connected to a bus is limited and multiple cores find it difficult to communicate at the same time. While shared bus designs are effective for communication, they do have drawbacks. The scalability of direct connections between cores will be limited. According to the findings, a change in implementation technique was sorely needed, and one that had been recommended for over a decade. This paradigm shift is called Network on Chip. Using an on-chip packet switching network as a solution for global interconnects. Instead of direct connections between the cores, routers are used. Soon, NoC is projected to dominate computing platforms. The remainder of this paper begins by discussing a background on Network on Chip under section II. Section III describes the proposed five port router architecture. Section IV shows the synthesis and simulation results and is followed by a conclusion in section V.

II. NETWORK ON CHIP – A BACKGROUND

The NoC architecture is established to separate the concerns of the communication and application with the physical layout. This architecture has scalability as well as configurability features like a network. With this NoC communication architecture, hardware resources can be interconnected to the other resources in the network. The general architecture of 3x3 NoC is presented in Fig. 1, which contains Processing Elements (PE) and network elements.

Fig.1. General Architecture of 3X3 NoC communication

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The network element includes channels, Router, and Network Interface (NI). The Processing Elements may include a general-purpose processor core, arithmetic logic unit, digital signal processing, memory cores, or specialized IP cores which are interconnected to the network. The element of the network offers communication to the entire system. The connection between the PE and router will take place through NI, and the channels bring the connection among the Routers. A channel is a bi-directional point-to-point interconnection that provides the bandwidth required for data transmission. The NoC can have support towards N number of resources. The concern is about connecting these resources to achieve a higher degree of performance in terms of communication. The connections among the nodes and channels of the network in a physical layout can be considered as Topology. The router or switch is an important element that routes the data from the source node to the destination node. The routing information in the packet header is used to make routing decisions at every routing node.

III. ROUTER ARCHITECTURE

The router is the most important component in a network on chip [2]. The data transmission in a router takes place from an input port to any of the output ports. Fig. 2 shows the block diagram of the proposed router. There are five input ports and five output ports on the router. Four input ports and four output ports are used to connect neighbouring routers. A processing element is connected to a network interface via one input port and one output port. The data has to be buffered using FIFO at an input port before transmitting via an output port. Arbitration, routing algorithm, and flow control are the controlling aspects of a router that helps in governing data transmission. A packet is transferred to a destination according to route information in the packet header [3]. The arbitration decides the serving of incoming data by the router. The flow control decides the data forwarding to the next router (hop). The routing computation decides the data be forwarded through a crossbar.

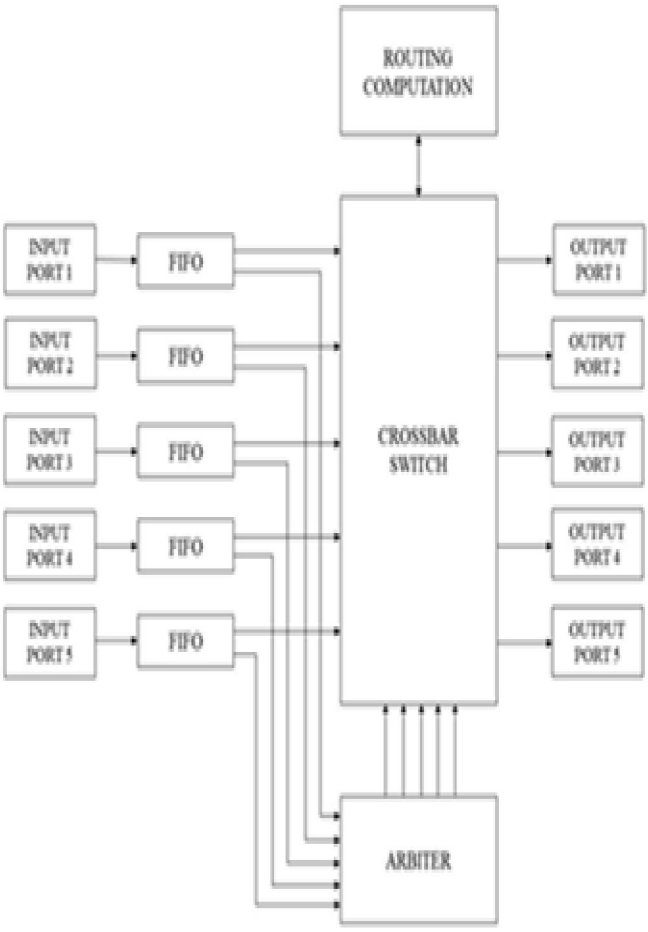

Fig.2. Block diagram of Router

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A. FIFO

The flow of data between the source and destination sides is controlled by FIFOs. Five FIFOs are required to store the data coming from individual input ports, it performs the read and write operations. Fig. 3 shows the block diagram of FIFO. Here the buffering method used is store and forward [4]. FIFO has full and empty control signals. Here for reading and writing operations, we use the synchronous clock. Write operation is done at the positive edge of the clock, write enable pin is one and FIFO is not full. In this condition, only the data write into the memory of the FIFO. If the read enables pin is high then at the rising edge of the clock, read operation is performed. If the FIFO is not empty then only the data is read from the memory of the FIFO.

Fig.3. Block diagram of FIFO

B. Arbiter

Arbitration is access to a shared resource between multiple agents [9]. Here arbiter uses a fixed round-robin algorithm. Fig. 4 shows the block diagram of the arbiter. It has five requests as inputs and five grants as outputs. The arbiter receives the requests from the five FIFOs and generates the grant signal for sending the input data from the source side to the output port. A round-robin arbiter schedules packets that have the same destination and output port. In a given time if there is more than one input port that requests the same output port then the arbiter will process according to the input priority request.

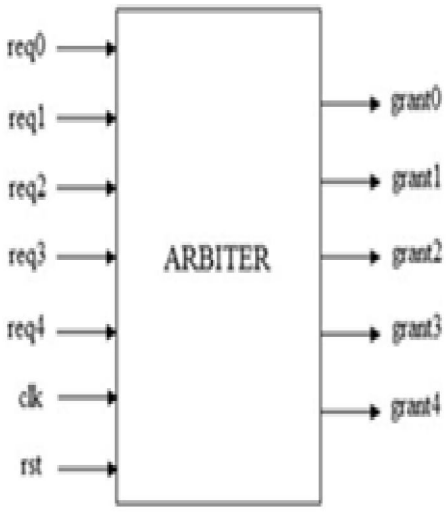

Fig.4. Block diagram of Arbiter

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C. XY routing

The XY routing is a distributive deterministic routing algorithm, which uses the coordinates to determine the destination and deliver the packet through a network. Fig. 5 depicts the XY routing algorithm. In the XY routing algorithm packet routes first horizontally along with the x-coordinate to reach the column and later, vertically along the y-coordinate to arrive at the destination. This routing is highly preferred for mesh and deadlock-free networks.

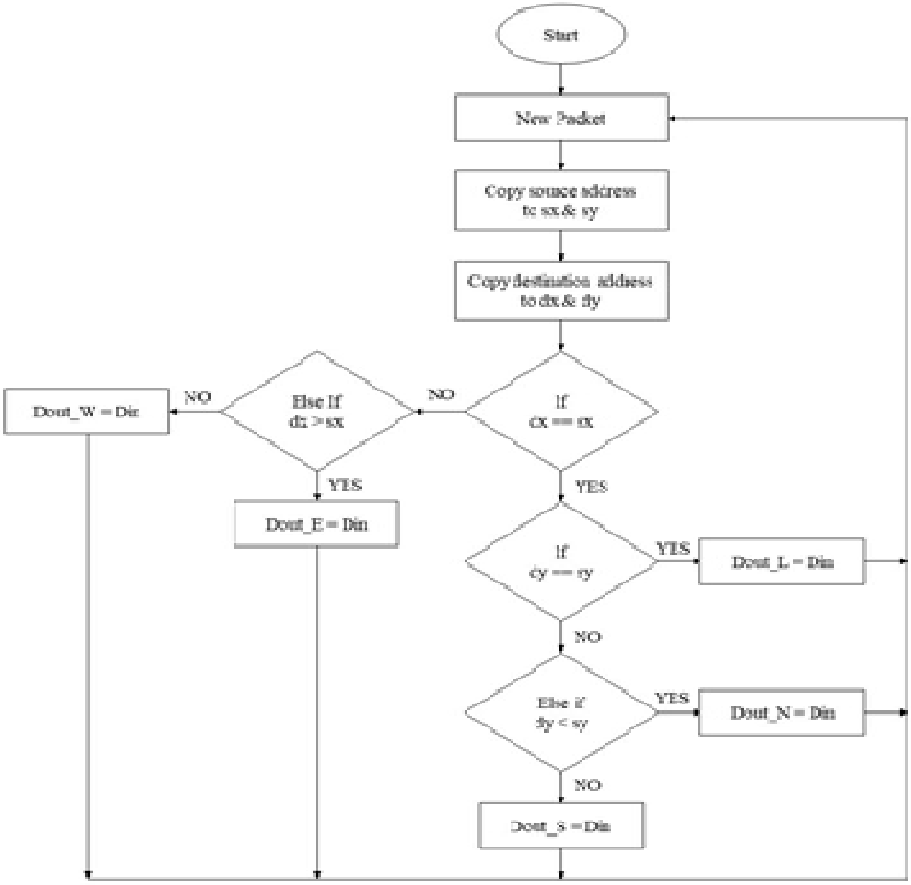

Fig.5. XY Routing Algorithm

D. Crossbar

The crossbar is the heart of the router data path. It switches the data from the input port to the desired output port. This is the essence of the router function. Fig. 6 shows the block diagram of the Crossbar. It has five inputs and five outputs to transport 16-bit data. The crossbar fabric is configured to send the data to any output port from any input port.

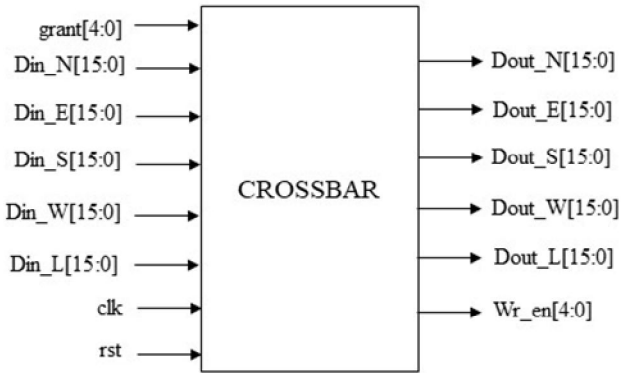

Fig.6. Block diagram of Crossbar

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IV. RESULT ANALYSIS

The five-port router for Network on Chip has been designed using Xilinx ISE 14.5 tool and implemented on Spartan-6 FPGA kit, Fig. 7 describes the simulated results and Fig. 8 represents the RTL schematic of the router. Fig. 9 shows the ChipScope Pro Analyzer VIO output. Table I gives the utilization percentages of the required FPGA resources to design five port router.

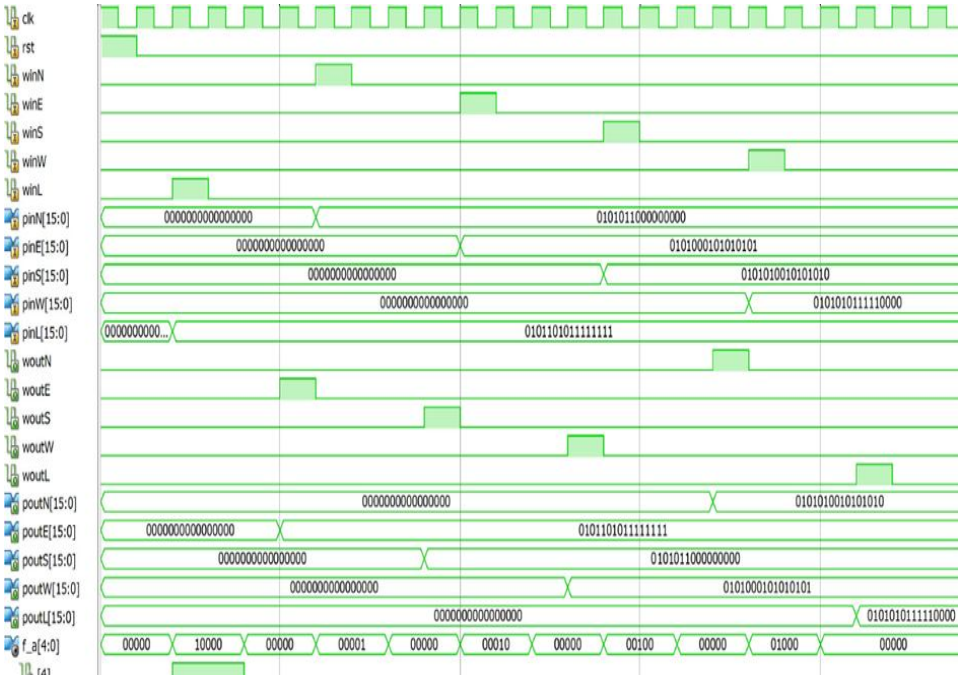

Fig.7. Simulation of router block

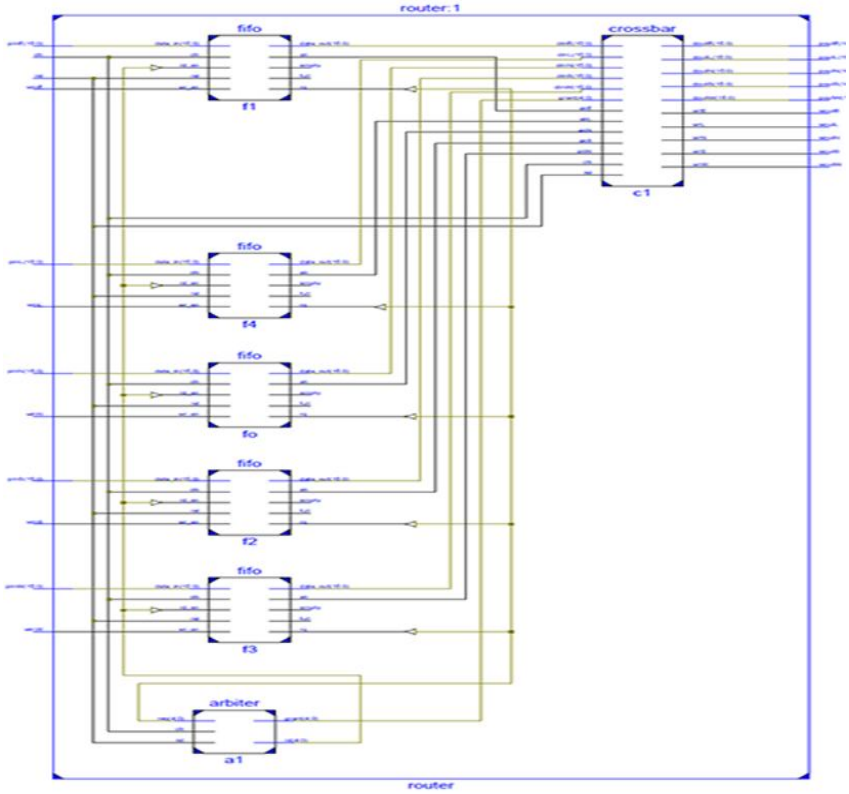

Fig.8. RTL schematic of the router

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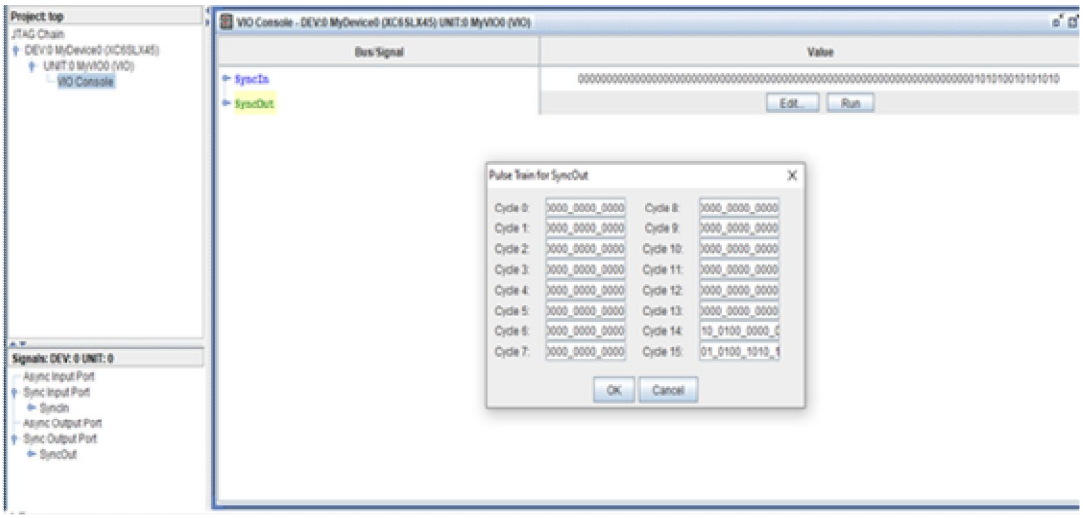

Fig.9. ChipScope Pro Analyzer VIO output

TABLE I

The device utilization summary for five port router

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	552	54576	1%
Number of Slice LUTs	1104	27288	4%
Number of fully used LUT-FF pairs	539	1117	48%
Number of bonded IOBs	172	218	78%
Number of BUFG/BUFGCTRL/BUFHCEs	1	16	6%

A. Timing Summary

1) Max Frequency: 168.233MHz

2) Maximum Setup Time of the clock 5.299ns

3) Maximum Hold time of the clock: 3.668ns

According to the above waveform, five packets are sent through five input ports i.e. pinL, pinN, pinE, pinS, and pinW. The proposed round-robin arbiter selects each packet one after the other and the XY Routing algorithm determines which output port should be allocated to respective packets i.e. poutE, poutS, poutW, poutN, and poutL.

V. CONCLUSION

A five-port router has been proposed in this paper. The proposed router is designed using Verilog and simulated using Xilinx 14.5 software. The design is targeted to the Spartan 6 XC6SLX45 FPGA design platform. The simulation makes it easier to comprehend the routing pattern and functioning of a five-port router for a Network on Chip. In the future, we intend to work on upgrading the router's scheduling mechanism to improve performance.

VI. ACKNOWLEDGEMENT

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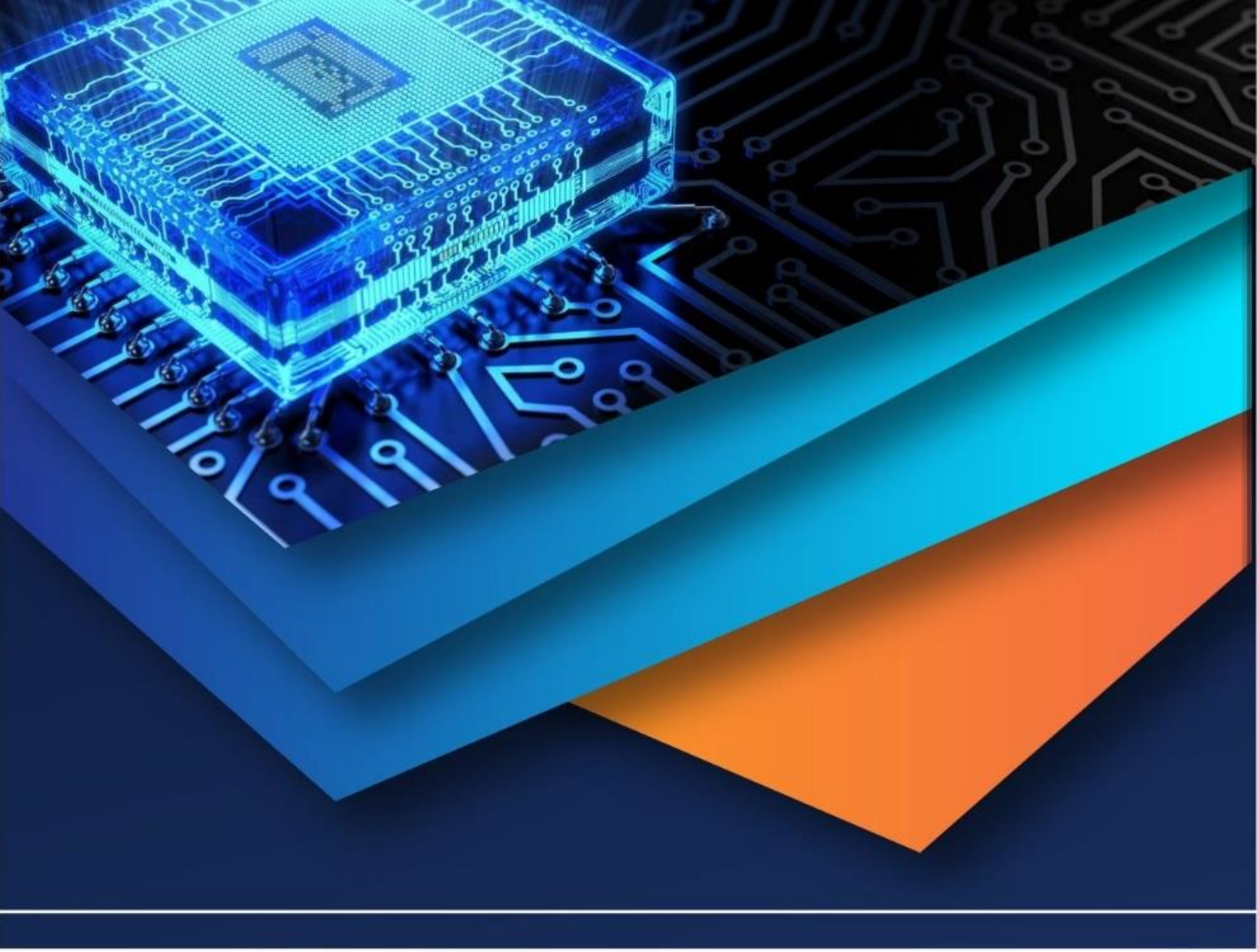

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