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Compare the Symmetric Hybridized Cascaded MLI with 17 levels with the Asymmetric Switched Capacitor MLI Topologies for Dynamic Loading

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Abstract: ***This article builds a symmetric hybridized cascaded a switching capacitor unit in a multilayer inverter and compares it to For 17 level inverters, A switched capacitor unit is utilized with an asymmetric multilevel inverter. In the symmetric hybridized multilevel inverter design, a In the midst of a dual-input dc source, there is a bi-directional switch is utilized to create a modified H-bridge inverter with a five-level output voltage instead of three. In the proposed scenario, In an asymmetric multilevel inverter, the switched capacitor unit substitutes the dc sources. which enlarges By a factor of two, The output voltage has been increased. and the voltage levels at the loads are increased by a factor of two. MATLAB-SIMULINK was used to verify the suggested topology using the staircase modulation approach. The findings show that multilayer inverter topologies with low total harmonic distortion, fewer switches, With greater levels of output voltage are better stable during load disturbance circumstances, making them ideal for renewable energy applications.***

Keywords: Multilevel inverter (MLI), staircase pulse width modulation technique (SPWM), switched capacitor unit (SCU), total harmonic distortion (THD), high output voltage levels.

I. INTRODUCTION

For greater voltage levels, multilayer inverters were created and used [1]. Multilevel inverters (MLI that are connected in a cascade have shown to be more versatile than traditional topologies in terms of attaining larger voltage and power levels. The inverter's modularity may be used to boost the inverter's power output. To produce cascaded MLIs, Many H-bridge inverters' output terminals are linked in series. [2], [3]. As a result, it is clear that this design allows for large power levels while using inverters with modest voltage ratings. Because of its modularity, If one of the inverter cells fails, it may be changed quickly and simply. A appropriate control method can be utilized to bypass a damaged inverter cell without stopping the load in the case of a malfunction in any inverter cell. preserving inverter output dependability [4]. With improvements in multilevel inverters, the demand for novel modulation methods for these devices is becoming more urgent. As a result, a slew of modulation techniques have emerged. Each modulation approach has advantages and disadvantages based on converter architecture and application domain. Depending on whether you're switching at a high or low frequency, [7] suggested a categorization of modulation techniques for multilayer inverters. A frequency of 1 kHz is used in high-power applications. Hybrid cascaded MLI [8] can also use PWM switching. This shortens the time it takes for storage components in multilayer inverters to charge and discharge. Modulation with a level shift and a phase shift techniques are two types of PWM systems that rely on the carrier. In order to create high-quality output waveforms, Many applications make use of level shift modulation techniques. DC magnitude is triangular, saw-toothed, and constant. waveforms can all be utilized as carriers in these approaches. Voltage sinusoidal waveforms, sinusoidal waveforms with a third harmonic inserted onto themand trapezoidal are examples of reference voltage waveforms that can be utilized in PWM systems. Researchers are now interested in selective harmonics removal, [9]-[15], also known as fundamental frequency switching. There are symmetric and asymmetric setups to choose from. with the cascaded MLI. Because the amplitude of the input DC sources is equal in the symmetric arrangement, the number of output levels is reduced, and more switches are used, resulting in greater overall distortion of harmonics (THD). DC sources with asymmetric MLI input, on the other hand, are uneven, allowing for various voltage levels to be created. More levels can be created with fewer switches when such voltage levels are combined, resulting in a decrease in THD. [16]-[19]. Two alternative Topologies for 17-level symmetric and asymmetric multilevel inverters are suggested. in this study: A novel phase hybridized stair-case cascaded multilevel inverter modulation method is proposed in the symmetric arrangement. An asymmetric multilevel inverter design with a switched capacitor unit is suggested. A detailed comparison of inverter topologies is also carried out.

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II. METHODOLOGY

A. 17-Level Hybridesed Cascaded Mli Topology Proposed In Symmetric Form

As illustrated in Figure 1, the 17-level symmetric inverter was developed and implemented using a hybridized H-bridge circuit architecture. Two steps may be seen in the operation of suitable topology. The output levels +V1, 0, -V1 are provided to the second leg of the H-bridge in the first stage, whereas the output levels +2V1, 0, -2V1 are created in the second stage. Figure 2 shows the symmetric basic hybridized cascaded MLI topology's produced five-level voltage of the output The various switching states that reflect the fundamental MLI's status are shown in Table 1.

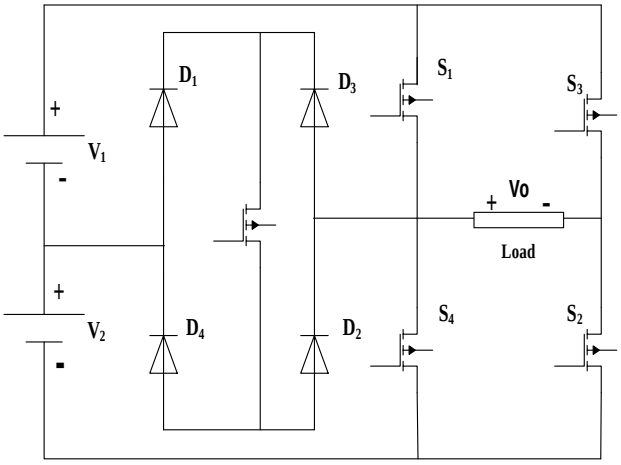


Figure 1: Hybridized H-bridge with 5 levels topology in its simplest form.

Table 1. Table of suggested fundamental hybridized MLI states

Levels of Output Voltage	Switching states				
Switches	S_1	S_2	S_3	S_4	S_A
+2V	1	1	0	0	0
+1V	0	1	0	0	1
0	0	1	0	1	0
0	1	0	1	0	0
-1	0	0	1	0	1
-2	0	0	1	1	0

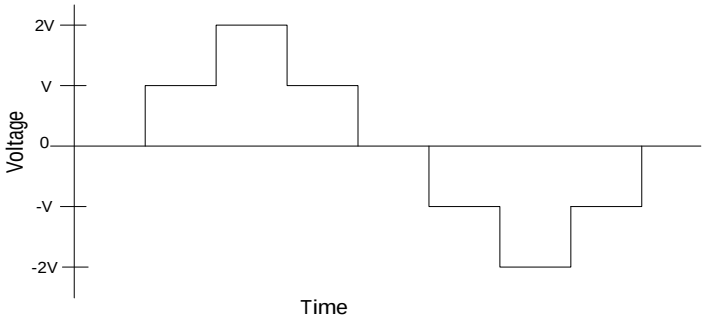


Figure 2.Waveform of output voltage with five levels

B. Staircase Modulation Technique

Kjeld Thorborg and Ake Nystrom were the pioneers of the The method of stairwell modulation. Staircase modulation is a concept that has been around for a long time. is to compare a high frequency triangular wave, Vtri, to a staircase modulating waveform, Vm. When the value of the staircase modulating signal exceeds the value of the triangle carrier signal, pulses are generated. This PWM pattern has been fine-tuned to produce an appropriate output voltage spectrum over the whole control range. The output voltage's frequency and fundamental component are both independently regulated and proportionate to the control voltages. The procedure for obtaining the required output Figure 3 depicts a voltage waveform. The triangle wave pattern is preserved, as is the case with most modulation methods, but the sine wave (as in sinusoidal PWM) is replaced by a staircase waveform. The staircase isn't supposed to be a sampled sine wave approximation. To achieve the required output voltage quality, two factors are chosen: modulation index M = Am / Atri and the number of steps. To create the triggering pulses for all the IGBTs, the pulses acquired after comparison are coupled with the control logic described.

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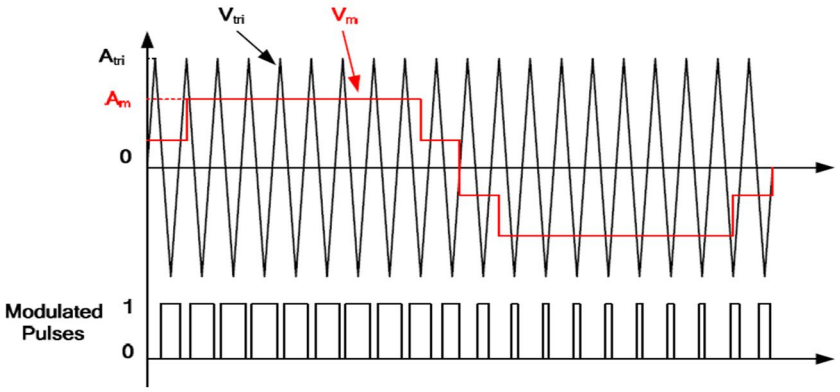


Figure 3. Staircase Modulation Technique modulated pulses

C. Circuit Parameters Are Calculated As Follows

The number of sources, switches, and output voltage levels are all factors to consider. are all factors to consider. are all discussed in the sections that follow. The dc sources' values are uneven in symmetric hybridized and asymmetric multilayer inverters, allows a large number of different output levels to be generated with a small number of switches The kth cell's DC sources and the pk cell's DC sources are assumed to be the same.

The input DC sources are equivalent in the inverter equations and the suggested symmetric hybridized multilevel inverter may be expressed as follows.

$$V_{d1} = V_{d2} = \bullet\bullet\bullet\bullet\bullet\bullet = V_{dk} = V_d \quad (1)$$

The following is a list of the possible levels to calculate: n = each cell's number of DC sources, m = number of cells.

$$N_{Levels} = 2mn + 1 \qquad (2)$$

The switches can be estimated as

$$N_{switch,k} = 2pk + 1 \qquad (3)$$

The highest output voltage is roughly equal to

$$V_o = mnVd \qquad (4)$$

The suggested The input of an asymmetric multilevel inverter Because the DC sources are not equal, the equation may be written as

$$V_{d1} = V_1 = V_d \qquad (5)$$

As a result, In the kth cell, the magnitude of the dc voltage source is given by

$$V_{dk} = (2p1 + 1).(2p2 + 1)\ldots.. \quad (2pk-1 + 1).Vd$$

$$= Vd .\prod_{j=1}^{k-1}. (2pj + 1) \quad (6)$$

In the kth cell, pk is the number of dc voltage sources, and kth is the number of cells. To calculate the number of output voltage levels, apply the formula below:

$$N_{Levels} = (2p1 + 1).(2p2 + 1)\ldots\ldots.. \quad (2pm + 1)$$

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$$= \prod_{j=1}^{m}.(2pj + 1) \qquad (7)$$

The following is an estimate of the maximum output voltage.

$$V0 = \frac{[(2p1 + 1).(2p2 + 1)____(2pm + 1)] - 1}{2}.Vd$$

$$= \frac{\left[\prod_{j=1}^{m}.(2p1 + 1)\right] - 1}{2}.Vd \qquad (8)$$

The number of switches expected is

$$N_{switch,k} = 2(pk + 1)$$

$$= \sum_{j=1}^{m} 2(pj + 1) \qquad (9)$$

The amount of switches available, voltage levels, and suggested topologies' output voltage may all be calculated using the aforementioned formulae.

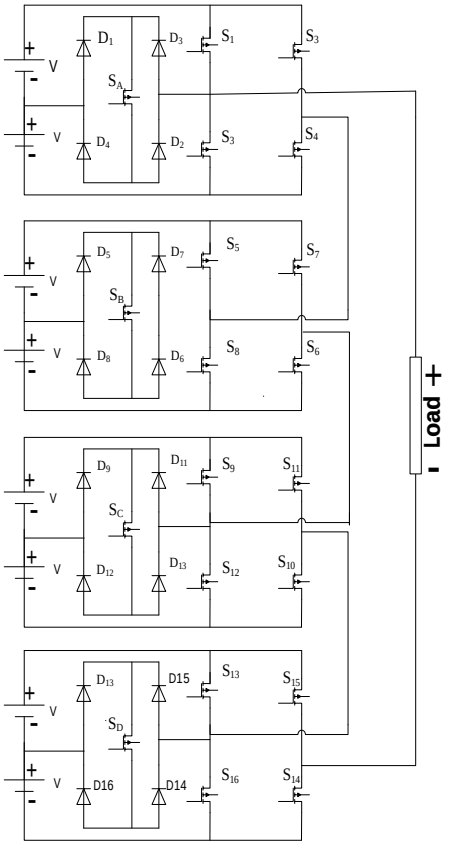


Figure 4: A symmetric 17-level MLI has been proposed

Table 2. MLI with 17 levels of symmetry switching state table.

V_0	1	2	3	4	5	6	7	8	0		-1	-2	-3	-4	-5	-6	-7	-8
S_1	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
S_2	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_3	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_4	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
S_5	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
S_6	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_7	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_8	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
S_9	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
S_{10}	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_{11}	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_{12}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
S_{13}	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
S_{14}	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_{15}	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_{16}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
S_A	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
S_B	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
S_C	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0
S_D	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0

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Figure 4 depicts symmetric hybridized cascaded MLI with 17 levels suggested In this topology, each H-bridge operates similarly to the basic Hybridized H-bridge architecture Figure 1 illustrates this. To get a range of output voltage values, pulses are created using a staircase modulation method in this symmetric inverter.

Pulses are produced and sent separately. The outputs of the first, second, third, and fourth stages are received by the first, second, third, and fourth stages, respectively. before they are combined to provide the proper output voltage. Table 2 shows the various The statuses of the power switches are controlled. All of the input voltage sources in this proposed architecture are set to V=25 V in order to come up with a When the load is finished, From peak to peak, the maximum voltage is 200 V. The loads utilized in the tests were a 100Ω resistor and a 175 mH inductor. Figure 7 shows the voltages at each step, as well as the output voltage and current.

D. MLI Switched Capacitor With 17 Levels Topology Proposed In Asymmetric Form

Figure 5 (a) depicts the fundamental architecture of the proposed switching capacitor. Two switches, a switched capacitor unit, a diode, and a supply voltage are all part of the suggested architecture. The load's input voltage is doubled by the switching capacitor [20]-[22]. The S2 switch will charge and discharge capacitor C'. through the S1 switch when the input voltage is delivered to the circuit. The suggested architecture provides With fewer switches, At the load ends, you may see voltage values of +V and +2V. The S1 and S2 switches have different switching patterns, as well as the voltage across the capacitor during the ON and OFF phases of the switch, are shown in Figure 5. and the voltage across the load at the output (b). While the capacitor charges, the load voltage equals the input voltage, and the capacitor charges to the input voltage. 12.5 V is the voltage. The input voltage plus the capacitor voltage equals 25 V. equals the load voltage. during discharge. The output voltage is doubled when the capacitor is discharged, according to the measurements. With this design, the output voltage for multi-levels may be increased while the input voltage is kept low. Figure.6 illustrates the proposed 17-level switching capacitor architecture. In the recommended architecture, There are ten switches and two switched capacitor units, each including There are two capacitors, two diodes, two supply voltage sources, and two capacitors in total. When powered up to 200 V, At the load end, the proposed switching capacitor units create 17 levels (peak to peak). The switched capacitor units receive separate pulses, which are then combined to generate the correct output voltage. Table.3 illustrates the reasoning behind switching The Waveforms of the proposed switching capacitor's output voltage and current units 1 and 2, as well as the suggested output voltage and current waveforms switched capacitor units 1 and 2, Figures 8(a), (b), and (c) illustrate the results (c). The 17 proposed level inverter voltage expressions and level voltages are listed in Table 3.

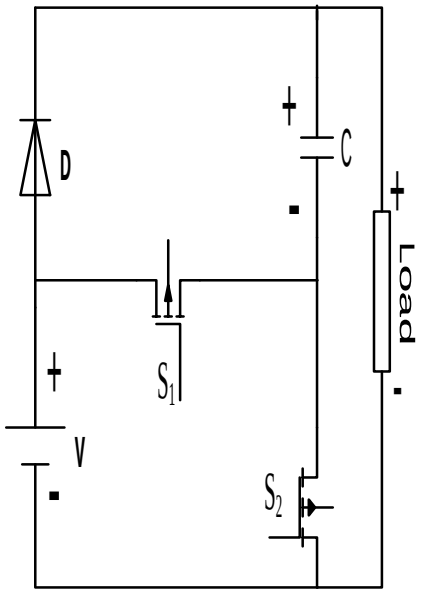


Figure 5: Topology of a Proposed Switched Capacitor Unit.

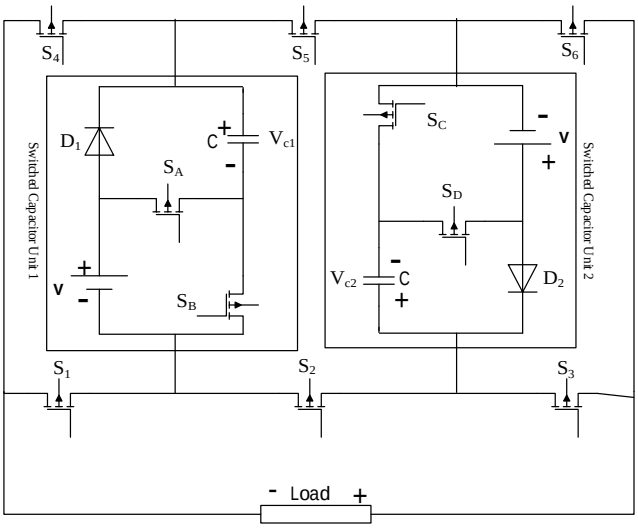


Figure 6: Asymmetric Switched Capacitor MLI with 17 levels proposed.

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Table 3: 17-level asymmetric inverter switching state table

V_0 Level	S1	S2	S3	S4	S5	S6	SA	SB	SC	SD	Levels of Output Voltage Expression	Output Voltage (V)
1	1	0	1	0	1	0	1	0	0	1	$4V+V_{C1}+V_{C2}$	100
2	1	0	1	0	1	0	0	1	0	1	$4V+V_{C2}$	87.5
3	0	0	1	1	1	0	0	1	1	1	$3V+V_{C2}$	75
4	1	0	1	0	1	0	1	0	1	0	$4V+V_{C1}$	62.5
5	1	0	1	0	1	0	0	1	1	0	4V	50
6	0	0	1	1	1	0	0	1	1	0	3V	37.5
7	1	0	0	0	1	1	1	0	0	0	$V+V_{C1}$	25
8	1	0	0	0	1	1	0	1	0	0	V	12.5
9	1	1	1	0	0	0	0	1	1	0	0	0
10	0	1	1	1	0	0	0	1	0	0	-V1	-12.5
11	0	1	1	1	0	0	1	0	1	0	$-V-V_{C1}$	-25
12	1	1	0	0	0	1	0	1	1	0	-3V	-37.5
13	0	1	0	1	0	1	0	1	1	0	-4V	-50
14	0	1	0	1	0	1	1	0	1	0	$-4V-V_{C1}$	-62.5
15	1	1	0	0	0	1	0	1	0	1	$-3V-V_{C2}$	-75
16	0	1	0	1	0	1	0	1	0	1	$-4V-V_{C2}$	-87.5
17	0	1	0	1	0	1	1	0	0	1	$-4V-V_{C1}-V_{C2}$	-100

III.SIMULATION RESULTS

A. Simulation results of 17 level Symmetric MLI as follows

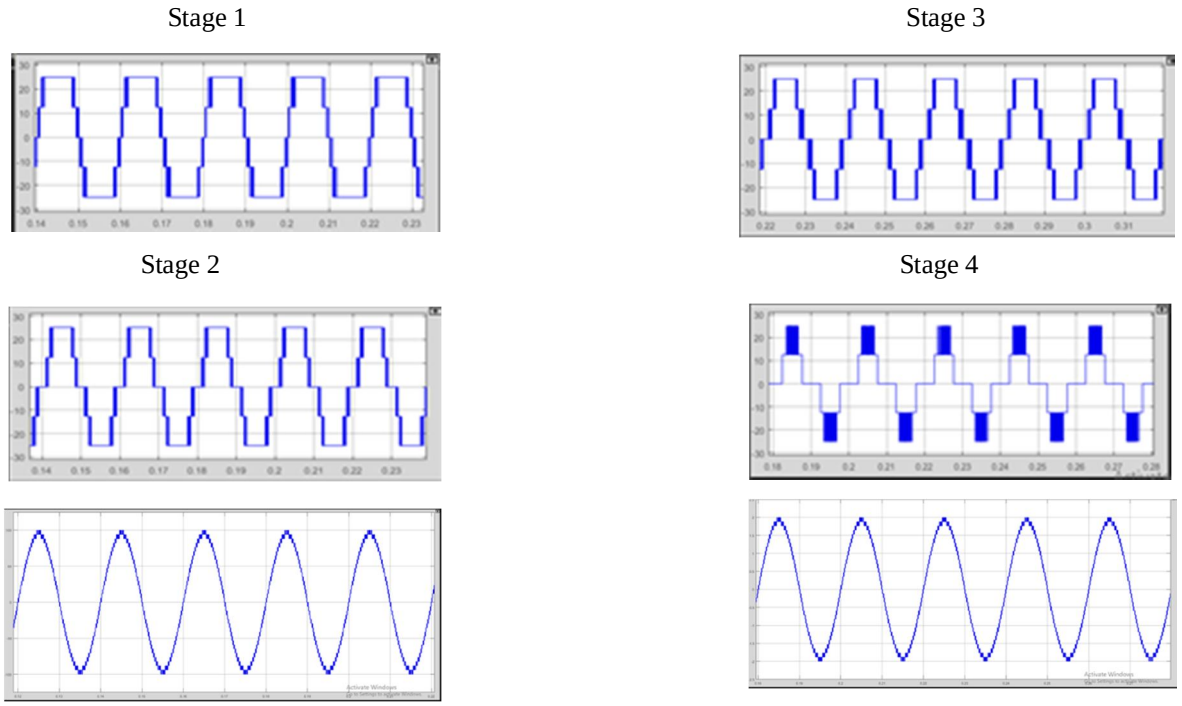
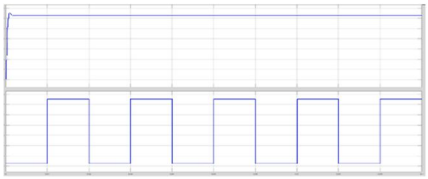


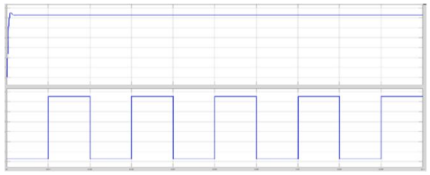
Figure 7: Individual stage output voltages, as well as the output voltage and current of a 17-level symmetric MLI.

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B. Simulation results of 17 level Asymmetric MLI as follow



(a) Switching capacitor unit 1 waveforms for 17-level MLI. Vc1=12.5V, V0=V+Vc1=25



(b) Switching capacitor unit 2 waveforms for 17-level MLI. Vc1=37.5V, V0=V+Vc2=37



© Peak-Peak Output Voltage=200V



(d) Peak-Peak Output Current=2A

Figure 8. Individual stage output voltages, as well as the output voltage and current of a 17-level Asymmetric MLI.

C. Proposed Topologies are Compared

Table 4: Comparison of 17-level Symmetric and Asymmetric MLI table

Item	17 level Symmetric MLI	17 level Asymmetric MLI
DC Sources	8	2
Switches	20	10
Diodes	0	2
Capacitor	0	2
THD	5.41%	4.54%

IV. CONCLUSIONS

The 17-level symmetric and asymmetric multilevel implementation and analysis inverter are presented in this study. With both unity and trailing power factor loads, the suggested There have been 17 level inverter systems successfully tested. In instance A, testing was done in a THD study utilizing a 17-level symmetric inverter output in a steady-state situation with load disturbance conditions. Case A findings indicate that the system is easily adaptable and maintains a steady output voltage with a THD of 5.41 % under the aforementioned parameters, whereas case B results show a THD of 4.54 %, which is within IEEE requirements. The suggested topology is also appropriate for abrupt load variation applications during load disturbances. Because of the reduced THD, these topologies automatically use fewer switches and fewer The addition of dc input voltage sources appears to have increased the density of the volume suggested inverter. The multilevel inverters with the recommended architecture are Appropriate for renewable energy applications. based on the findings of cases A and B.

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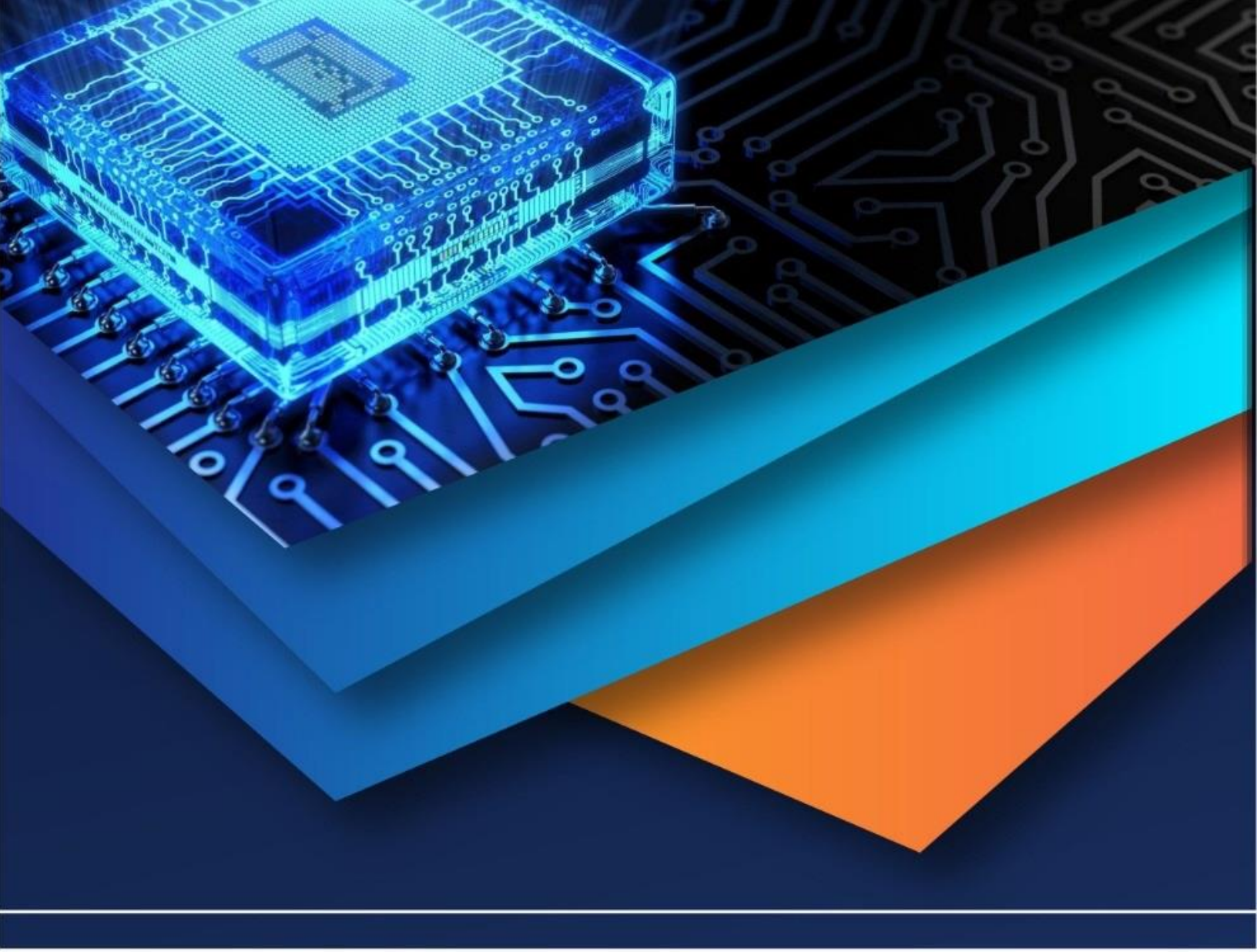
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