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Implementation of 32-BIT Pipelined ADC Using 90nm Analog CMOS Technology

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Abstract: ***After seeing the technological evolution, we have understood about the A/D converter that it is the meeting point of the analog to digital domains. As technology is being continuously scaled down, the transistor sizes have decreased drastically resulting in reduced area and power consumption in the digital domain. The successive approximation ADC is best suitable for low power applications with moderate speed and simple design. Here, the implementation of 32-bit pipelined analog-to-digital converter with the help of successive approximation register based Sub-ADC. The SAR ADC architectures are popular for achieving high energy efficiency and low power applications. But they suffer from resolution and speed limitation. To overcome the speed limitations of SAR ADC, we proposed the implementation of 90nm using CMOS technology of a low power, high speed pipelined analog-to-digital converter (ADC). The capacitive digital-to-analog converter (DAC), two stage CMOS comparator with output inverter of proposed ADC are lower than those of a conventional ADC. To achieve low power and to minimize the size of the input sampling capacitance in order to ease durability.***

Keywords: Analog-digital convertor (ADC), data conversion, low power, successive approximation register architecture (SAR), digital to analog convertor (DAC).

I. INTRODUCTION

The high-resolution and power efficient analog-to-digital converter has always been in demand for various applications such as cable TVs, ultrasonic medical imaging, broadband satellite transmitters and receivers. The most important advantage of CMOS technology is that it dissipates less power and by using pipelined ADC with the CMOS technology, it will convert the signal from analog to digital more accurately and achieve high speed in all applications and going to consume less power that will make it more widely usable. The low power ADC with minimum resolution and low sampling frequency is the most suitable combination for biomedical applications.

The electronics of biomedical has achieved a significant position in healthcare industry, where biomedical devices are playing very crucial role in the diagnosis of diseases, in the cure, for the prevention of disease and for the mitigation also. They are used in so many life saving conditions such as cardiac pacemakers for arrhythmia, and retinal implants for blindness and so on. There has been so many researches regarding the brain machinery and with each research the main concern is the biomedical application's speed and power.

Generally, Bio-medical signals do not vary too much so to resolve this we need to proceed in a very simple way for the conversion, and which will lead to lot of power consumption with less speed. So, Conversion with the previous architectures is not precisely used for bio-medical signals .The best solution for the conversion till now is SAR ADC as it consumes low power due to its simple and easy structure. The specification of SAR ADC makes the most suitable choice, but the only problem is that it suffers from the resolution and speed limitations.

To resolve the limitation issue of SAR ADC, we proposed a systematic design of a low-power, high-speed pipelined Analog-to Digital Converter (ADC). The circuits that we used to design the pipelined ADC are Successive Approximation Register ADC, Digital to Analog Converter (DAC), static cross-coupled CMOS Comparator, Sample and Hold circuit, Edge Triggered D Flip flop with set and reset pins, a control unit consist of a multiplexer, a d flip-flop and an HL flip-flop. Successive Approximation Register ADC uses the binary algorithm in conversion which makes the operations more easily. Multiplexer, a d flip-flop and an HL flip-flop is used as an control unit by leveraging with DAC makes ease of mitigating capacitance holding size, the proposed pipelined DAC with the cross-coupled CMOS Comparator which outputs the bit because of its high resolution.

To balance the signals at a moment, the input signals which we are giving must be sampled .In order to make it happened, the sample and hold circuit is used for a better sampling process. A chronic nature of clock prevents the need of synchronization for the whole circuit to ensure the balanced leveraging of the output of foregoing blocks in the circuits

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II. LITERATURE REVIEW

We can implement the ADC with many different kind of Specifications' which we are concern of. If we use the flash ADC then it's time conversion does not change materially which leads to the complexity of the structure and the increase in resolution which doubles the ADC circuitry per bit. Therefore, the SAR ADC will have some advantages over the flash ADCs to fulfill the required specifications.

A. It consumes less power as its structure consists of only one comparator, DAC and they all consumes little power.

B. It follows only one simple principle i.e. the binary search algorithm, which prepares it or simplification and for implementation than the other ADC designs. Since the main purpose of the paper is to achieve a low power and small area ADC, the SAR architecture has been chosen as sub-ADC. But as we all know that SAR ADC has the limitation of high resolution and speed. So, to resolve this issue we proposed a high speed, power efficient Pipelined ADC.

III. PROPOSED ADC FLOW CHART

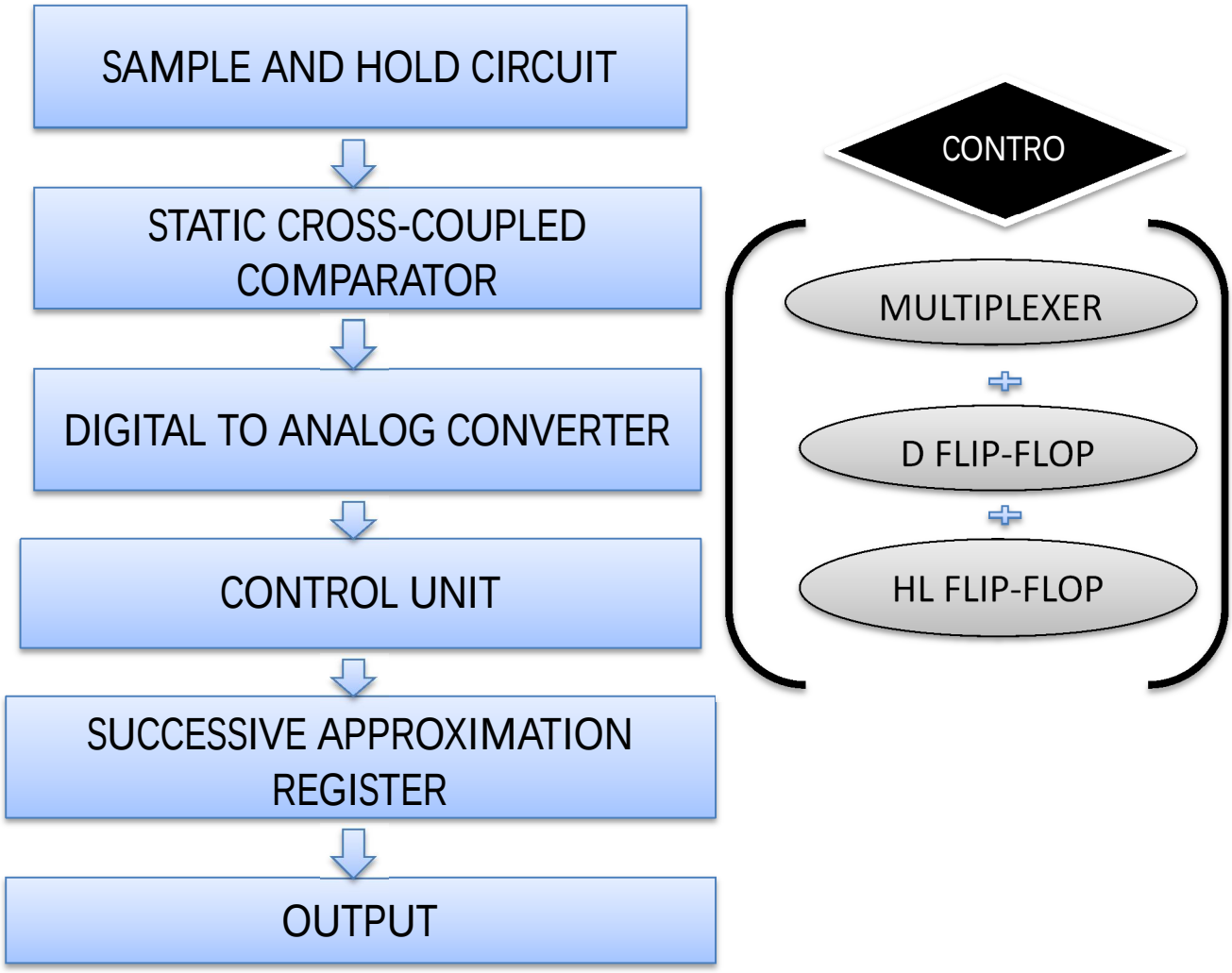


Fig. 1 Block diagram of ADC

The fig.1 shows the block diagram for ADC architecture as it represents the function of the whole circuit of 32-bit SAR-ADC. In each stage, the analog input is sampled by the sample and hold circuit. Then signal is quantized by sub-ADC to resolve the issue of N-bits. By using a sub-DAC the value which is quantized of the sub-ADC is again converted into analog voltage value and gets subtracted from the original input signal to overcome the quantization error.

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IV. COMPONENTS OF SAR-ADC

A. Sample And Hold Circuit

Sample-and-hold (S/H) circuit is one of the main significant analog building blocks, especially in analog-to-digital converters (ADCs). It is also often referred to as “track-and-hold” circuit.

Normally, these two terms are synonymous except for a few individual switched capacitor, sample and hold circuits that do not have a phase where the output signal is tracking the input signal. It is the first block of the ADC components in which the input signal is seen by the input of the S/H circuit.

Therefore, it has a significant effect on the whole ADC performance which in turns will affect the overall system. In many cases, using the S/H circuit at the front of the data converters have a significant effect. This effect appears in minimizing the errors due to slightly different delay times in the internal operation of the converter

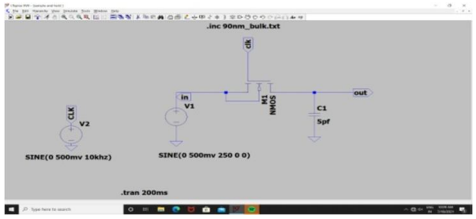


Fig. 2 Circuit diagram of sample and hold circuit

B. Static Cross-Coupled Comapartor

The comparator is the second most widely used component in electronic circuits, after operational amplifier. It is a key building block for applications where digital information needs to be recovered from analog signal especially in ADCs.

It is the second block of the ADC components in which the output of S/H circuit seen by the input of the comparator. Therefore, it has a significant effect on the whole ADC performance which in turns will affect the overall system.

In the static comparators, at every point in time (except during the switching transients), each gate output is connected to either (VDD) or (VSS) via a low-resistance path. It is used in medium speed applications.

Static comparator is a suitable choice for medium speed applications. It has advantages of good performance and robustness (i.e. low sensitivity to noise), but unfortunately it has static power dissipation. The static power dissipation is due to the short circuit power dissipation which is the direct current path from the supply voltage to the ground while the switches are ON simultaneously for a short period.

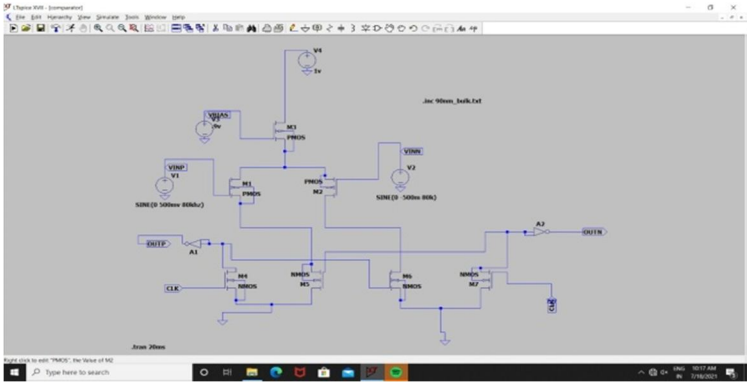


Fig. 3 Circuit diagram of static cross-coupled comparator

C. Digital-To-Analog Converter

There are four main types of digital-to-analog converter (DAC) circuits which are decoder based, binary weighted, thermometer code and hybrid. The main theme of this work is to reduce the power consumption therefore the binary weighted DAC is the most suitable type in term of low power.

The binary weighted type might be binary arrays of currents signals (in resistor or current approaches) or binary weighted arrays of charges. The conventional voltage driven R2R techniques suffers from difficulties in the fabrication process. In addition to that, it requires careful control of the on-resistance ratios in the MOS switches over a wide range of values.

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Therefore, the binary weighted arrays of charges is preferred due to the following advantages: As the MOS device is used as a charge switch, it has inherently zero offset voltage and as an amplifier, it has very high input resistance. In addition to that, capacitors are easily fabricated in metal gate technology. As a result, using the capacitors rather than the resistors as the precision components, and using the charge rather than the current as the working medium.

Fig. 4 shows the schematic of DAC which is made up of 9 NMOS and 8PMOS and also and capacitors whose range is from 50f to 6400f.

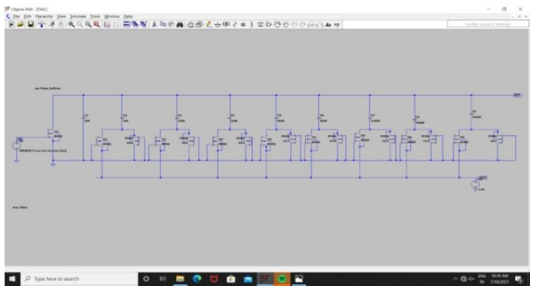


Fig. 4 Circuit diagram of DAC

D. Control Unit

The control unit consist of an multiplexer, an D flip-flop and an hybrid latch flip-flop which are going to work as an controlling part for the digital-to-analog converter.

This control unit will give its output to the Comparator for the further processing and each part of this control unit is going to play its part to improve the speed and size.

1) D Flip-Flop

The D flip flop is the most important flip flop from other clocked types. It ensures that at the same time, both the inputs, i.e., S and R, are never equal to 1. The Delay flip-flop is designed using a gated SR flip-flop with an inverter connected between the inputs allowing for a single input (Data).

D Flip-Flop One of the most frequently used sub-circuits of SAR ADC is Flip Flop. Flip-flops are critical timing elements in digital circuits which have a large impact on circuit speed and power consumption. The performance of the Flip-flop is an important element to determine the performance of synchronous circuit.

Fig.5 shows the schematic of D flip-flop which consist of 5 NAND gates and a clock at the input.

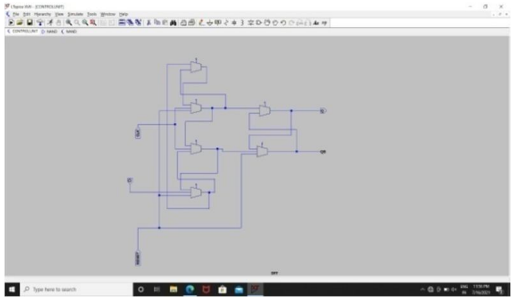


Fig. 5 Circuit diagram of D flip-flop

2) Multiplexer

Multiplexer is a combinational circuit that has maximum of 2 n data inputs, ‘n’ selection lines and single output line. One of these data inputs will be connected to the output based on the values of selection lines. Since there are ‘n’ selection lines, there will be 2 n possible combinations of zeros and ones.

Fig.6 shows the schematic of multiplexer which consist of 4 NOR gates and 5 inverters and having an chronic nature of clock to ease the durability.

The main reason for using a SAR ADC in a multiplexed data acquisition system is its fast response with no latency. Note that although the sensors connected to the multiplexer may produce low-frequency (nearly DC) signals, the multiplexer output can have rapid fluctuations.

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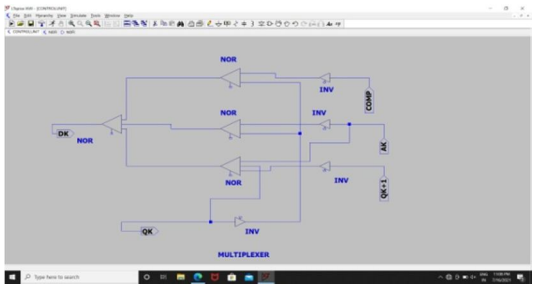
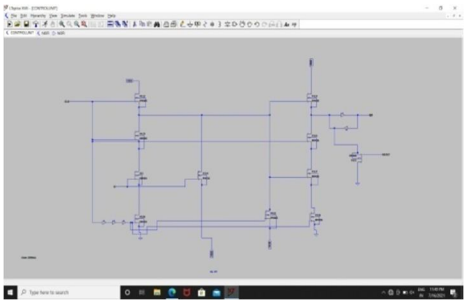


Fig. 6 Circuit diagram of multiplexer

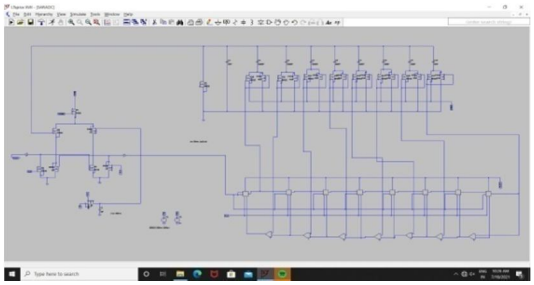
3) Hybrid Latch Flip-Flop


Fig. 7 Circuit diagram of HL flip-flop

The fig. 7 shows the schematic of hybrid latch flip flop which consist of 3 PMOS, 7 NMOS and 5 inverters (3 are in series and 2 are parallel).

E. 8-BIT SAR ADC

A wide range of applications in many different areas such as biomedical applications and wireless communication systems require low power and medium resolution ADC. The SA-ADC has received a great interest among many other ADC architectures because of its efficiency in this kind of applications. The successive approximation register (SAR) is the digital controller circuit which is responsible for executing the binary search algorithm technique. The SAR controller is the last block of the ADC components in which the output of the SAR-ADC circuit will be determined according to the comparator output. Therefore, it has a significant effect on the whole ADC performance which in turns will affect the overall system. The main sources of power consumption in this converter come from the comparator, DAC, and the SAR logic. The power consumption in the SAR logic is how the clock system is one of the most power consuming components. The simulation is done using 90nm CMOS technology in low voltage operation (supply voltage is 1V). It is going to be tested in medium (100 KHz) clock frequency and going to be evaluated using D-flip flop (D-FF) and hybrid latch-flip flop (HL-FF). For an N bit SAR ADC, digital control unit needs at least N flip-flops to perform conversion for ADC. As the need of 32-bit SAR-ADC therefore, an unnecessary SAR employs minimum number of flip-flops. These flip-flops will guess and store the converted result.


Fig. 8 Schematic of 8-bit pipelined SAR ADC

The fig.8 shows the circuitry of 8-bit SAR-ADC which is going to be used as an symbol and will use it as 4n so that the symbol can be used four times to make it 32-bit SAR-ADC.

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F. 32-BIT SAR ADC (in LT-spice XVII using 90nm technology)

Each stage of the schematic contains an 8-bit pipelined SAR-ADC.

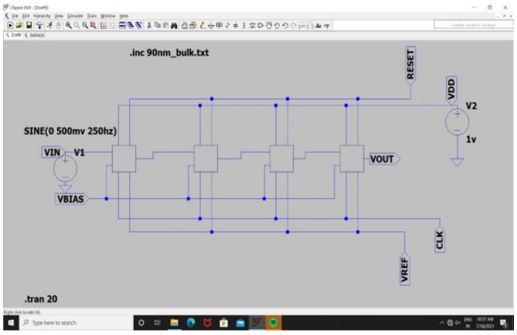
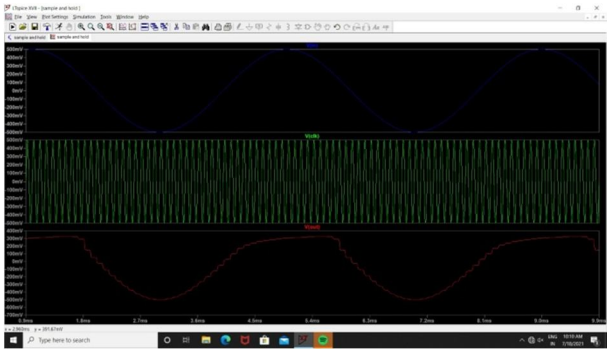
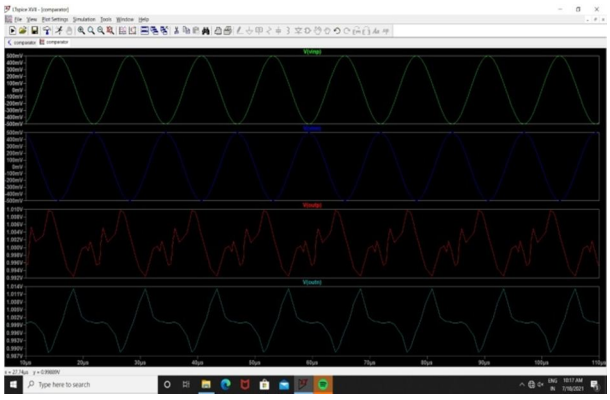


Fig. 9 Schematic of 32-bit pipelined SAR ADC

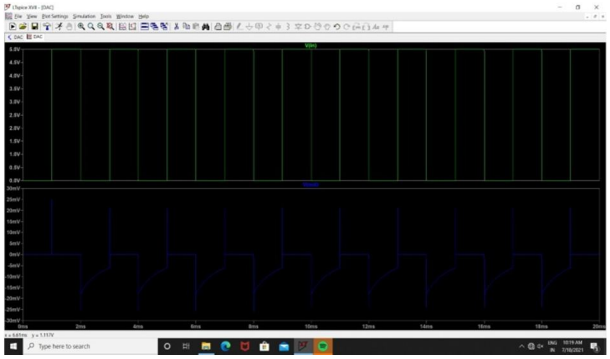
V. RESULTS



a) Output Waveform Of Sample And Hold Circuit

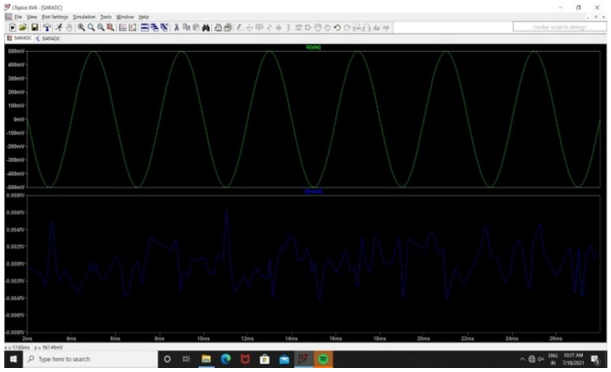


b) Output Wave Form Of Static Cross-Coupled Comparator

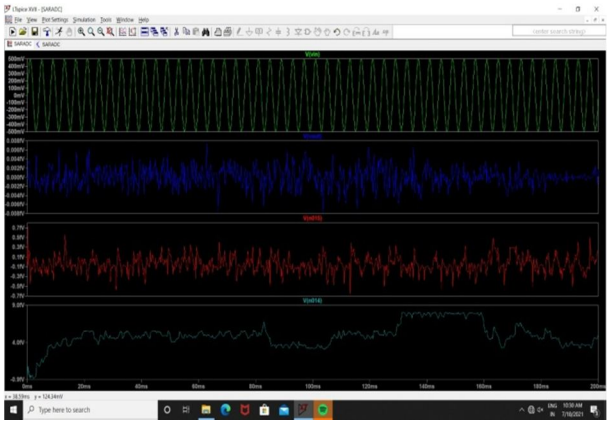


c) Output Waveform Of Dac

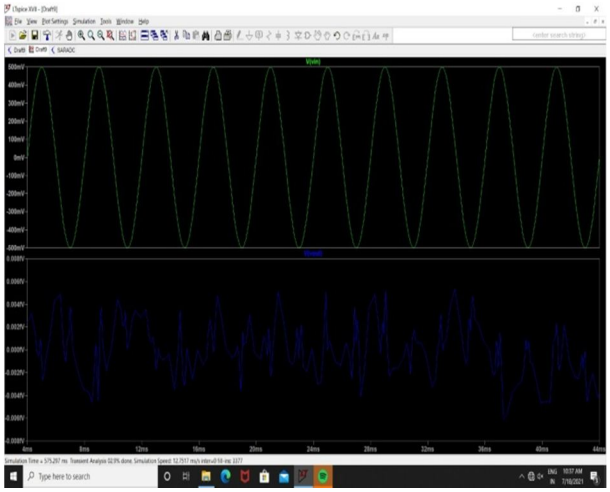
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d) Output Waveform OF 8-BIT SAR-ADC



e) Transient Analysis OF 8-BIT SAR-ADC



f) Output waveform of 32-BIT SAR-ADC

VI. CONCLUSION

The proposed SAR-ADC schematic is simulated using 90nm CMOS technology on LT Spice XVII for a 250 Hz sinusoidal input which fulfills the requirements of biomedical (low-frequency) applications. The sampling frequency is 10 KS/s and the speed is 100 KHz under supply voltage of 1V.This device is suitable for standard CMOS technology VLSI implementation. This ADC is operated at low frequency especially in bio medical applications. SAR-ADC is one of the most popular and easiest approach for designing A/D converters, due to their reasonably fast conversion time, moderate accuracy, low circuit complexity and it is a best choice for low power applications. Thus, the main challenge in designing a SAR-ADC is to succeed in proposing low power, simple and accurate design.

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AUTHORS PROFILE

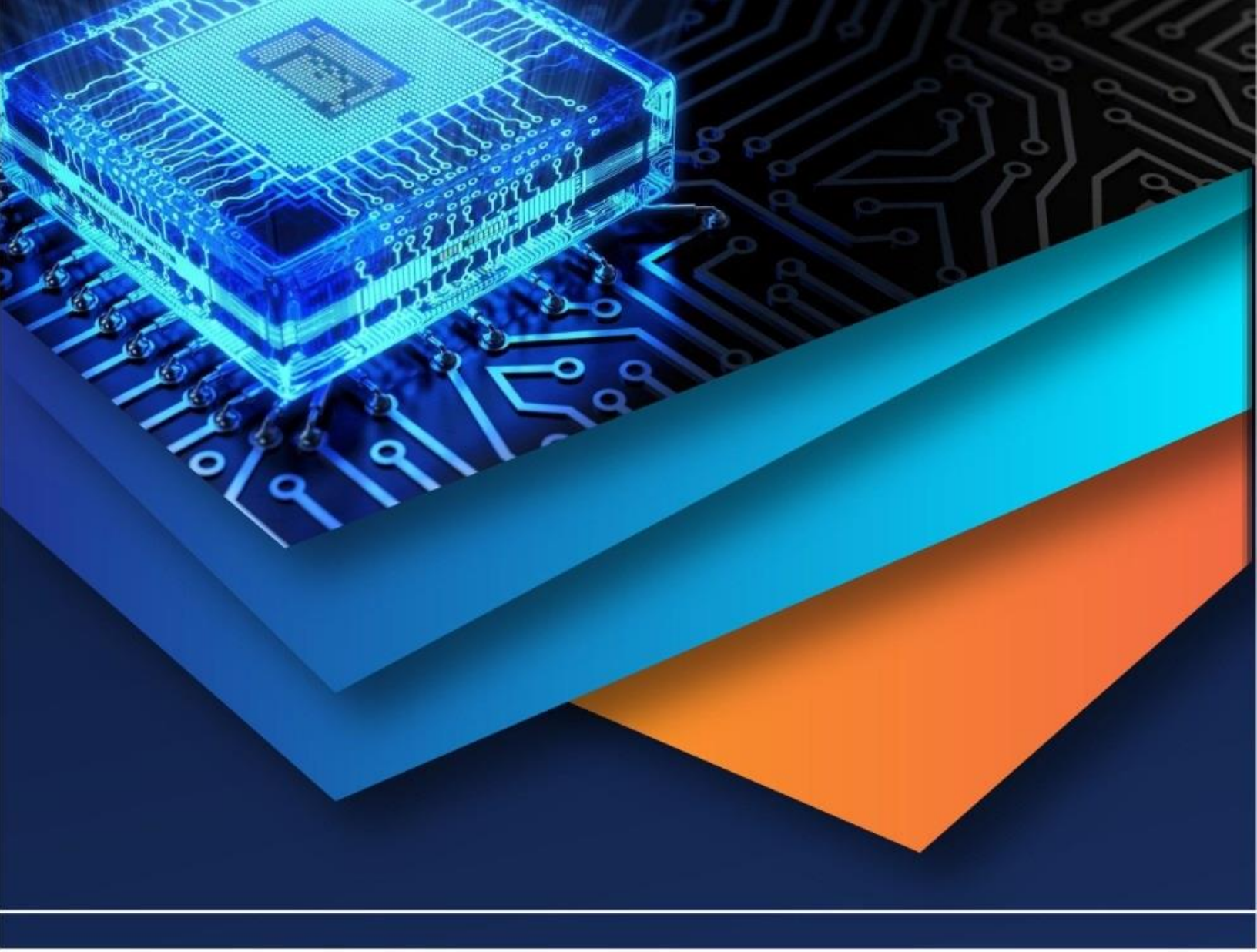
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