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Simulation Analysis of Circuit and Designing of PCB Layout of a CMOS based NAND Logic Gate using Open-Source Software eSim

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Abstract: ***A real world signals are mostly based on Boolean operators. In simple language Boolean operators are logic gates and logic gates are the building blocks of any circuit. There are different types of logic gates like AND, OR, NOT, NAND, NOR, XOR, and XNOR. These all-logic gates are implemented using a Boolean function. And all these logic gates internally are implemented using diodes and transistors. And when we implement all these logic gates using transistor and diodes then it comes under logic families. In this paper we are going to do the analysis of NAND GATE using CMOS in 180 nm technology and has also designed its PCB layout. We are going to carried out the whole simulation of the proposed design of NAND Gate in eSim (Electronic Simulation) Software which is an EDA tool. And by changing the different values of inputs of NAND Gate we are observing respective output in simulation process of eSim.***
Keywords: simulation, PCB, NAND, CMOS, eSim

I. INTRODUCTION

Logic family is a type of method which is used for implementation of different types of logic gates in VLSI industry. And logic family is classified into two types that is Bipolar Logic Family and Unipolar Logic Family. Bipolar logic family is classified into two types Saturated and unsaturated logic family. And Unipolar logic family is classified into three types P-MOS (P- channel Metal Oxide semiconductor), N-MOS (N-channel Metal Oxide semiconductor) and CMOS (Complementarily Metal Oxide Semiconductor). As we know that CMOS consist of both p- channel and n-channel MOSFET (Metal Oxide Semiconductor Field Effect Transistor) which are connected in series with each other. For implementation of NAND Gate using CMOS, we have to connect Both P-MOS in parallel with each other and N-MOS in series with each other. Let us name the first P-MOS as M1, Second PMOS as M2 and one N-MOS as M3, and other N-MOS as M4. Vcc1 is the high voltage and GND is taken as Ground. As in this circuit we are going to do the analysis of 2 input NAND Gate using 180nm technology which is performed in eSim. There are two input A and B which is going into both P-MOS and N-MOS. And output of this proposed NAND Gate is obtained at Yout.

II. SYSTEM DESCRIPTION

Digital circuits are the circuit which takes a combination of different number of inputs into it and providing an output. Digital circuits use basic logic gates to make any type of circuit. It uses active and passive components for the implementation of any type of digital circuits. There are several different types of circuits which are there in digital circuits. The most commonly known circuits are combinational circuits and sequential circuits. Combinational circuits are those circuits which provide their output depends on the input present at that time. These are memoryless circuits. Example of combinational circuits are Half adder, multiplexer, demultiplexer, etc. Sequential circuits are those circuits which provide their output depends on the input present at that time and it also depends on the past output. These circuits have memory elements in them. Example of sequential circuits are registers, counters, etc. There are so many types of number system which we are using in digital circuits. And Binary number system is from one of them. Binary number system consists of only two values 0 or 1, where using 0 does not always means that there is no value the value is given zero only but it means that low value is provided and similarly for 1 it does not mean that only 1 is provided but it means that any high value is provided. So in binary number system we are only dealing with high as well as low value and while talking about logic family high value can be anything in volt and similarly low value can be any low value in volt. Since, everything is working in the form of digital everywhere either you see it in the machine language of computer systems as it also uses only 0 and 1 so, for understanding the computer language we need to learn digital then only we can understand the language of computer otherwise not. or you can see it in digital watches, etc. There are so many advantages also of digital circuits as compare to analog. These advantages are:

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1) It is faster than analog circuit.
2) It is almost noiseless or we can say that digital circuits have very much less noise as compare to analog.
3) It's switching time is also very much faster than analog.
4) They are not very much expensive.

Applications of digital circuits are:

a) In rocket science.
b) It is also, used in communications.
c) It is also used in traffic lights.
d) It is also used, where we need to count the total number of people's by using counter. For example: In any book fair, if we need to count that how many people's come in the fair then, there we used counters which comes under digital circuits.
e) As converter digital to analog converters (DAC) and vice versa.

A. *NAND Gate*

It is the Universal Logic Gates means we can make any of the logic Gate using NAND Gate. The NAND Gate has two or more than two input signals but only one output signal. If any one of the inputs of NAND Gate is zero (0) then output will be one (1). Or we can also say that if both of the input are one (1) then output will be zero (0). It is basically a complemented or inverted form of AND Gate. And it is called NAND Gate because it is formed by the combination of AND and NOT Gate.

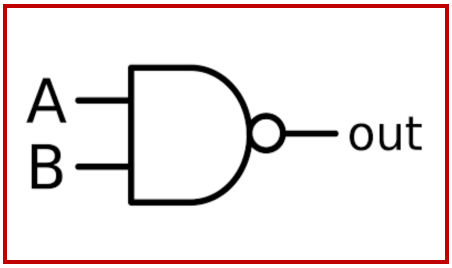


Fig. 1: 2-input NAND Logic Gate

TABLE I
Truth Table of 2-input NAND Logic Gate

Input (A)	Input (B)	Output (Yout)
0	0	1
0	1	1
1	0	1
1	1	0

B. *CMOS Technology*

As we know that, CMOS is series combination of P-MOS and N-MOS. Whatever input we will give that will come in complemented form. CMOS consist of Two Network i.e., PUN (Pull UP Network) and PDN (Pull Down Network). Pull UP Network consist of P-MOS and Pull-Down Network (PDN) consist of N-Mos Network. PUN is complemented or inverted of PDN. All passive components which are used in electronics industry are so much large that it has to be embedded on the board so, we use VLSI technology, so that it can be easily designed. That's why Nowadays, CMOS become very much useful in all electronics industry of VLSI domain. It is the method which is used for the manufacturing of most of the IC's (Integrated circuits). And it is used in Analog signals, Digital signals and mixed signals ICs which are fabricated using CMOS in the industry. Let us first understand a concept of N-Mos and P-Mos that how it is connected when we have mathematical equation is given. So, N-MOS should be in parallel when it is (+) sign and N-MOS should be series when it is (-) sign. Similarly, P-MOS is just opposite of that N-MOS i.e., P-MOS should be in series when it is (+) sign and it should be in parallel when it is (-) sign.

1) *P-MOS:* When input is given Low, P-MOS will come in ON state and it will act as closed/short circuit. And When input is given High, P-Mos will come in OFF state and it will act as open circuit.
2) *N-MOS:* When input is given Low, N-MOS will come in OFF state and it will act as an open Circuit. And When input is given High, N-MOS will come in ON state and it will act as a closed/short circuit.

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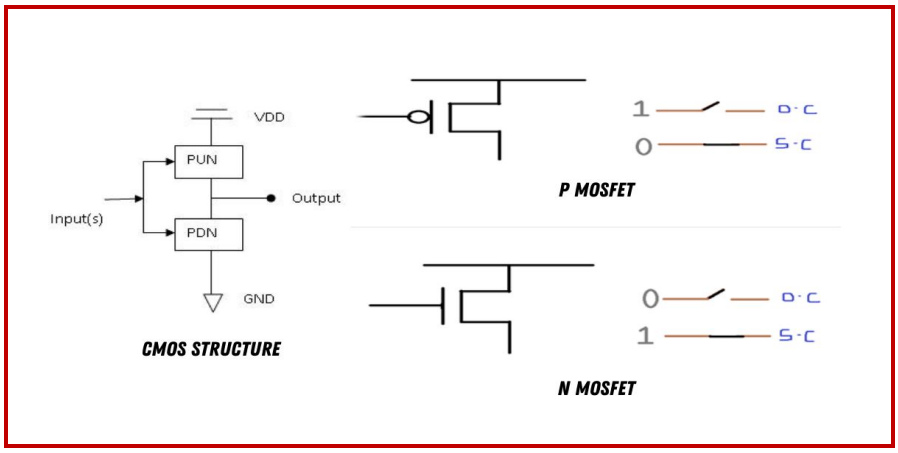


Fig. 2: CMOS Technology

III.REALIZATION OF CMOS BASED NAND GATE

For implementation of NAND Gate using CMOS, we have to connect Both P-MOS (BS250) in parallel with each other and N-MOS (2N7000) in series with each other. After opening of eSim software, we created a. new project by giving any project name then, a window of schematic is open where we have to draw a circuit of NAND Gate using CMOS in 180nm technology So, the components which are required in designing of NAND Gate circuit are resistors, dc voltage, pulse voltage, ground, global label, plot, connecting wire, BS250 and 2N7000. Vcc1 is basically the DC voltage, it means that it is the voltage which is provided at drain terminal of MOSFET. Global label is used for giving input name as well as output name in NAND Gate circuit. Ground is used for giving ground in the circuit or you can say for giving neutral to the circuit. Plot component is used for plotting the graph. Pulse voltage is the voltage which is used to provide the pulse signal in both the input of NAND gate. We have connected the resistors in parallel of both pulse voltage which is provided in the inputs of NAND Gate so, that it behaves as a load in the circuit. Now, for implementation of NAND Gate first select two BS250 and two 2N7000 from the place component tool and search for the BS250 and 2N7000 in the schematic window and we then connected both BS250 in parallel with each other using connecting wire tool and both 2N7000 in series with each other. Similarly, select all other required components from the place tool component and arrange all those components in such a way as it is shown in fig.7. Now, also connect the ground in all the places at negative terminals and supply voltage is also connected. Now select the three plot components from the place component tool and connect all the plots at input as well as at output. And after connected the plot now connect the global labels at both the input and output and give name to input as A input and B input and output name as Yout. When we have completed the whole circuit of NAND Gate then, we have given the name to each component according to our wish and also give the respective values of resistors and Vcc1 which is needed for the simulation of circuit .When whole circuit is completed then , we annotated the circuit and then , check for ERC (electrical rule check) after that we have generated a Netlist in by default format at the same path directory in the library of eSim then, goes back to eSim environment and run KiCad to Ngspice and give respective values in the analysis ,source details and also add the respective library in device modelling of BS250 and 2N7000 after that convert it , for simulation we click on simulation tool and then, the respective waveform of input-output of NAND Gate is obtained. This is how the whole simulation process is carried out for the realization of NAND Gate.

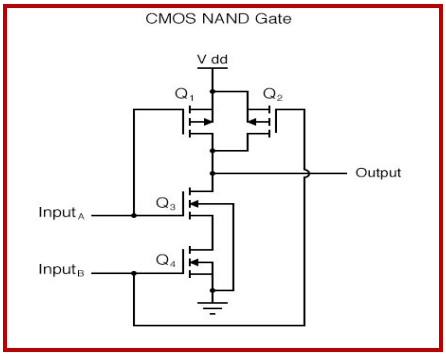


Fig. 3: CMOS based NAND Gate

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IV. SIMULATION RESULT AND PCB LAYOUT

Here, for the realization of NAND Gate PCB we have make a through hole mounted copper layer PCB. Now, we have to do the annotation of the circuit first and then check for ERC (electrical rule check) after that we have to go to CvPcb then, a new window is open in eSim of PCB in which we have to enter all the respective specifications in front of the respective components which we have used for the designing of PCB. Since, we are making the through hole mounted PCB so, we have to add all the specifications by keeping in mind of through hole PCB only. After adding all these respective specifications go back to schematic window of eSim and again do annotation, ERC and after that click on NET list in which we have to generate only the Netlist of PCB in default format. After Netlist is generated go to tools and click on Printed circuit board then a new window opens as a name PCB new then go to read Netlist option and by default the current netlist is selected click ok then your whole circuit come in the PCB window in which each component is aligned on each other. Now, we have to arrange the components in a proper alignment but before that we have to make the border of PCB only, inside which we have to aligned all the components in such a way that no white line (known as air line) should be intersected with each other. We have to make border line of the PCB using Edge cut layer it is one of the layers of PCB which is drawn using the Line or Polygon tool. Now, after making the border line of the PCB and when arrangement of all components in a proper orientation without any intersection of any air line is completed. The next step which we have to follow is to make the track. For making of track layer, we have to use B.cu layer in which B stands for back and cu stands for copper so, B.cu (back copper) layer is used for making track, select track from place option and we can also change the track width according to the specifications of PCB from the design rules option. Now, make track over the air line and connect each component using track. After making the track in PCB now we have to fill the remaining zone. Now, the whole part of the PCB is completed the last step which have to follow is we need to add the dimension of whole PCB so, for adding it select margin in the layer option and then, go to place option after that click on dimension now, we have to make a proper line at the border of PCB for measuring its dimension on the length and breadth side of it. Finally, the whole process of PCB designing is completed.

The working of NAND Gate is as follows: -

1) When Low (0) is given to both input A and input B of N-MOS and P-MOS then both PMOS M1 and M2 comes in ON state and become short circuited. Also, at the same time Both N-MOS M3 and M4 comes in OFF state and become open circuited. As, both P-MOS i.e., M1 and M2 becomes short circuited then it gives Vcc1 at output Yout. Hence, output at Yout comes High (1) {i.e., Vcc1}.

2) When Low (0) input is given to input A and High (1) input is given to input B of N-MOS and P-MOS, then input A goes to P-MOS M1 and also it goes to N-MOS M3 at the same time as there is low (0) input is given in input A, P-MOS M1 comes in ON state and it became short circuited and N-MOS M3 comes in OFF state and it became open circuited. Now comes to input B which goes into P-MOS M2 and N-MOS M4 as there is high (1) input is given in input B, P-MOS M2 comes in OFF State and it becomes open circuited and NMOS M4 comes in ON state and it became short circuited. So, the output which comes at Yout is Vcc1. Hence, output at Yout is High (1) {i.e., Vcc1}.

3) When High (1) input is given to input A and Low (0) input is given to input B of both N-MOS and P-MOS, then input A goes to P-MOS M1 and also it goes to N-MOS M3 at the same time as there is High (1) input is given in input A, P-MOS M1 comes in OFF state and it becomes open circuited and N-MOS M3 comes in ON state and it becomes short circuited. Now comes to input B which goes into P-MOS M2 and NMOS M4 as Low (0) input is given in input B, P-MOS M2 comes in ON state and it became short circuited and N-MOS M4 comes in OFF state and it becomes open circuited. So, the output which comes at Yout is Vcc1. Hence, output at Yout is High (1) {i.e., Vcc1}.

4) When High (1) input is given to both input A and input B of N-MOS and P-MOS then both P-MOS M1 and M2 comes in OFF state and both becomes open circuited. Also, at the same time Both N-MOS M3 and M4 comes in ON state and both becomes short circuited. As, both NMOS i.e., M3 and M4 becomes short circuited then it gives GND at output Yout because both P-MOS M1 and M2 are open circuited at that time. Hence, output at Yout comes Low (0) {i.e., GND}.

The only work which is left now is of the PCB Fabrication. For the fabrication of PCB we need to generate the Gerber file of the PCB. Before generating the Gerber file, we first need to plot it so, for plotting go to PCBnew window file option and in the file option click on plot after it is plotted click on generate drill file now your drill file is generated in the respective folder of NAND Gate in FOSSEE eSim in your c drive and save it there. After Completing saving of drill file just open command prompt window in your system and write gerbview in that then, a gerbview window is open in front of you. Then, in gerbview window go to file and there is a option there of load Gerber file click on it then it opens the c drive of your system then open that same path directory where you just saved the drill file and one by one load each file in gerbview window. When all files is loaded. Our PCB is ready for the manufacturing purpose you can give this Gerber file to any manufacturer then, he/she can print your PCB Board and finally at the end your PCB is now ready to use.

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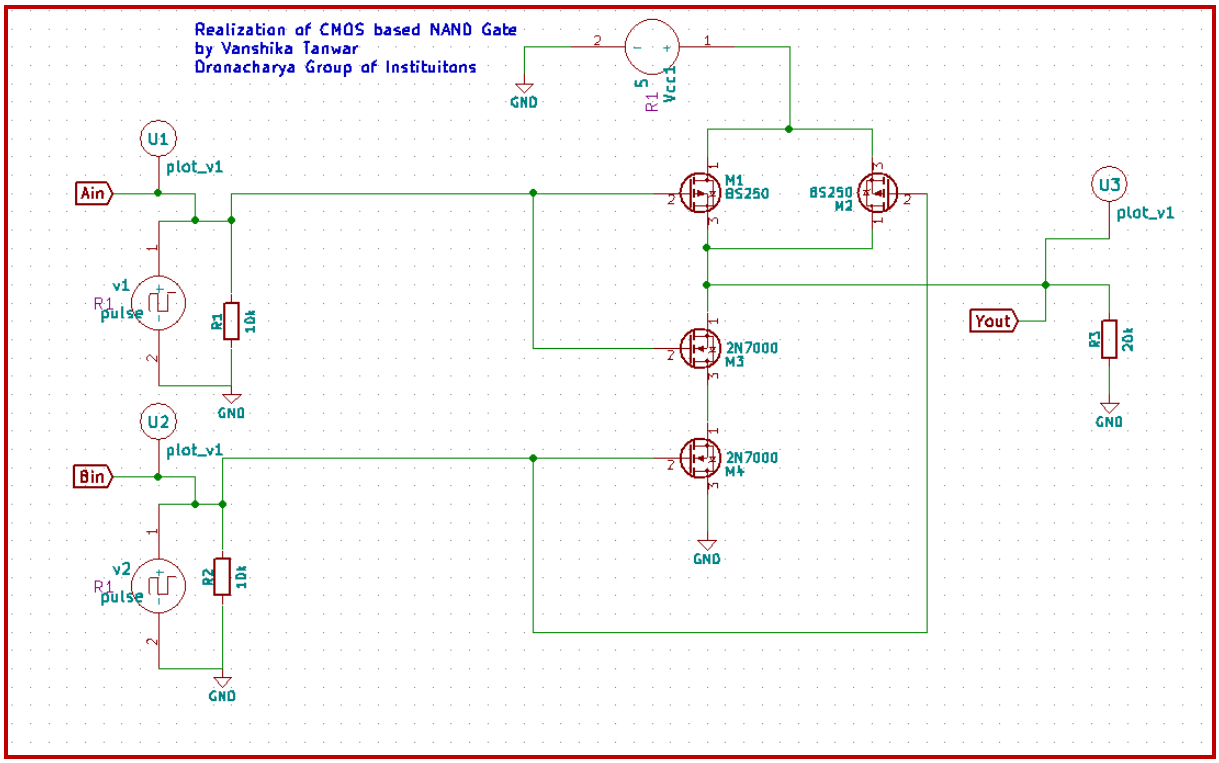


Fig. 4: eSim Schematic of a CMOS based 2-input NAND Logic Gate

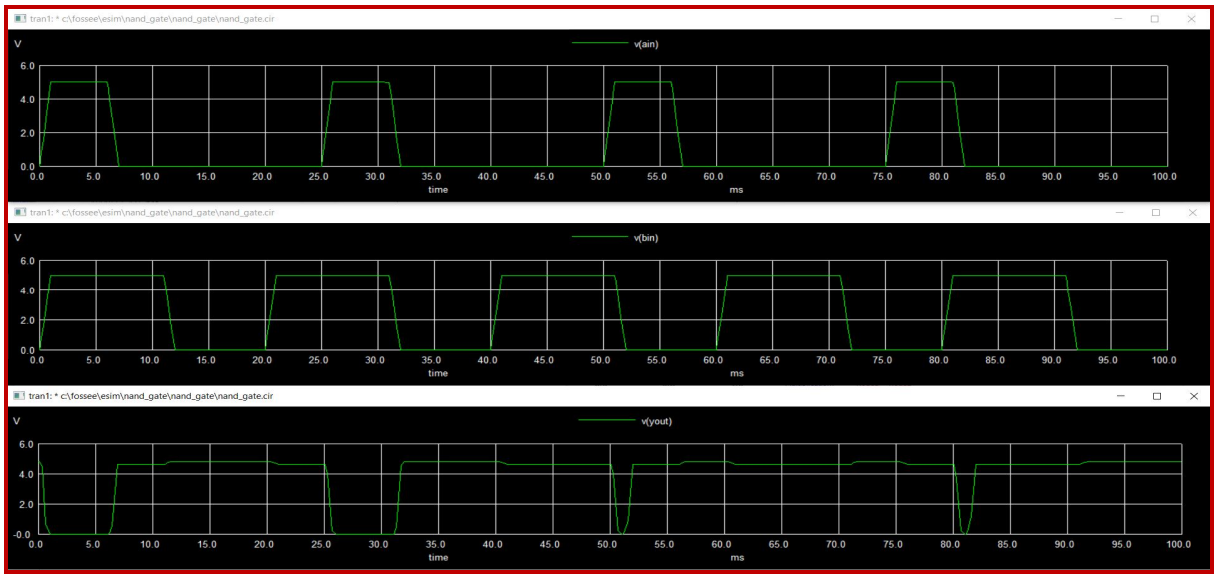


Fig. 5: Simulation Output of a CMOS based 2-input NAND Logic Gate

TABLE II
Output Comparison of a CMOS based 2-input NAND Logic Gate

A	B	M1	M2	M3	M4	Yout	Logic
0 (LOW)	0 (LOW)	ON	ON	OFF	OFF	Vcc1	1 (HIGH)
0 (LOW)	1 (HIGH)	ON	OFF	OFF	ON	Vcc1	1 (HIGH)
1 (HIGH)	0 (LOW)	OFF	ON	ON	OFF	Vcc1	1 (HIGH)
1 (HIGH)	1 (HIGH)	OFF	OFF	ON	ON	GND	0 (LOW)

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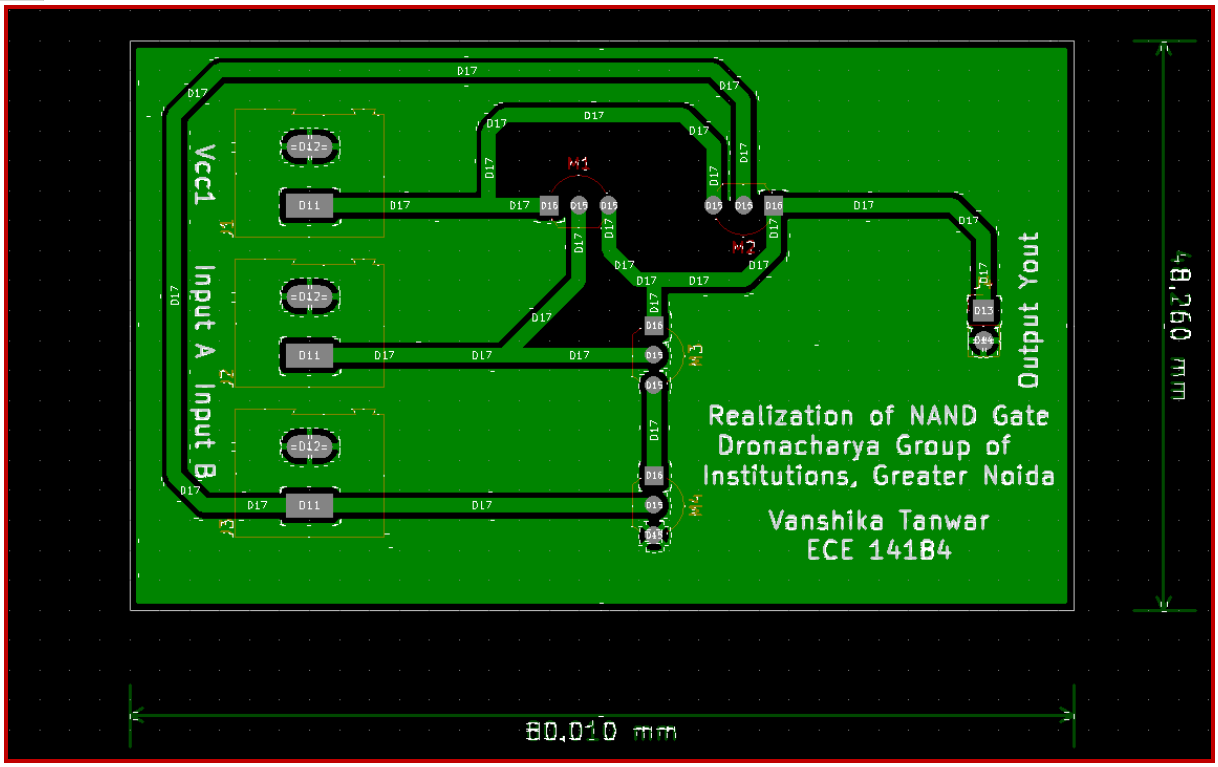


Fig. 6: PCB Layout (gerbview) of a CMOS based 2-input NAND Logic Gate

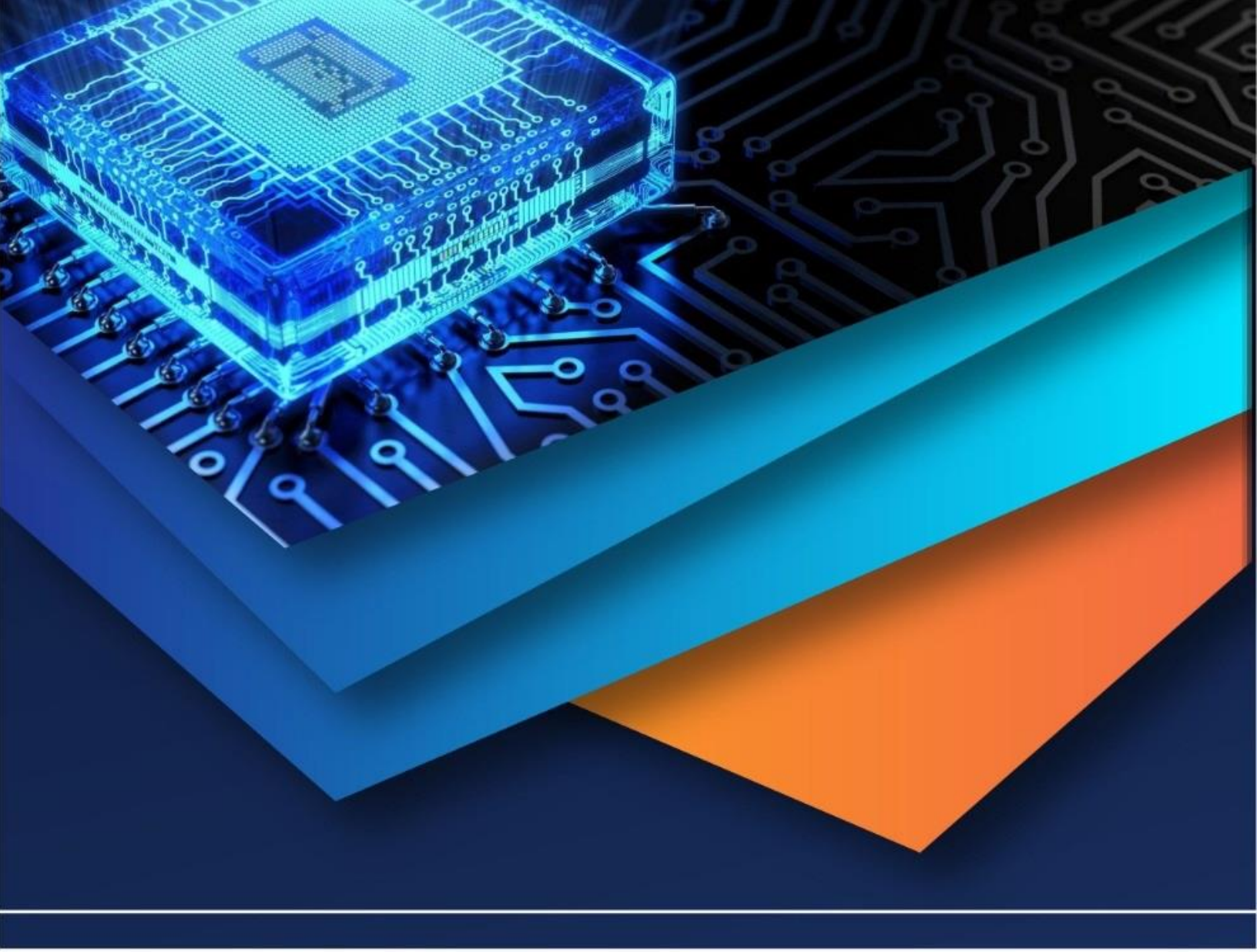
V. CONCLUSIONS

This paper presents schematics, its simulation and PCB layout design of NAND gate using CMOS. NAND gate layout has been designed and simulated using eSim. In the layout of NAND Gate 180nm technology has been used for simulation. Under a condition of Vcc1=5v power supply and it covers the best area and power utilization of the layout. Also, the delay time, rise time and fall time are calculated in simulation. It can be observed from simulation result that NAND gate consumes more power than a fully automatic NAND gate, but some other techniques can be used to reduce the power in the future.

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