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Design of Linear Feedback Shift Register for Low Power Applications

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***Abstract:** This paper presents the design & implementation of the Linear Feedback Shift Register (LFSR) using the Mentor Graphics tool in 90nm technology. LFSR's have a wide variety of applications. They are used in pseudo-random variety generation, whitening sequences and pseudo-noise sequences. MOS current-mode logic (MCML) and Dynamic current-mode logic (DYCML) are employed to design an LFSR. MCML is widely used in high-speed applications and these MCML circuits are based on current steering logic. The advantages of the MCML method are that they have high noise immunity due to their differential nature of inputs. The disadvantage of MCML approach is static power dissipation. To overcome these issues of MCML logic, Dynamic CML logic is used. Its advantages include low static power dissipation and high performance. This paper shows the comparison results of CMOS, Dynamic CML and MCML designs in terms of delay, power and transistor count.*
***Keywords:** MCML, DYCML, LFSR.*

I. INTRODUCTION

A shift register is a sequential circuit that stores or shifts binary data. Input bits which are loaded into the sequential logic device are then shifted to its output at each and every positive or negative edge of the clock cycle. Data bits may be fed to the sequential device either serially from left to right or from right to left, or at the same time in a parallel manner. A LFSR is a shift register in which a few outputs are connected or fed back to the input by some logic gates. Most commonly, the XOR gate is used. LFSR is used to generate pseudo-noise, pseudo-random numbers, whitening sequences & fast digital counters [4].

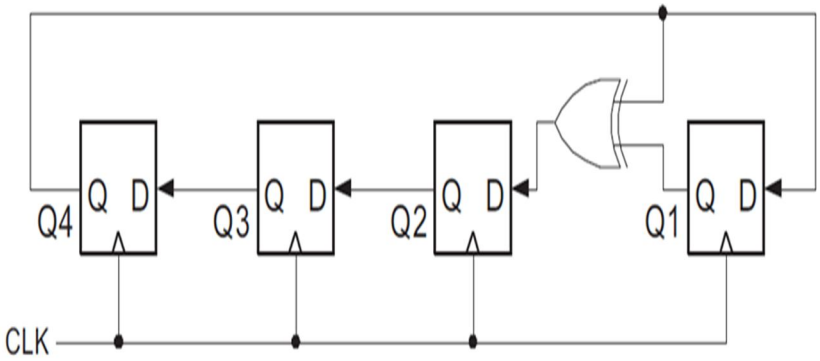


Fig. 1 4-bit LFSR using XOR.

The above shown LFSR counts (2^4 -1) different non-zero-bit patterns. In general, it counts (2^n -1) non-zero-bit patterns where 'n' is number of flip flops.

The main objective of this work is to design an LFSR using CMOS, MCML and Dynamic CML methods. MCML is a new logic style for mixed-signal applications with low power. Its high-speed switching, and the reduced output swing voltage correspond to its high performance, low-noise features and low power consumption. The MCML circuit consists of three elements: 1) Load circuit 2) Pull-down circuit and 3) Current source. To overcome the disadvantages of MCML logic, Dynamic CML with a dynamic current source is utilized to reduce Static Power Dissipation & obtain high performance.

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II. METHODOLOGY

A. Existing Methods

1) 4-bit LFSR using CMOS Posedge D-FF and XOR.

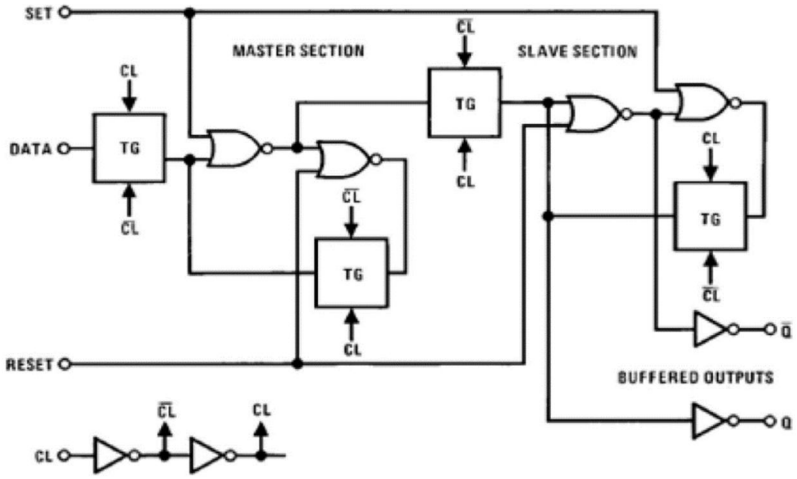


Fig. 2 Posedge D-FF.

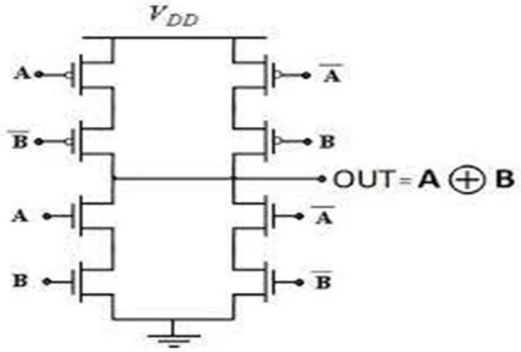


Fig. 3: XOR gate.

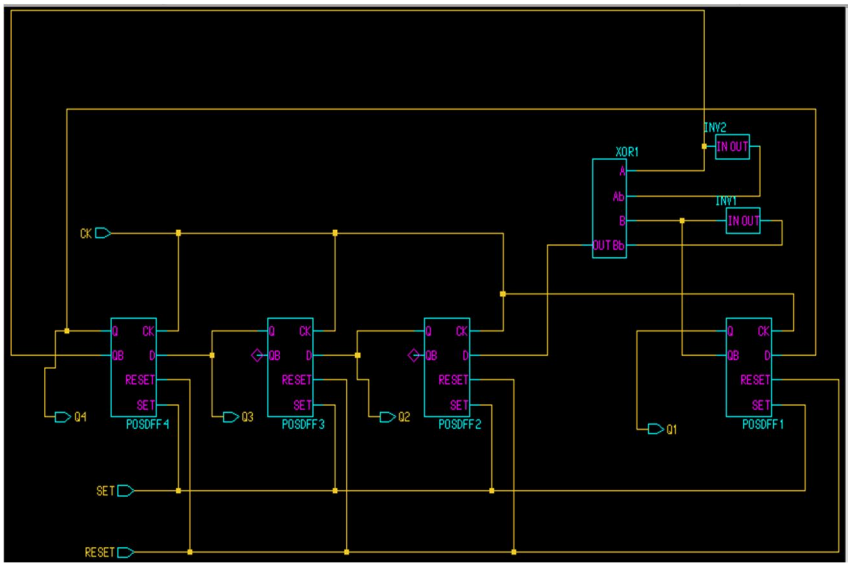


Fig. 4 Schematic of CMOS 4-bit LFSR.

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2) 4-bit LFSR using MCML.

MCML LFSR is designed using MCML-XOR and MCML D-FF.

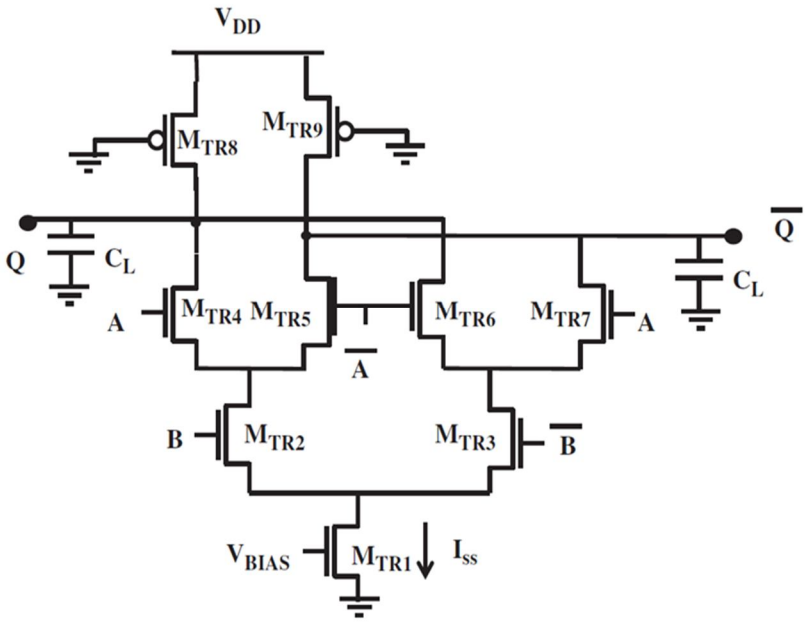


Fig. 5 Circuit diagram of MCML-XOR.

In the above figure, the MCML-XOR with two differential inputs, A & B, is depicted. To accomplish the logic function, it has two stages of source-coupled transistor pairs, as well as a constant current source M_{TR1} to generate 'I_{SS}' bias current. The input B activates the upper-level transistor pairs M_{TR4}–M_{TR5} and M_{TR6}–M_{TR7} by driving the transistor pair M_{TR2}–M_{TR3}. When input B is high, transistor M_{TR3} is turned off, and the I_{SS} bias current passes from M_{TR2} to M_{TR5} or M_{TR4}, depending on input A. When input B is low, however, the I_{SS} bias current travels through M_{TR3} transistor and is directed to either M_{TR7} or M_{TR6} transistor.

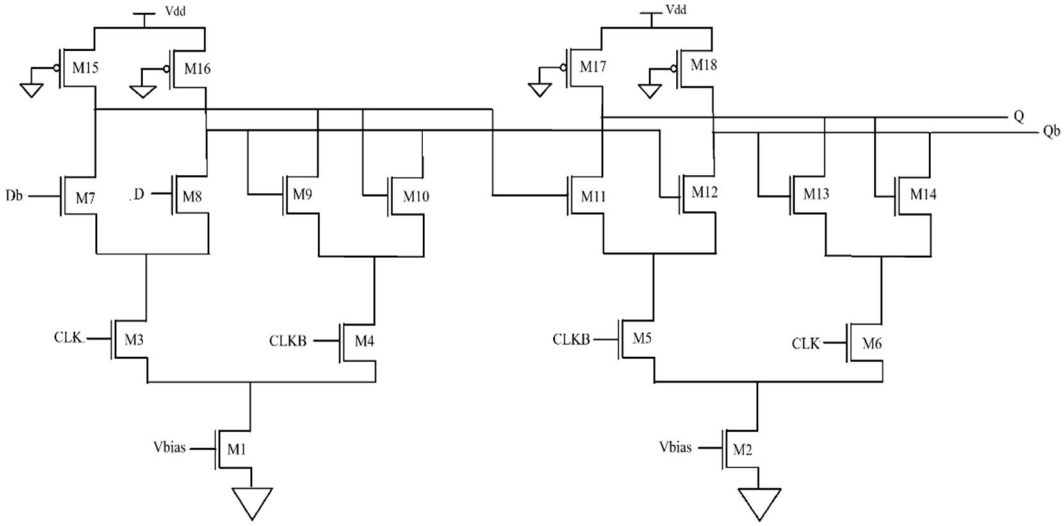


Fig. 6 Circuit diagram of MCML D-FLIPFLOP.

The operation of the above circuit is as follows: Current Mode Logic (CML) comprises of a hold stage and a sample stage; the differential pair transistors are controlled by the complementary clock signals. When the clock signal is high, the current flows through tracking pair & when the 'clk' signal is low, current passes through the storage pair. When input data 'D' is high, current flows through one branch and the other transistor is off, which means there is no current flowing through it and the hold pair is activated when 'CLK' goes low.

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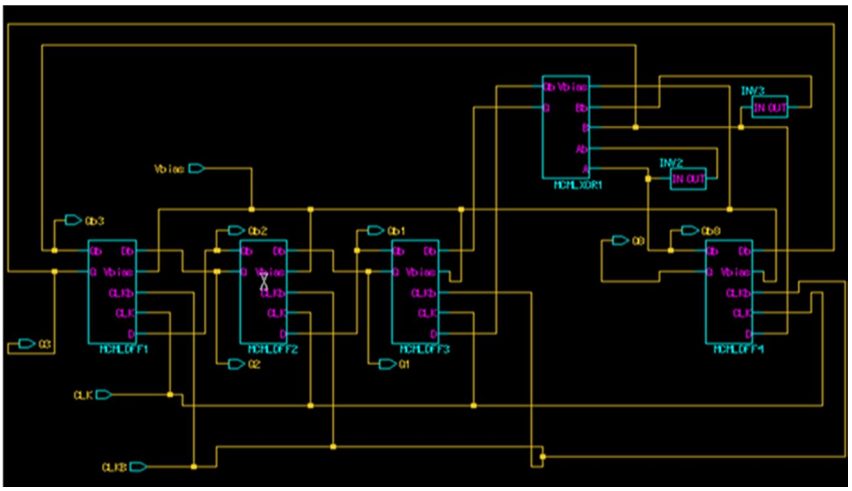


Fig. 7 Schematic of MCML 4-bit LFSR.

B. Proposed Method

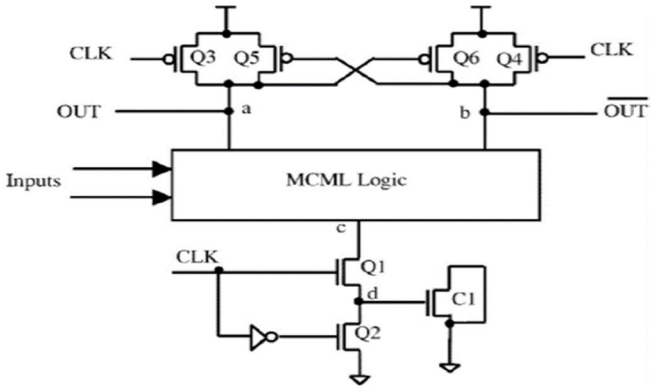


Fig. 8 Dynamic CML architecture.

The explanation of the above figure is as follows: when the 'clk' is low, Q4 and Q3 transistors will turn ON, charging up the output nodes respectively. The Q1 transistor remains off, Q2 discharges C1 to GND, and during the high phase of the clock, Q1 will be ON, which creates a current path between the output nodes and the C1 capacitor while the transistors Q4, Q3 & Q2 will turn OFF. The Q5 & Q6 transistors help in evaluation & also help to maintain the logic levels [4]. Q1 & C1 together form a dynamic current source, which in turn improves the performance of Dynamic-CML.

Following the above shown Dynamic CML architecture, Dynamic CML based d-flipflop & xor circuits are designed similarly as MOS current mode logic-based d-flipflop and xor.

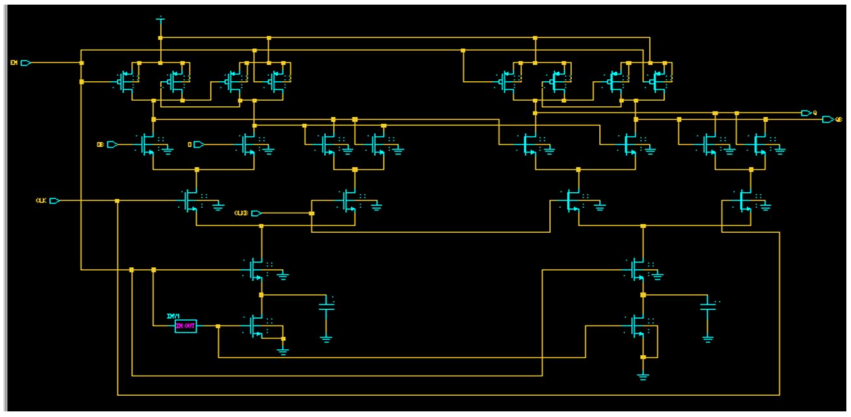


Fig. 9 Dynamic-CML D-FLIPFLOP.

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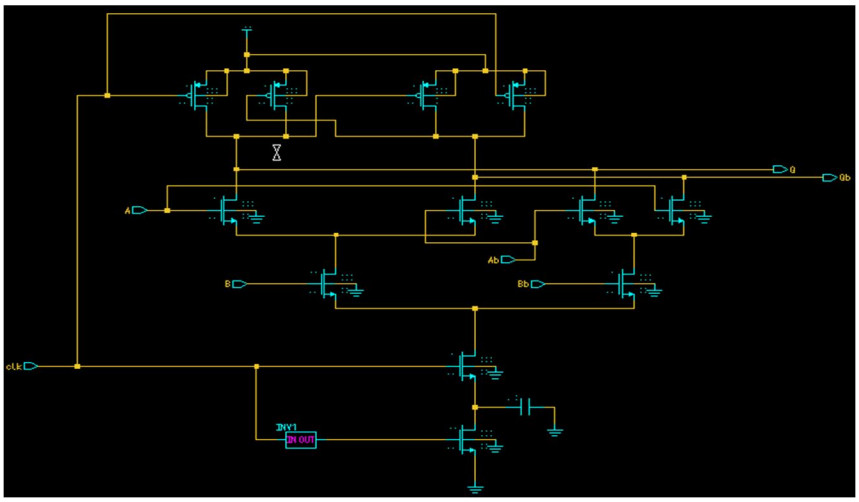


Fig. 10 Dynamic-CML XOR.

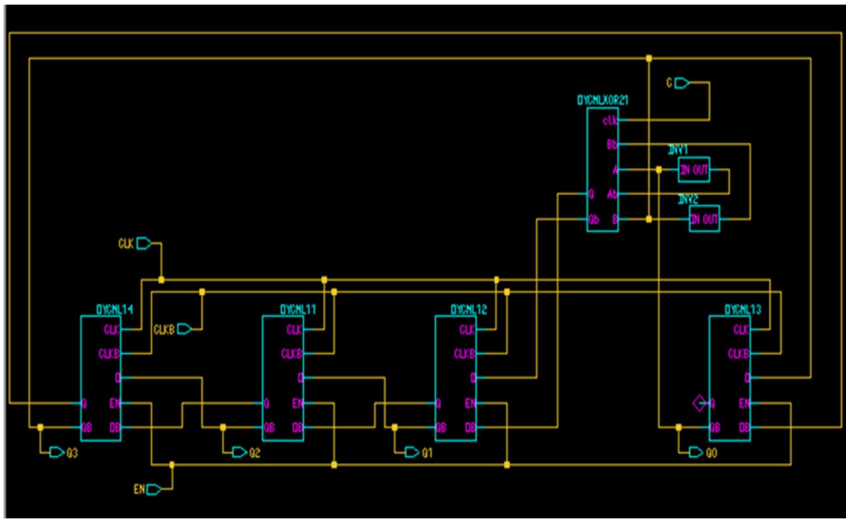


Fig. 11 Schematic of DY-CML 4-bit LFSR.

III. SIMULATION RESULTS

The Schematics of CMOS, MCML and DY-CML based 4-bit LFSR's are simulated and their transient responses are analysed using Mentor Graphics tool.

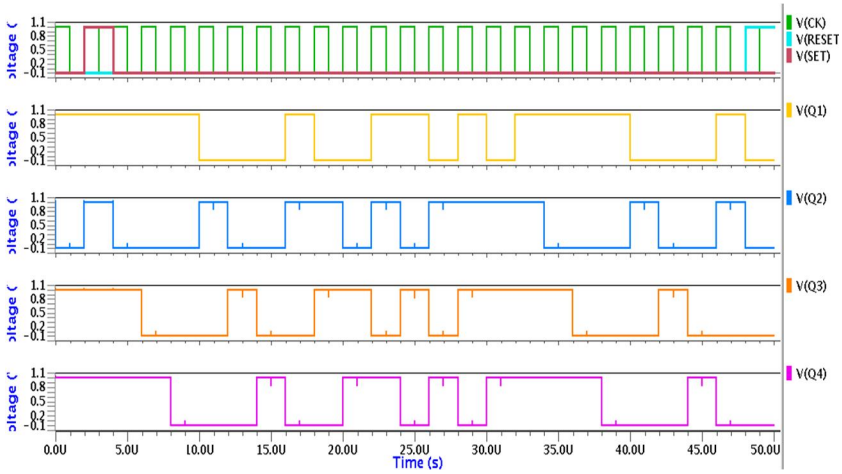


Fig. 12 Transient analysis of CMOS 4-bit LFSR.

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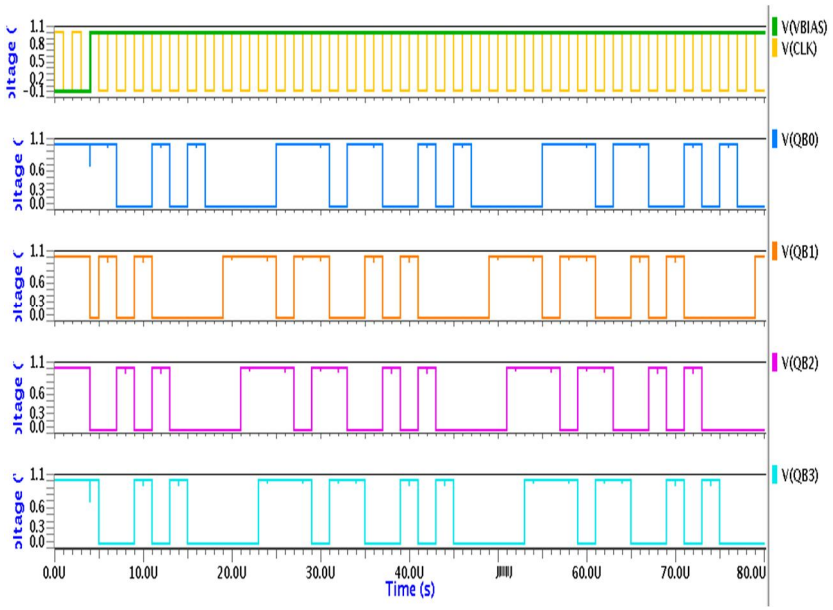


Fig. 13 Transient analysis of MCML 4-bit LFSR.

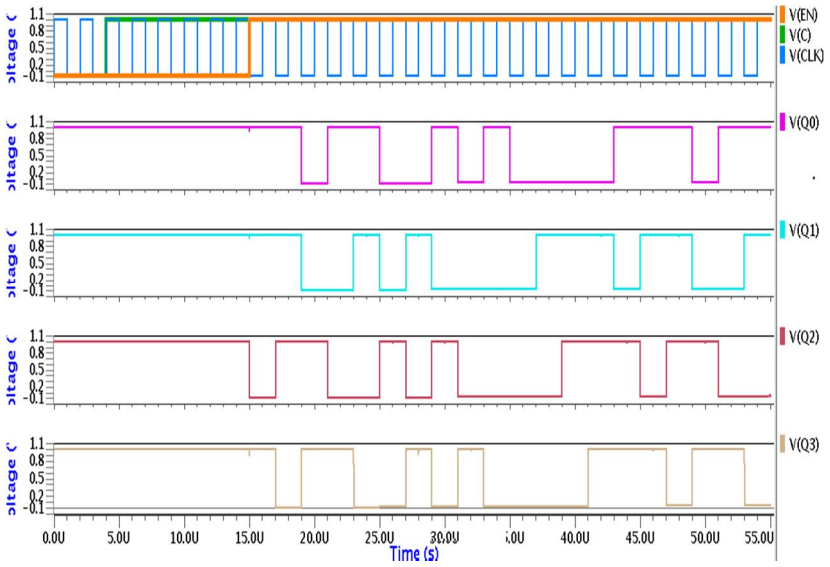


Fig. 14 Transient analysis of DY-CML 4-bit LFSR.

Table 1: Comparison of 4-bit LFSR's.

Designs	Power (nw)	Delay (ps)	Transistor count
CMOS 4-bit LFSR	69.5067	342	172
MCML 4-bit LFSR	26.1872	207	85
DY-CML4-bit LFSR	22.4503	458	122

IV. CONCLUSION

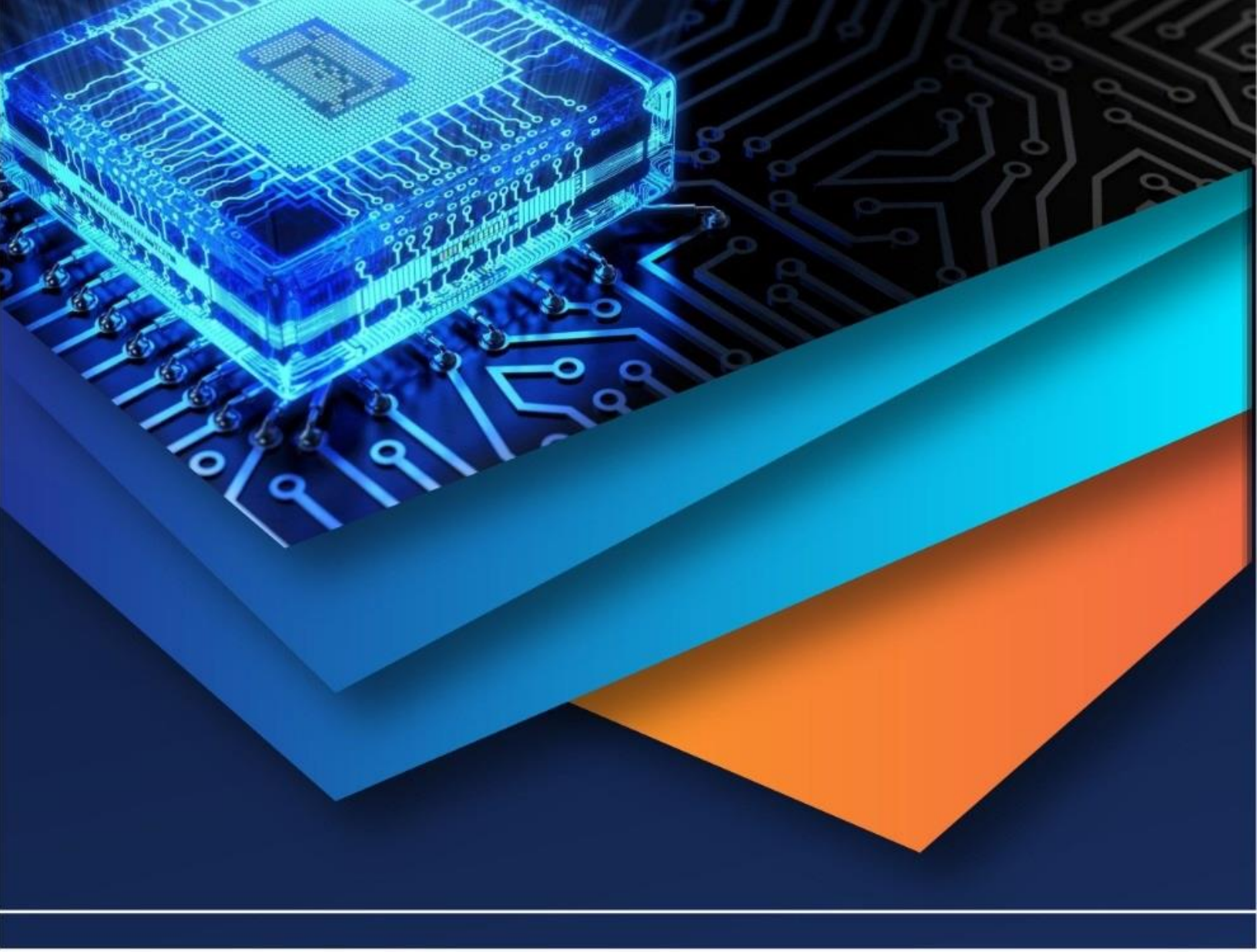
This paper proposes the design of a 4-bit LFSR using CMOS, MCML and DY-CML methods. The MCML method has the advantage of low power and high performance. The advantage of DY-CML method is to decrease static power by using a dynamic current source. All simulations are accomplished on Mentor Graphics (90nm technology). From table 1, we notice that though number of transistors is higher in the DY-CML method, the overall power difference between MCML and DY-CML methods is **3.7369nw**, which indicates that Dynamic CML is more suitable for low power applications when compared to CMOS and MOS current mode logic.

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