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Closed loop analysis of Dual Bridge Converter with 4- levels

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Abstract: ***A dual bridge (DB) LLC resonant converter for dc-dc conversion with closed loop is proposed in the system. The model is capable of delivering very low voltage, with a variable input dc fluctuations in the source side. The new PWM technique used helps the bridge output robust. The proposed model works only in 4 modes of operation. DB LLC converter uses different phase shift for each individual switches with different duty ratios. The model is simulated with 160V/200V DC input and 24V output with 20A i.e. 480W is provided to verify the operation.***
Keywords: Dual Bridge, LLC resonant converter, Closed loop operation, Boost converter.

I. INTRODUCTION

A novel dc-dc dual bridge LLC converter with wide range of input and output voltage is proposed in this project. The proposed model is composite skeletal structure of buck-boost converter and LLC converter. The converter helps in operation in high voltage which decreases the high frequency transformers losses. Converter operation reduces the resonant current which helps in higher turns ration for transformer. The model used different phase-shift modulation gains MD at different input voltages by using Pulse width modulation. The observations are concluded by simulating a prototype converter with 100V-200V DC input and 480W (24V / 20A) output. The converter operates at a fixed higher frequency so that the input regulation is maintained in limit. This also reduces the loss in the converter. The range of input purely depends on the inductor. Therefore, the voltage range is in given range.
In a typical dual bridge the operation of a single cycle has 6 steps i.e. 4 HW and a 3FW. The proposed model has only 2 HB and 2 FB operation. So, we use only 4 levels of operation.
The model can maintain constant output voltage for drift disturbances in the source side. The model helps in designing of charging circuits for batteries. Dual bridge LLC converter is capable of varying the output power from 1 to 4 times the half bridge power. This feature is very helpful in real-time applications. As, the proposed model helps in delivering 3-phase power in just single phase supply.

II. DESIGNING THE PROPOSED MODEL

A. Topology

The Figure 1(a) shows the basic LLC Dual bridge converter. Two capacitors are used to shift the amplitude of the input voltage to half, which is used in half bridge operation. During half bridge operation the switches Q1,Q5 or Q2,Q6 pairs of switches are used. In half bridge mode only one of Q5,Q6 are used because as the switches we use have built in anti-parallel diode. This helps in conduction in reverse direction. Whenever Q5 is triggered Q6 anti-parallel diode is helpful in current conduction and vice versa. Figure 1(b) shows the operation of half bridge. Where the output voltage is only half the input. During the full bridge Q1,Q4 and Q2,Q3 are triggered in operating sequence. The three-element resonant tank is composed of L_r, C_r, and L_m. The LC resonant frequency is denoted as fr=1/(2*π*sqrt(L*C)).

B. Operating Principle

The operating of proposed DB LLC has total of 10 stages in two cycles. These can be divided into 5 of each cycle. Where the stages are symmetrical in each cycle. From figure 2 we can conclude that the stages are from t_0 to t_5 in first cycle.

1) *Stage 1[t_0,t_1]:*Q5 has been conducting before this stage, Q1 and Q4 are turned on at t0. During this time interval, the converter operates in the FB mode, and the resonant tank voltage VAB equals the input voltage Vin. The primary resonant current i_{Lr} is sinusoidal due to the resonance between L_r and C_r. Because the magnetizing inductor voltage V_{Lm} is clamped at nV_o as shown in figure 2, where n is the turn ratio and V_o is the output voltage, the magnetizing current i_{Lm} is increasing linearly. The rectifier diode DA is conducting, and the difference between i_{Lr} and i_{Lm} is transferred to the output stage.
2) *Stage 2[t_1,t_2]:*At1,Q4 is turned off .During this time interval, the primary resonant current i_{Lr} begins to charge C4 and discharge C3 and C6. The drain–source voltage of Q5 is zero because it is kept conducting during this period. When the drain–source voltage of Q4 increases to $V_{in}/2$, the drain–source voltage of Q6 decreases to zero and ZVS turn ON of Q6 can be achieved until the driving signal comes. The resonant tank voltage V_{AB} during this time changes from V_{in} to $V_{in}/2$.

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3) *Stage 3[t_2,t_3]:*Q6 is turned on under ZVS at t2, and Q1, Q5, and DA are still in on-state. During this time interval, the converter operates in HB mode and the resonant tank voltage V_{AB} equals to $V_{in}/2$ as shown in figure 2. The magnetizing voltage V_{Lm} is still clamped to the output voltage, and the magnetizing current i_{Lm} keeps on linearly increasing. And the operation of this stage is similar to stage 1, only the amplitudes of voltage across the resonant tank are different.
4) *Stage 4[t_3,t_4]:*During this stage, the converter is still operating in HB mode and the resonant current i_{Lr} equals to magnetizing current i_{Lm} and the magnetizing inductor Lm starts to resonate together with Lr and Cr instead of being clamped. The rectifier diode DA is turned off, with ZCS avoiding the reverse recovery. Since output is separated from primary the power to the load is only supplied by the output capacitor Co. And the resonant current i_{Lm} during this stage can be called circulating current , which is not beneficial for efficiency.
5) *Stage 5[t_4,t_5]:*At the moment of t5, Q1 and Q5 are turned off. During this dead-time interval, C1, C4, and C5 are charged by the resonant current and their drain–source voltages increase. Correspondingly, C2 and C3 are discharged until their body diodes conduct and ZVS turn on for switches Q2 and Q3 can be achieved subsequently

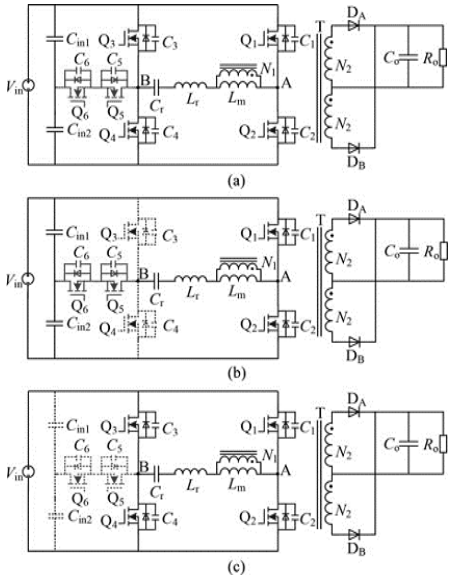


Figure 1 a) Dual Bridge LLC converter b) Half bridge operation of Dual Bridge LLC converter c) Full Bridge operation of Dual Bridge LLC converter

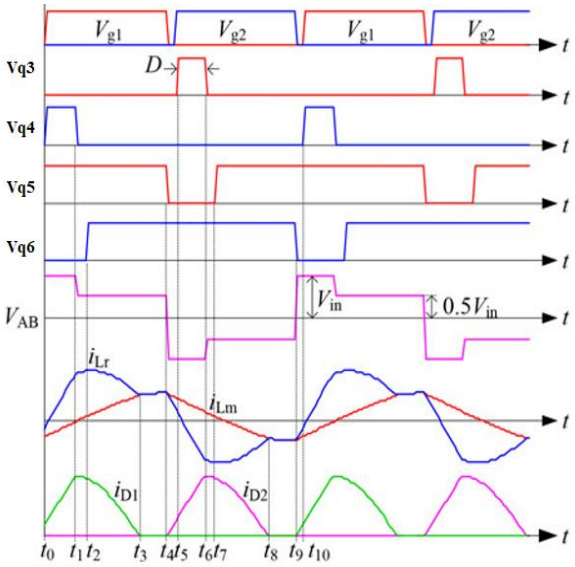


Figure 2 Waveforms of Dual Bridge LLC converter

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III. DESIGN AND ANALYSIS OF THE DUAL BRIDGE CONVERTER

A. Voltage Gain

There are 2 modes of operation Half Bridge(HF), Full Bridge (FB) only as shown in Figure 4. At heavy load the operation is mostly FB because the average should be met with the load. So,we can even find the maximum output voltage even.

The voltage gain for different gains is given as $M_{dc.}$

M_{dc} = 1 for FB

0.5 for HB.

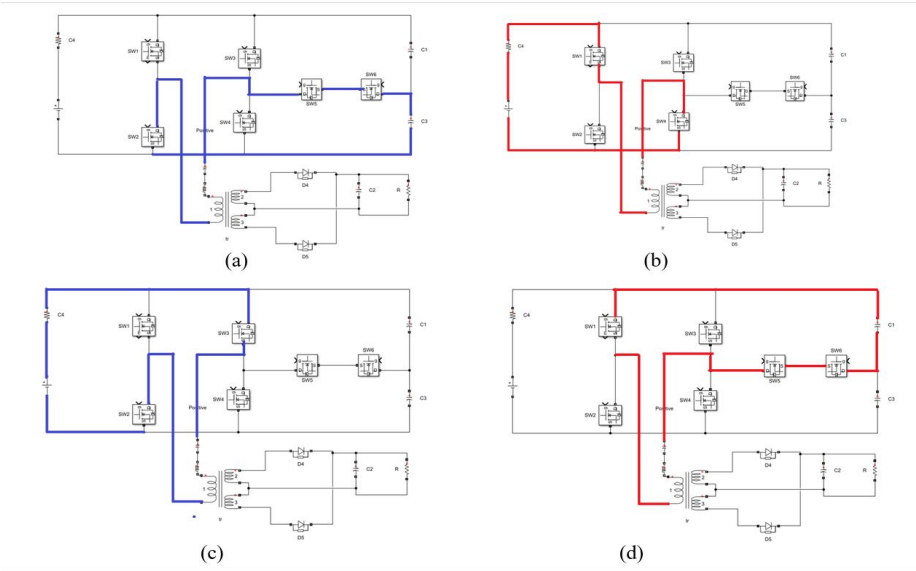


Figure 3 Operation of the Converter (a) during positive Vdc (b) during 0.5Vdc (c) during -0.5Vdc (d) during -Vdc

B. Voltage Calculation of the Bridge in Open Loop Mode

During the operation of Q3,Q2 the voltage across load is V_{dc} ,during Q2,Q6,D5 the voltage is $0.5V_{dc}$. In the similar manner the voltage when switches Q1,Q5,D5 are triggered the voltage is $-0.5V_{dc}$.The pattern repeats for all cycles. It is easy to calculate the average voltage of the output by just finding the area under half the curve. As the output is AC we go for only half cycle.

It given as- V_{avg}= (Vdc*T1+0.5Vdc*(T2-T1))/(T1+T2) Volts.

The value of switch frequency we uses is 100 kHz.

As in the same way we can work for RMS as – $V_{rms}=V_{dc}$* sqrt((T1+0.5(T1-T2))/T1+T2) Volts.

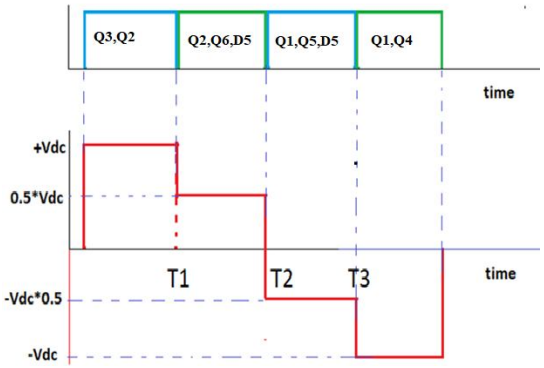


Figure 4 Output voltage waveform

We can observe that the Output voltage is changing with respect to the change in Duty ratio of switches Q3,Q4,Q5,Q6. As we know that switch Q3,Q4 are complementary and Q2,Q1 are independent of voltages. So, for more voltage greater that average we need Q3 to conduct more time and also to get less voltage we need Q6 to conduct more.

This model has minimum of 80V output and maximum of 160V. So, the output varies between these limits. So, to control this we use Pulse width modulation which help in triggering Q3,Q4,Q5,Q6 switches to get optimal voltages.

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IV. PULSE WIDTH MODULATION

A. Modulation Scheme

Fixed-frequency PWM control is adopted for the DB LLC resonant converter, and the switching frequency fs equals to the resonant frequency f_r .The operating waveforms of the proposed converter. Switches Q1 and Q2 are operated with the fixed 50% duty ratio. Switches Q3 and Q5 are turned on alternatively, and switches Q4 andQ6 are turned on alternatively. The duty ratio of Q3 and Q4 is D and that of Q5 and Q6 is 1−D.ThevariationrangeofdutyratioD I s0–0.5. In this case, the variation of the input voltage is V_{max} :V_{min} =2:1. When the input voltage is at its minimum value V_{min}, the duty ratio of Q3 and Q4 is 50% and that of Q5 and Q6 is 50% as well. Then the converter operates like an FB LLC converter with 50% duty ratio. When the input voltage reaches its maximum value V_{max}, the duty ratio of Q3 and Q4 is 0, whereas the duty ratio of Q5 and Q6 is 100%. In this case, the proposed DB converter operates the same as an HB converter with 50% duty ratio. When the input voltage changes between V_{min} and V_{max}, the duty ratio of Q3 and Q4 changes between 50% and 0% and the duty ratio of Q5 and Q6 is from 50% to 100%. It can be seen that switches Q5 and Q6 together play the role of a bidirectional switch.

B. ZVS Condition

Magnetizing current must satisfy ZVS conduction. The voltage and current of each switch are differently in different modes. V_{q1}, V_{q2}, V_{q3}, and V_{q4} maximum voltage are V_{dc}, and Vds5 and Vds6 are $V_{dc}/2$ of maximum, and because the I_{Lm} charging currents affect Q1 and Q2, Q1 can easily reach the ZVS condition, Q2 is the hardest to achieve ZVS conduction compared to other switches, so here consider the ZVS condition of Q2.

C. Pulse Generation

A simple method to generate the PWM pulse train corresponding to a given signal is the interceptive PWM: the signal (Square wave) is compared with a saw tooth waveform. When the latter is less than the former, the PWM signal is in high state (1). Otherwise it is in the low state (0).

The technique is used so that we achieve respective states.

1) Switch Q1,Q4 is closed for $+V_{dc}$
2) Switch Q2,Q3 is closed for $-V_{dc}$
3) Switch Q1,Q5 is closed for $+V_{dc}/2$
4) Switch Q2 Q6 is closed for $-V_{dc}/2$

State a,b constitute a FB and b,c constitute a HB converter.

D. Closed Loop Model

As the figure 5 shows closed loop system which contains a comparator helpful in finding the error in the voltage of the output. The error signal is fed to the Proportional Integrator, which help in reducing the error signal. The output of the Proportional Integrator is fed to a Square wave with amplitude equals to the output of the Proportional Integrator.

When the error is more PI for corresponding K_p, K_i values output over shoots to reduce it we use saturation so that it doesn't cross the prescribed limit. In the project the maximum saturation used here is about 0.9 as the amplitude of the sawtooth is 1V.

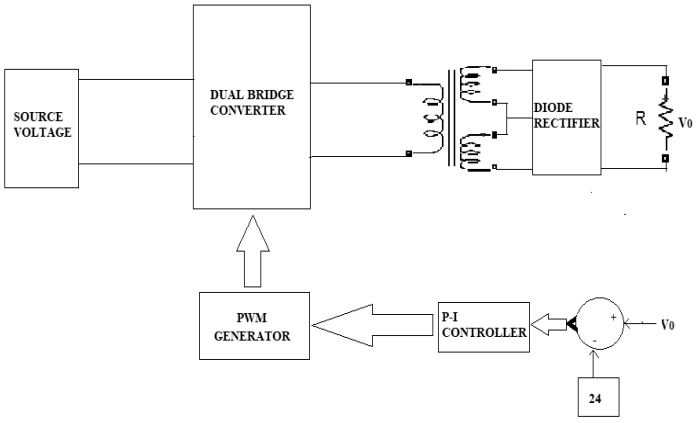


Figure 5 Block diagram of closed loop system

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V. SIMULATION RESULT

For verification of proposed model and analyse the performance, we use MATLAB for simulation with the parameters as stated in Table 1.

The figure 6 (a) shows the LLC Converter voltage for 160V and output 24V (b) shows the voltage for output voltage 10V.

TABLE I
List of Circuit Parameters

Parameter	Nominal Values
V_{in}	160V
f	100kHz
L_m	126.3mH
L_r	25.3uH
C_r	100nF
Turn ratio	5:1:1
R_{out},C_{out}	1.2Ω,7*690uF
Step change in input voltage	160-200V

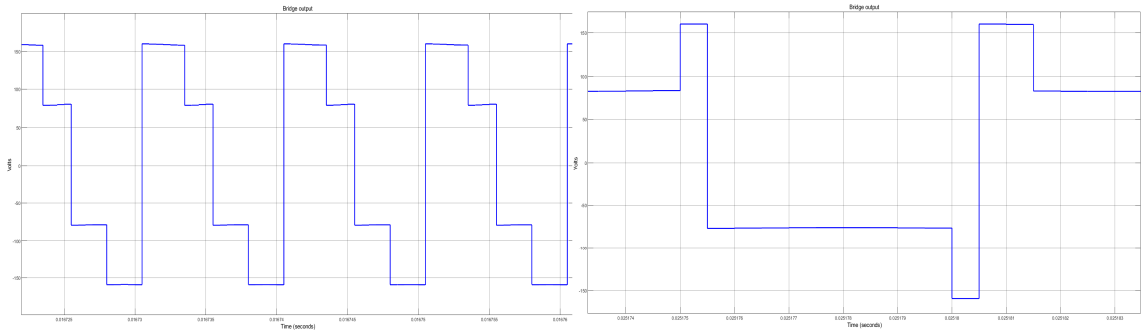


Figure 6 (a) LLC converter Voltage for 24V output (b) LLC converter Voltage for 10V output

The duty cycle changes according to the PI controller. Figure 7 shows the variation in the duty cycle voltage. As the initial voltage is 160V and the output is 24v Volts, the duty cycle of the switch Q3 is about 0.288. But after the voltage spike the Duty cycle is reduced to 0.155. That shows the closed loop is working.

Figure 8 shows the voltage at the output and the change in input voltage of the system. As the initial input voltage is constant of about 160V. But there is a sudden rise in step voltage source which is about 40% of the input. But the voltage at the output is maintained constant. This is because of the PWM generation of using the signal fed from output.

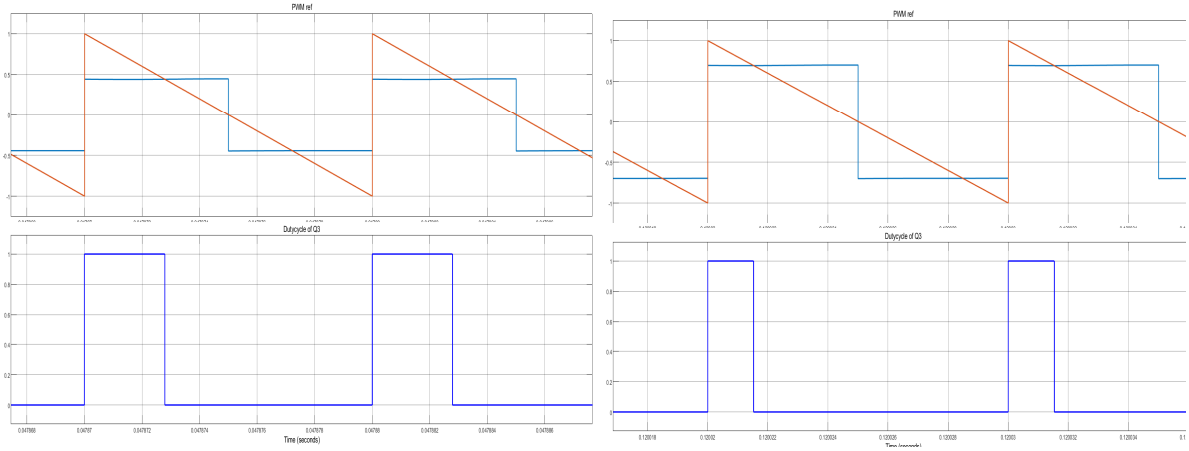


Figure 7 The duty cycle of Q3 and PWM generation block

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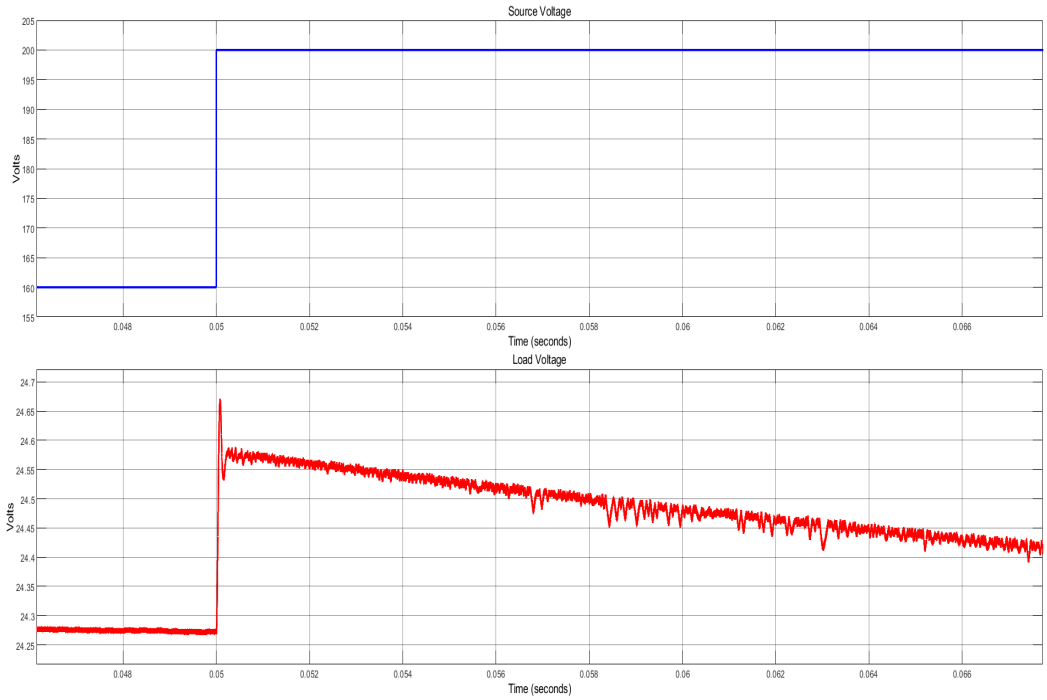


Figure 8 Output voltage variation with input voltage

VI. CONCLUSIONS

This paper has proposed a closed loop system for DB LLC with varying source voltage. With the DB operation the input voltage is efficiently used to give required output voltage. As the input is high the turns ratio of the HF transformers are increases which in turn decrease the losses by large magnetizing inductance in the input side. The PWM system uses different duty ratios for different load conditions which are varying in the source side. The simulation model shows that the proposed method of feedback system can reduce the effect of source voltage on load side and can easily adjust the duty ratios of the switches to obtain the constant and required voltage. Here, we can vary the output voltage and this helps in providing variety of applications.

VII. ACKNOWLEDGMENT

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REFERENCES

[1] Y. Jeong, J. K. Kim, J. B. Lee and G. W. Moon, "An Asymmetric Half-Bridge Resonant Converter Having a Reduced Conduction Loss for DC/DC Power Applications With a Wide Range of Low Input Voltage," in IEEE Transactions on Power Electronics, vol. 32, no. 10, pp. 7795-7804, Oct. 2017.

[2] R. Saasaa, W. Eberle and M. Agamy, "A single-stage interleaved LLC PFC converter," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-6.

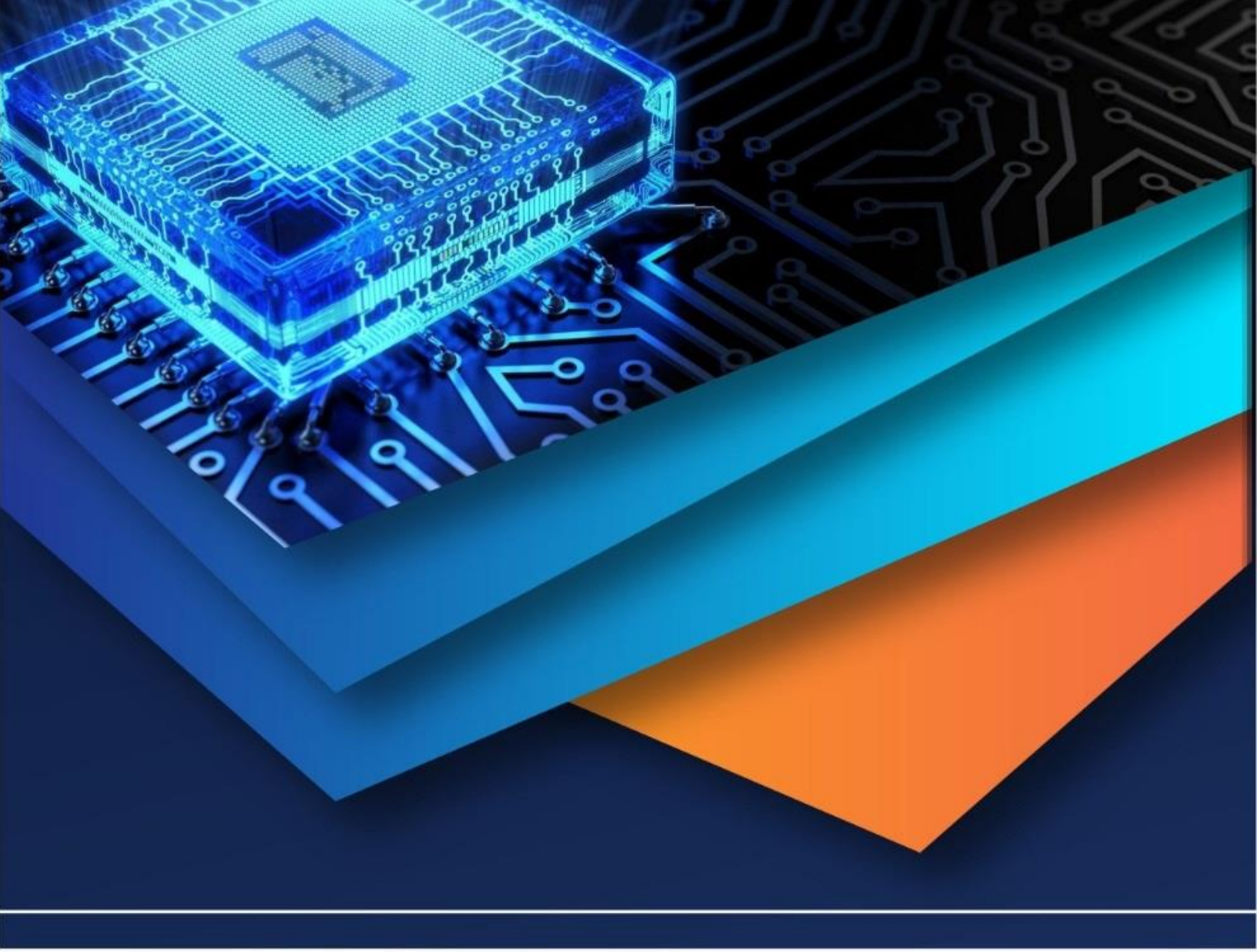
[3] X. Sun, X. Li, Y. Shen, B. Wang and X. Guo, "Dual-Bridge LLC Resonant Converter With Fixed-Frequency PWM Control for Wide Input Applications," in IEEE Transactions on Power Electronics, vol. 32, no. 1, pp. 69-80, Jan. 2017.

[4] M. M. Jovanović and B. T. Irving, "Efficiency optimization of LLC resonant converters operating in wide input- and/or output-voltage range by on-the-fly topology-morphing control," 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, 2015, pp. 1420-1427.

[5] C. E. Kim, J. I. Baek and J. Lee, "High-Efficiency Single-Stage LLC Resonant Converter for Wide-Input-Voltage Range," in IEEE Transactions on Power Electronics.

[6] J. H. Kim, C. E. Kim, J. K. Kim, J. B. Lee and G. W. Moon, "Analysis on Load-Adaptive Phase-Shift Control for High Efficiency FullBridge LLC Resonant Converter Under Light-Load Conditions," in IEEE Transactions on Power Electronics, vol. 31, no. 7, pp. 4942-4955, July 2016

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