iJRASET
International Journal For Research in Applied Science and Engineering Technology



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 9 **Issue:** VIII **Month of publication:** August 2021

DOI: https://doi.org/10.22214/ijraset.2021.37893

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429
Volume 9 Issue VIII Aug 2021- Available at www.ijraset.com

FinFET Response under Radiation and Bias Stress

Uma Bisht[1], Ankit Pawariya[2]
[1]*M.Tech. Scholar,* [2]*Assistant Professor, Department of Electronics and communication, CBS Group of Institutions, Jhajjar (Haryana), Maharishi Dayanand University, Rohtak*

Abstract: ***The study of FinFET Response under various parameters change is widely studied in many branches of Electronics Engineering. FinFET structure is going beyond the downscaling limit of the conventional planar CMOS technology. The major applications of FinFET have been mainly devoted to digital circuits, analog circuits, and targeting a successful mixed integration of analog and digital circuits. The purpose of this paper is to provide a clear and exhaustive understanding of the state of the art, challenges, and future trends of the FinFET technology from a microwave modeling perspective. Inspired by the traditional modeling techniques for conventional MOSFETs, different strategies have been proposed over the last years to model the FinFET behavior at gamma radiation. With the aim to support the development of this technology, a comparative study of the achieved results is carried out to gain both useful feedbacks to investigate the microwave FinFET performance as well as valuable modeling.***

Keywords: CMOS, MOSFET, FinFET, Hot carriers, Gamma Chamber, SCE, DIBL, Oslo Si-Bulk FinFET, Wafer probe station.

I. INTRODUCTION

MOSFET is the elementary unit in the high-density integrated circuits, known as ICs. When these elementary units interact with the high energy radiation, which is mostly present in space, like gamma radiation, cosmic radiation, and ultraviolet rays, we observe shifts in the characteristics of the devices from normal behavior. On the other hand, when we use a transistor for a certain period, its performance changing gradually. Some changes in the behavior of transistors are observed like the degradation in the performance, reliability and sometimes complete failure of the device is known as means transistor aging or silicon aging. This impact that aging cause is somewhat like what we observe in the case of radiation. Since in space, satellites are continuously using integrated circuits under high energy radiations so, it is very important to know that how aging will impact the radiation behavior of the transistor[9]. To observe this a comparative study of the performance of bulk Si FinFET from these experimental setups: a) Radiation after stress and b) Stress after radiation. For this experiment, the radiation[11] used as gamma radiation and devices were bulk Si FinFETs from IBM USA. Finally, we concluded the overall impact of bias stress on radiation performance.

1) *FinFET is a Multigate Device:* A Fin-shaped field-effect transistor has a fin-shaped body, so it is called FinFET. The channel (fin) of the FinFET is vertical. A simple MOSFET contains substrate, gate, source, and drain. But in the case of a multigate device, the MOSFET device can have a gate on two, three, or four sides of the channel. A double gate structure is made when we cover the channel with gate material from different sides. These devices come under the category of FinFETs. It is because of the shape of the gate which looks like a fin. The benefit of a FinFET device is that it has a high current density and faster switching time than a complementary metal oxide conductor (CMOS).
   Why FinFET instead of MOSFET?
   To understand that we need to understand the short channel effects (SCE). So, we will start with Moore's law and scaling theory. It is an observation that suggests that the number of transistor available in an IC (integrated circuit) gets double every two years. When the number of transistors increases on the same IC it reduces the cost of the devices also increases the processing speed of the devices. Following are the SCE: 1) DIBL 2) Subthreshold swing 3) Velocity saturation 4) Punch-through 5) Hot carrier effects
2) *DIBL is a short channel effect in MOSFETs:* It refers that when we apply a higher voltage on the drain terminal then, it causes a reduction in the threshold voltage of the transistor. In the case of a large value of channel length of a transistor, the bottleneck in the formation of the channel happens very far from the drain region. So, in a way, there is no impact of drain voltage on the combination of gate and substrate. That's why threshold voltage is independent of drain voltage. But in the case of short channel devices, the drain region is very close to the gate of the channel. So, when we apply high drain voltage in a short channel transistor, it can turn on the transistor prematurely.

©IJRASET: All Rights are Reserved

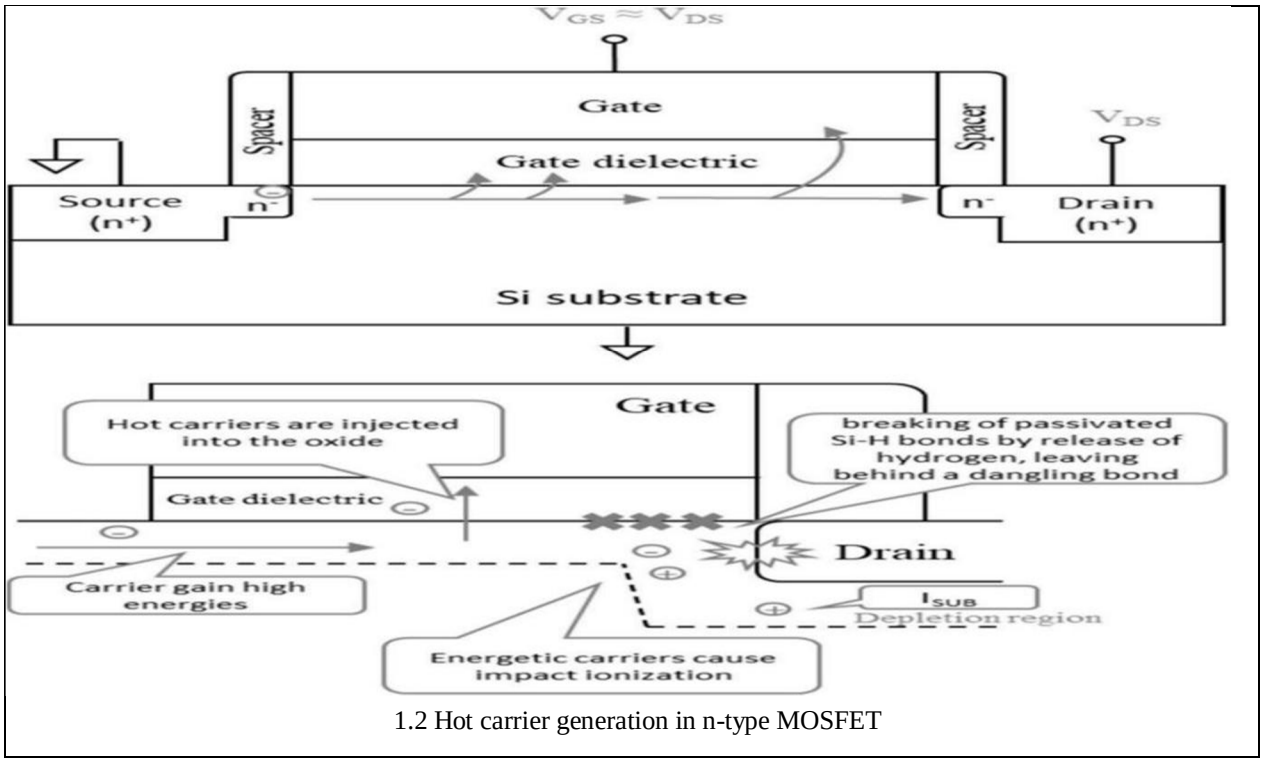
a) *Subthreshold Swing:* In the subthreshold region (is a region in which MOSFET is operating at the voltage little less than the threshold voltage[11] of the MOSFET), the behavior of the drain current is very much like the forward biased diode. It is considered good to have a smaller value of subthreshold swing. A high value of subthreshold swing causes a higher off-state current.

b) *Velocity Saturation:* The drift velocity of electrons is directly related to the value of the electric field only for lower values of electric field. But in the case of the high value of the electric field, drift velocity gets saturated, which we called saturation velocity. In short channel MOSFET saturation current is almost linearly dependent on drain source voltage and output impedance also reduces. In short channel devices, the electric field in longitudinal direction also increases. Because of the high value of the electric field, a saturation of velocity occurs, and it also affects the MOSFETs' I-V characteristics.

c) *Punch Through:* It is an extreme case of barrier lowering. When we increase the bias applied at the drain region, the depletion region formed around the drain can easily get extended toward the source region and can cause the merging of the two depletion regions. In this case, the gate voltage doesn't have control over the drain current. Another problem is that it leads to a decrease in effective channel length. Because of punch-through, we can't turn off the transistor and the device becomes useless.

d) *Hot Carrier Effects:* Hot carrier injection occurs in semiconductor devices when electrons and holes gain a very large amount of kinetic energies and they cross the potential barriers and reach the conduction or valence band in the silicon oxide. The hot electron effect model is somewhere is showing a similar effect as in case of power dissipated, the electron gas temperature, and overheating. Hot carrier injection mainly occurs in N- channel, HCI is an irreversible event in MOSFET. HCI depends on the internal electric field induced in the channel.

The cross-sectional view of n-type MOSFET has been shown in the diagram to describe hot carrier generation phenomena. Some of these electrons have such a high amount of energy that they can cause impact ionization[1] as they reach near the drain region. Because of that, it can give rise to the drain to body current. It is also possible that some of these hot carriers can collect by the gate after tunneling through the oxide.



1.2 Hot carrier generation in n-type MOSFET

Above mentioned short channel effects occur in conventional MOSFET. While in FinFET, since the channel is wrapped around by the gate structure, it provides better SCE. It also has been observed that FinFET allows having better mobility. Because of all this, FinFETs give higher speed, low power consumption due to low leakage.

©IJRASET: All Rights are Reserved

II. IMPACT OF RADIATION ON MOSFET

Many radiation particles are present in space and other radiation environments. Particle and photon radiation are two types of radiation[10]. Particle radiation includes charged particles and neutral particles like electrons, ions, protons, alpha particles, and neutrons. On the other hand, photon radiation constitutes high energy gamma rays and x-rays. We have different units for both types of radiation when we are dealing with their radiation impact[9]. When we are looking at the impact of photon radiation, the unit that we use is *rad.* "A rad is the amount of photon radiation which deposits 100 ergs of energy per gram of a given material". Insulators and oxides are the key components of all electronic devices from MOSFETs to bipolar ICs. When a device interacts with radiation, it builds up charge in the insulators like silicon oxide that can lead to device failure. In radiation environments, interaction with high energy photons and electrons can significantly reduce the lifetime of the system due to TID, total dose effects. Apart from TID, there are some transient effects, which we call Single Event Effects (SEE). TID is a long-term effect that permanently degrades the device while SEEs are transient.

1) *TID (Total Ionizing Dose):* When MOSFET is put under some radiation, the high energy electrons (like the ones present in the environment or photon generated secondary electrons) and protons can cause the ionization of the atoms and hence electron-hole pairs generated. Until these high energy particles have energy that is greater than the minimum energy required to generate electron-hole pairs ($E \leq hv$), additional electron-hole pairs will keep on generating by them. In this way, a single particle or photon can generate a considerable amount of electron-hole pairs. When such high energy radiation particles interact with MOSFETs, as expected, the generation of electron-hole pairs takes place. This e-h pair generation in the oxide is the main reason that causes almost all kindsof TID effects. Charge build-up induced in the oxide can cause device failure. The mechanism of charge build-up and device degradation. The e-h pairs are generated by the radiation, charge carriers will be swept by the gate electric field. Because of the positive electric field in the oxide, the electron will move toward the gate, and holes will travel toward the interface. The number of e-h pairs that avoid recombination is called the charge yield.

A. *Traps Due to Radiation and bias Stres*

1) *Oxide Traps:* The number of electrons is moving from the source to drain in the inversion layer of Si substrate can be trapped due to the gate oxide's defects which are located very close to the semiconductor-dielectric interface ($Si-SiO_2$)[6]. The mobility of holes is less in comparison to that of electrons. Because of the applied gate electric field, the generated holes travel to the oxide/gate interface, if the bias is negative. If the bias is positive near the interface, Vacancies are present because of oxygen's "out-diffusion" in the oxide, dangling bonds. These vacancies can work as "trapping centers" for holes. Some holes will be captured bytraps as they travel toward the interface. The fraction of holes that are going to be trapped in something depends on the fabrication process. Since the effective charge trapped in the oxide is positive so it causes a negative shift in the threshold-voltage of NMOS as well as PMOS transistor. Electrons, trapped in the gate oxide, decrease the net potential drop between the positively biased gate terminal and grounded substrate, which decreases the effective gate voltage and subsequently decreases the drain current.
2) *Interface Traps:* Radiation can also cause the formation of interface traps. These traps can be positive, negative, or neutral. Because of the presence of these traps at the interface, its charge can be easily changed by applying a gate bias. Traps which are present in band gap's lower portion are able to donate an electron to Si and hence, called donors. Therefore, for the PMOS transistor, the interface traps are positively charged which causes negative shifts in threshold voltage. While the traps that are present in the band gap's upper portion are able to accept an electron from Si and hence, called acceptors. Therefore NMOS transistor consists of negatively charge interface traps which finally cause the threshold voltage ($\mathbf{V_{th}}$) to shift positively. For interface traps at the mid gap, they are approximately neutral. Previously, we have also seen the impact of oxide traps on NMOS and PMOS. So, we can conclude from here that $\mathbf{N_{it}}$ (interface traps charge) and $\mathbf{N_{ot}}$ (oxide traps charge) and are additive for PMOS and subtractive for NMOS.

III. REQUIREMENTS

To conduct the experiment, OSLO bulk FinFET is needed for radiation and stress purposes. To observe the impact of the different experiment on the transistor, I used wafer probe station for measurements and gamma chamber to radiate the transistors.

A. *OSLO Si-Bulk FinFET*

We have two chip each having 3 Bulk Si-FinFET of scaled length equal to (dev1 = 70nm), (dev2 = 100nm) and (dev3 = 150nm), with the supply voltage (V_{DD}) of 1.2V. Measuring devices have an effective width (W) of 33.6μm.

©IJRASET: All Rights are Reserved

Device	nFin	designW	scaledL	nX	nY	Gate Area = 0.07* nFin* scaledL* nX*nY (μm^2)
NPEgA_1, dev1=N	24	1.008	0.07	10	2	2.352
NPEgA_1, dev3=N	24	1.008	0.10	10	2	3.36
NPEgA_1, dev5=N	24	1.008	0.15	10	2	5.04

Table 1 Specifications of bulk Si-FinFET

B. Wafer Probe Station

In this experiment, the Cascada wafer probing station was used to measure the impact of bias stress and radiation on DC transfer characteristics of transistors. Here the chip is irradiated by gamma rays to see the impact of radiation on the chip and shift in the transfer characteristics (I_D vs V_{GS}) for which Keysight B1500A semiconductor device parameter analyzer was used. The device used for this is shown in the figure 3.1



Figure 3.1 Probe station

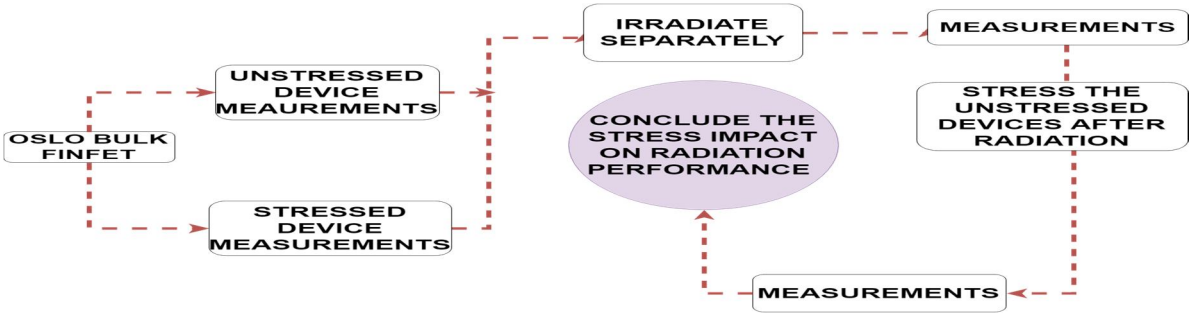
C. Gamma Chamber

FinFET transistors were kept under gamma radiation. Gamma radiation available in the chamber had a dose rate of 2.936 KGy/Hour. In this experiment, we tried to accumulate the radiation of 4 MRad. For that, we need to calculate the amount of time we should keep the transistors into the gamma chamber.

In this experiment of gamma radiation, we have

1) Measurements of fresh transistors.
2) Measurements of the transistor which we first put under stress and then radiation, which is R2.
3) Measurements of the transistor which we first radiated and then put under stress, which is R1.

D. Schematic of Procedure



We started the experiment by taking the measurements on fresh devices of both the chips R1 and R2. In measurements, we take the I_D vs V_{GS} and I_D vs V_{ds} curve for all six devices. Then, we put the transistors on chip R2 under stress.

To put the FinFETs under stress we applied the following biases at different terminals using Cascade wafer probe station.

©IJRASET: All Rights are Reserved

FinFET device of length	Applied V_{ds}	Applied V_{gs}	Time duration
70nm	V_{ds} = 1.2 V	V_{gs} = 1.5 V	1600
100nm	V_{ds} = 2.5 V	V_{gs} = 1.5 V	3700
150nm	V_{ds} = 2.5 V	V_{gs} = 1.5 V	3600

These devices transfer characteristics, (I_D vs V_{GS}), are measured by applying the variable voltage at the gate terminal. Gate terminal voltage varied from -0.6V to 1.5V at same Vds, drain voltage.
After that, we put both the chips under gamma radiation of 4Mrad. 1 Mrad = 10,000 Gy
The rate of gamma radiation in the chamber was 2.936 KGy/hour.
Time required = 4 Mrad/ 2.936 KGY/hour = 13 Hours, 37 Min
Time required = 13 Hours, 37 mins.
We took out the chips from gamma chamber after a calculated time and got the gamma irradiation of 4Mrad on R1 and R2. We put the devices under test and took the measurements using probe station. Then, we put R1 under stress to observe the impact of after radiation. Again we used the same bias stress as we put for R2 to get the comparative study.

IV. OBSERVATION

Si-FinFET is tested under the following conditions:
1) Stress followed by radiation and
2) Radiation followed by stress
And observed on Bulk Si-FinFET of different lengths for 4MRad dose w.r.t change in the device parameters such as ΔV_{tlin}, %Igon, shown in figure 3.1 and figure 3.2 respectively.

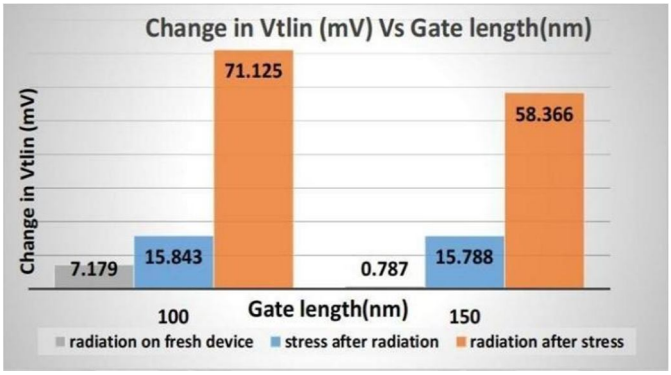


Figure 3.1 Change in V_{tlin} for 100 and 150 nm gate length for the different set of experiment

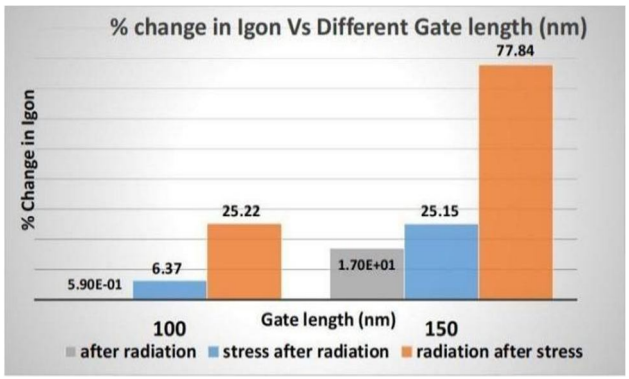


Figure 3.2 Percentage change in Igon for 100 and 150 nm gate length for the different set of experiment

After the experiment, out of 6 devices, two devices of gate length 70nm get shorted. For remaining devices, we observed the parameters of the measured device using DC transfer characteristics that include the change in gate leakage current and linear threshold voltage shift (ΔV_{tlin}).

V. RESULT

Figure 3.1 show %Vtlin respectively vs. Effective gate length = 100nm and 150nm devices for process A and B. A positive shift in the threshold voltage was observed. The increase in threshold voltage value, ΔVtlin, is evident of the interface traps build-up at the Si-SiO_2 interface. Process A shows a largely positive shift in Vtlin in comparison to the process B.
The reason is that stress on FinFETs before radiation haa generated an extra number of defects at the interface. So, when we radiated the stressed device, because of the extra number of defects, it generates a relatively large number of interface traps and hence we got a positive shift in threshold voltage.

©IJRASET: All Rights are Reserved

Figure 3.2 shows the increase in gate leakage current because of stress and radiation. It is clear from the graph that the change in gate leakage current is more in the case of process A, in comparison to process B. When we first stress the device then it generates traps in the oxide. During irradiation, generated electron-hole pairs have the availability of traps to move. So, trapped charge build-up in oxide regions increases transistor leakage current. But when we follow procedure B, since there is no prior stress and hence no availability of vacancies, gate leakage current is less. As we suggested that radiation after stress contains a large number of traps, so % increase in leakage current, is more in comparison to the stress after radiation.

VI. CONCLUSION

DC characteristics or transfer characteristics of Si-bulk FinFET are measured from these experimental procedures :"Radiation after stress" and "Stress after radiation". In process A, we found that gate leakage current will be larger in comparison to process B because of oxide traps generated by stress before radiation.

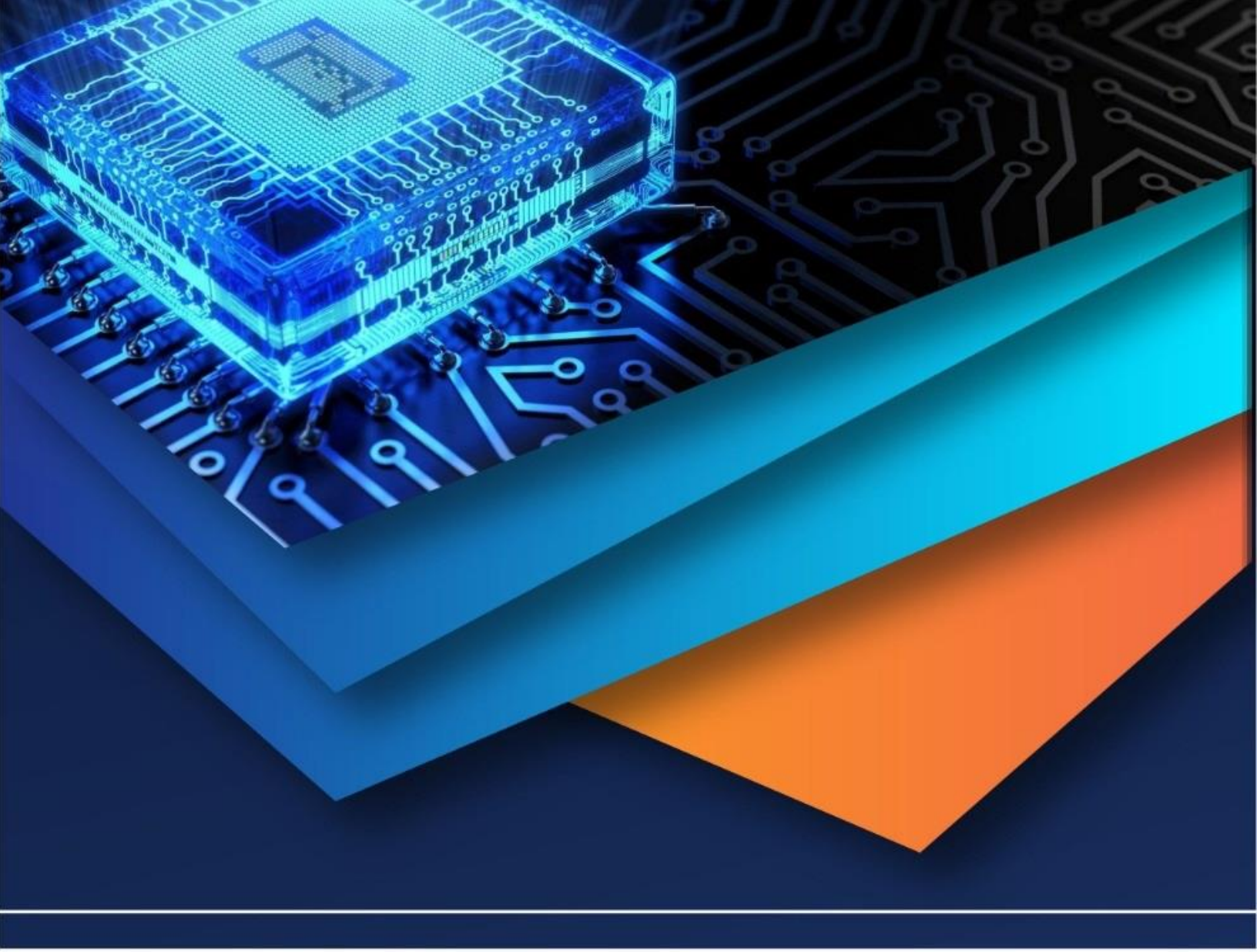
For effective length 100nm, the change in V_{tlin} is 71.125 mV for process A and 15.843 mV for experimental setup B. For effective length 150nm, change in V_{tlin} is 58.366 for process A and 15.788 for experimental setup B. Process A shows considerably large degradation in V_{tlin} in comparison to B.

We found that bias-stress or continuous usage of devices make Bulk FinFETs morevulnerable to get impacted by radiation.

REFERENCES

[1] Cheng T. Wang, Hot Carrier Design Considerations for MOS Devices and Circuits, Van Nostrand Reinhold, 1990.
[2] Y. Nissan-Cohen, J. Shappir, and D. Frohman-Bentchkowsky, \Trap Generation and Occupation Dynamics in SiO2 under Charge Injection Stress," J. Appl. Phys., vol. 60, no. 6, pp. 2024{2035, Sept. 1986.
[3] Brian Doyle, Marc Bourcerie, Jean-Claude Marchetaux, and Alain Boudou, Interface State Creation and Charge Trapping in the Medium-to-High Gate Voltage Range (Vd _ Vg _ Vd) During Hot-Carrier Stressing of n=MOS Transistors," IEEE Transactions on Electron Devices, vol. 37, no. 3, pp. 744{754, March 1990.
[4] L. Lipkin, A. Reisman, and C. K. Williams, \Hole Trapping Phenomena in the gate Insulator of As-Fabricated Insulated Gate Field E_ect Transistors," J. Appl. Phys., vol.68, no. 9, pp. 4620{4633, Nov. 1990.
[5] S. J. Wang, J. M. Sung, and S. A. Lyon, \Relationship Between Hole Trapping and Interface State Generation in Metal-Oxide-Silicon Structures,"Applied Physics Letters, vol. 52, no. 17, pp. 1431{1433, April 1988.
[6] S. Lai, \Two-Carrier Nature of Interface-State Generation in Hole Trapping and Radiation Damage," Appl. Phys. Lett., vol. 39, pp. 58, 1981.
[7] Y. Roh, \Interface Traps Induced by Hole Trapping in Metal-Oxide Semiconductor Devices," J. Non-Cryst. Sol., vol. 187, pp. 165{169, 1995.
[8] Eiji Takeda, Hitoshi Kume, Toru Toyabe, and Shojiro Asai, \Submicrometer MOSFET Structure for Minimizing Hot-Carrier Generation," IEEE Transactions on Electron Devices, vol. ED-29, no. 4, pp. 611{618, Apr. 1982.
[9] Y. H. Lho, K. Y. Kim, "Radiation Effects on the Power MOSFET for Space Applications," ETRI Journal, vol. 27, no. 4, Aug. 2005, pp. 449-452. DOI: 10.4218/etrij.05.0205.0031
[10] J. R. Schwank, M. R. Shaneyfelt, D. M. Fleetwood, et al., "Radiation Effects in MOS Oxides," IEEE Trans. Nuclear Science, Vol. 55, no. 4, pp. 1833-1853, 2008.
[11] H. L. Hughes, J. M. Benedetto, "Radiation Effects and Hardening of MOS Technology: Devices and Circuits," IEEE Trans. Nuclear Science, vol. 50, number. 3, pp. 500-521, 2003.

©IJRASET: All Rights are Reserved



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Call : 08813907089 (24*7 Support on Whatsapp)