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Simulation and Analysis of different CMOS Full Adders for Delay Optimisation

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Abstract: ***Full adder circuit is one among the fundamental and necessary digital part. The full adder is be a part of microprocessors, digital signal processors etc. It's needed for the arithmetic and logical operations. Full adder design enhancements are necessary for recent advancement. The requirement of an adder cell is to provide high speed, consume low power and provide high voltage swing. This paper analyses and compares 3 adders with completely different logic designs (Conventional, transmission gate & pseudo NMOS) for transistor count, power dissipation and delay. The simulation is performed in Cadence virtuoso tool with accessible GPDK – 180nm kit. Transmission gate full adder has sheer advantage of high speed, fewer space and also it shows higher performance in terms of delay.***
Keywords: Delay, power dissipation, voltage, transistor sizing.

I. INTRODUCTION

Addition is one among the common and wide used elementary operation in several VLSI systems. The usage of adders are for arithmetic operations such as subtraction, multiplication, division, address decoders etc. The full adder is designed and 1-bit full adder performance plays a very important role in VLSI. The Modified architectures of full adders exploit different logic styles and technologies and that they ordinarily aim at reducing power consumption and increasing speed. The optimized design is needed to forestall any decrease in signal magnitude, give little delays, consume less power in crucial paths and even at low voltage it has to maintain consistency.

In recent advanced applications of VLSI technologies in audio and video process, microprocessors and digital signal process etc., arithmetic operations are used. Before, VLSI applications were principally addicted to space, dependableness and value instead of power. Demand for low power increased and thanks to latest growth of electronic product like moveable mobile phones, laptops and alternative devices wants high speed and low power consumption. The foremost downside in portable devices was that it consumed high power that result in less battery life and caused failure in semiconducting material elements of the devices. To regulate the heat dissipation, the device needs high packaging price and cooling necessities.

Full-adder is a combinational circuit with 3 inputs. The primary 2 inputs are A and B, the third input Cin represents the carry. The 2 outputs are selected by the Sum (S) and Carry (C). Sum gives the values of least significant bit and Carry gives values of most significant bits. A pair of XOR gates, a pair of NAND gates and one OR circuit the full adder circuit is built.

SUM=A XOR B XOR C

COUT=AB + C (A+B)

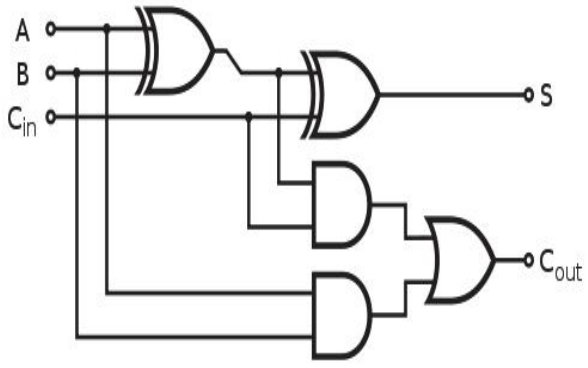

Figure. 1 Full adder block diagram.

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Table 1. Truth table of full adder

INPUTS			OUTPUTS	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

II. OBJECTIVE

1) Design of single bit full adder using different CMOS technique and comparative analysis in the terms of delay and power is the main aim of the project.
2) The design of full adder using three different CMOS techniques are implemented in this project.
a) Conventional CMOS full adder
b) Transmission gate full adder
c) Pseudo NMOS full adder (Proposed design)
3) A full adder to be designed using conventional CMOS technique that is complementary CMOS structure. Then Transient analysis is to be performed and propagation delay and average power consumption are to be calculated by using the tool.
4) Pseudo NMOS technique is considered to design the full adder. This proposed design should be optimized in terms of delay when compared to conventional CMOS design.
5) A full adder to be implemented using transmission gates, which is based on the XOR gate architecture.
6) The average power and propagation delay are to be compared with the different full adder designs.

III.BACKGROUND

A single bit full adder operation and also the truth table is explained in CMOS VLSI style textbook. The expression for the adder is implemented in the paper for standard CMOS technique and for pseudo NMOS technique [1]. Analysis and comparison of 4 architectures with totally different logic designs (Conventional, transmission gate, fourteen semiconductor units and GDI based technique) for transistor counts, power dissipation, delay and power delay product. It is performed in virtuoso Cadence. The area optimized by considering the acceptable transistors size for PMOS and NMOS [2]. The target is to scale back power and delay of a full adder by numerous one bit full adder styles and techniques. A comparative analysis is shown for power and delay with totally different range of transistors that is employed to increase the battery life. The adder circuit is designed and implemented in the virtuoso platform [3]. The performance of eleven 1-bit full adder cells supported different logic designs area unit evaluated. The work includes analysis performance of various logic designs as well as input test pattern that area unit analysed considering the delay and power-delay product. Cadence Virtuoso atmosphere is employed for creating schematics. All the analyses showed that 10-Transistor full adder options smart delay performance, represents higher delay product and consumes lower power as compared to entire eleven full adder [4]-[5]. A comparison of different full adder circuits is analysed. Full adder circuits area unit extensively utilized in digital style. The various forms of full adder like standard CMOS, EXOR and EXNOR, pass transistor unit logic gate diffusion technique were performed. Among these, GDI technique took less range of transistors and so consumed less power. In GDI – 14T, 12T and its supported MUX is implemented. The power consumption was less for 12T whereas higher output is obtained for 10T. Simulation was conducted 180nm technology with mentor graphics tool [6].

IV. METHODOLOGY

There are many architecture to implement a full adder. Every architecture offers some advantages at an equivalent time have some demerits. So, a designer has to concentrate on a precise criterion before implementing a design approach. During this project full adders are simulated and designed.

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A. Conventional CMOS Full Adder (28T)

There are different styles for implementing full adder logic, standard CMOS full adder is that the most simple approach. It has 28 transistors. In Figure 2, the circuit diagram for the planning is shown. The expression is created by modifying the fundamental equation of full adder as

SUM = ABC + COUT (A+B+C)

COUT = AB + C (A+B)

The expression is translated into complementary CMOS circuit to implement the traditional full adder. The design has NMOS and PMOS transistors that represents Pull down and Pull up parts respectively. The implementation offers smart driving capability and full swing in output voltage. However because the semiconductor unit numbers are additional, it consumes additional power and occupied additional space. Because of several leakages, the sub threshold will increase. Because the pull up network consists of PMOS networks it ends up in high input capacitance and ends up in additional dynamic power and delay.

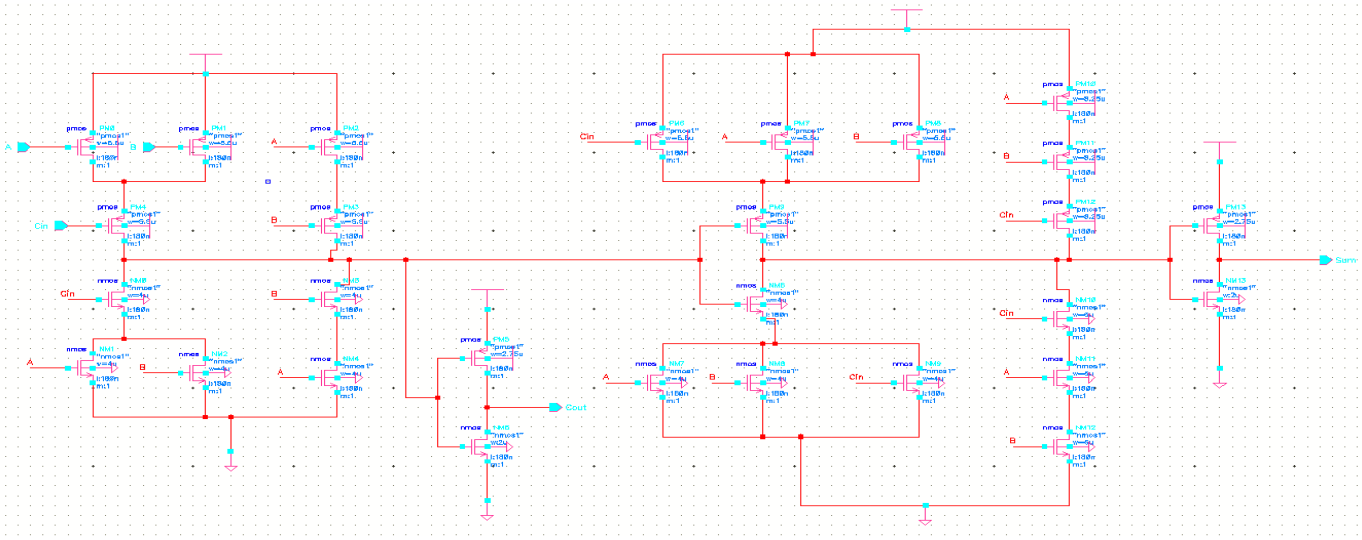

Figure. 2 Conventional CMOS full adder.

B. Transmission Gate Full Adder (20T)

Transmission gate full adder circuit consists of twenty transistors to implement. Figure 3 represents the semiconductor unit level implementation of this topology. The design uses the XOR gates that is formed by transmission gate. A PMOS and an NMOS transistor are connected in parallel to create the transmission gate with control signals. Since transmission gate passes entire voltage vary at its output, therefore the degradation of output voltage of the adder is incredibly less. Parasitic Capacitance is accumulated because of the rise within the internal node count. The driving capability is lower when compared to alternative style methodologies. This circuit occupies less area than conventional circuit.

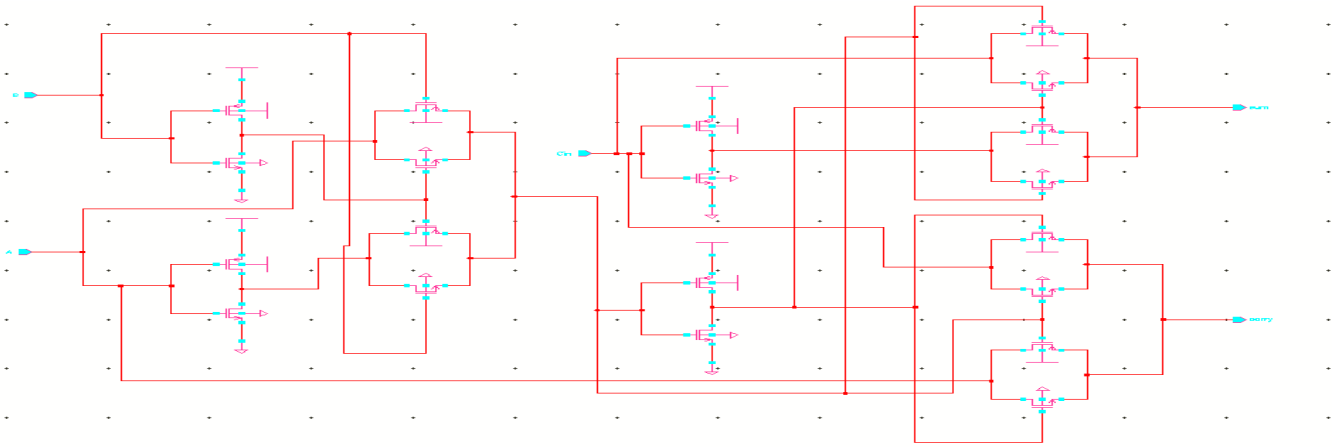

Figure. 3 Transmission gate full adder.

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C. Pseudo NMOS Full Adder (18T) (Proposed Design)

Static CMOS gates are slowed as a result of input should drive each NMOS and PMOS transistors. In any transition, either the pull-up or pull-down network is activated; that means the input capacitance of the inactive network loads the input. Moreover, PMOS transistors have poor quality and should be sized larger to realize comparable rising and falling delays. Here, the architecture of Pseudo-NMOS logic is given, it offers improved speed by removing the PMOS transistors from loading the input. A single PMOS transistor is used for Pull up circuit and it is connected the ground. By connecting PMOS to a ground, there's a good reduction within the pull-up transistors. This methodology additionally brings down the capacitance of the input by employing a single resistance. A, B, C as inputs and Sum, carry as outputs. The figure 4 shows the Schematic diagram of a full adder.

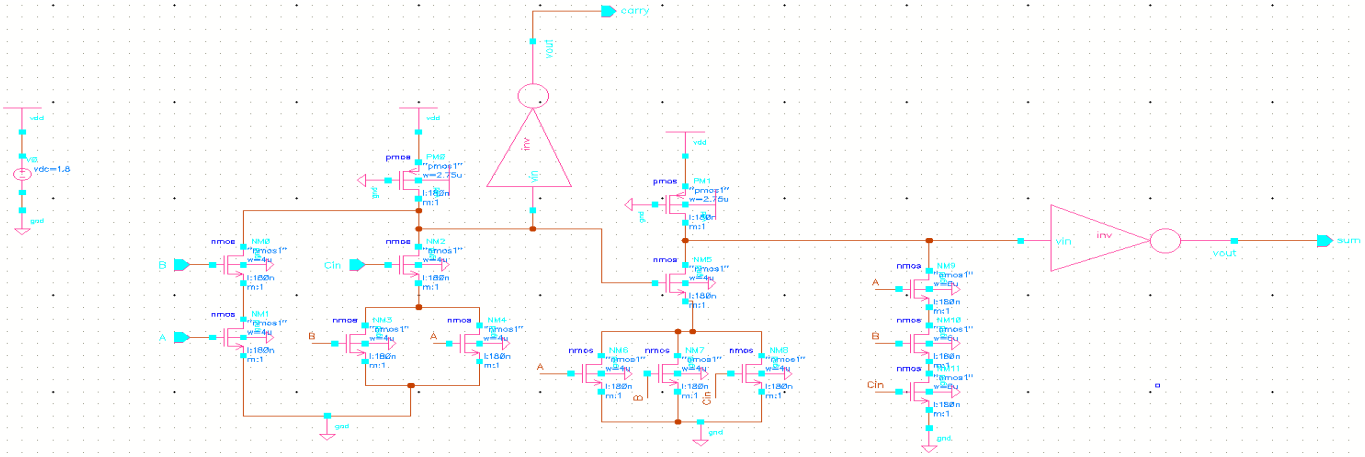

Figure. 4 Pseudo NMOS full adder.

V. RESULTS AND DISCUSSION

Table. 2 Results.

Sl No.	Adder type	No. of Transistors	Delay		Power
			Input to Sum	Input to Carry	
1	CMOS Full Adder	28	169.09 ps	100.83 ps	32.77 uW
2	Pseudo NMOS Full Adder	18	104.75 ps	70.97 ps	1.26 mW
3	Transmission Gate Full Adder	20	88.18 ps	48.56 ps	21.69 uW

For simulating and comparing the performances of 1 bit full adder with different design topologies, Cadence Design Suite 6.1.6 for GPDK 180nm CMOS technology operating in Virtuoso environment at room temperature was used. For the analysis, the supply voltage VDD was set at 1.8 Volt for each of the full adder. During the simulation, the inputs (A, B, C), pulses with different periods were given which is VPULSE in this software, where the pulses were varied from 0 Volt to 1.8 Volt. Here, in order to compare and inspect the different simulated full adder topologies, the width and length of PMOS and NMOS were set at an indistinguishable value for each of the adder. Length was set at 180 nm. Width of PMOS and NMOS were set at 2.75 um and 2 um respectively. The width of the PMOS was calculated by parametric analysis of Wp (A variable for the width of PMOS) versus average propagation delay with respect to a CMOS inverter. With that analysis it was found that the average propagation delay is minimum for the PMOS for the width of 2.75 um. Keeping the CMOS inverter as a reference the width of the PMOS in the design are set accordingly. Transient analysis was done to verify the adding process by observing how sum and carry is changing with the given input (A, B, C) values. Delay was also calculated by monitoring the transient response. Performing DC analysis the power consumptions by the adder circuits were obtained.

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By doing transient analysis the truth table of a full adder are successfully verified. During the simulation it is clearly investigated that increasing the value of load capacitance reduces this noise at an obvious manner. The propagation time delay was calculated by the 50% of input voltage at which the time difference between the input and output waveform was calculated. Rising and falling propagation delays of input to sum and input to carry are obtained and from these two values the average propagation delay is calculated using the equation below

$$tpd = (tPLH+tPHL)/2$$

Where, tpd is the average propagation delay, tPLH is the rising propagation delay and tPHL is the falling propagation delay.

From the Table 2, in terms of delay carried out of transient analysis, transmission shows the best performance among all others but it has considerable amount of power consumption. The conventional CMOS full adder gives the full swing voltage but the delay is more due to the parasitic capacitances and also power is more due to static leakage current. In the proposed design i.e., the Pseudo NMOS design is implemented by using the same expression used in the conventional CMOS adder but with a different technique. In the proposed design the area and delay is optimized when compared to the conventional CMOS adder circuit, but has the pull-up device is always ON there will be more static current which can be eliminated by using dynamic circuits concept in the future.

VI. CONCLUSION

Here in the paper, different full adder circuits are designed and simulated for power consumption and delay. The proposed full adder is the Pseudo NMOS full adder which is faster than the conventional CMOS full adder. The area of Pseudo NMOS full adder is lesser than the CMOS conventional full adder as in less transistors are used. Comparatively, the transmission gates offers benefits in both power consumption and delay. For different applications, a specific full adder architecture is used. In the proposed full adder delay is optimised but the power consumption is increased. This can be resolved by using sleep transistors to minimize the static power consumption.

VII. ACKNOWLEDGEMENT

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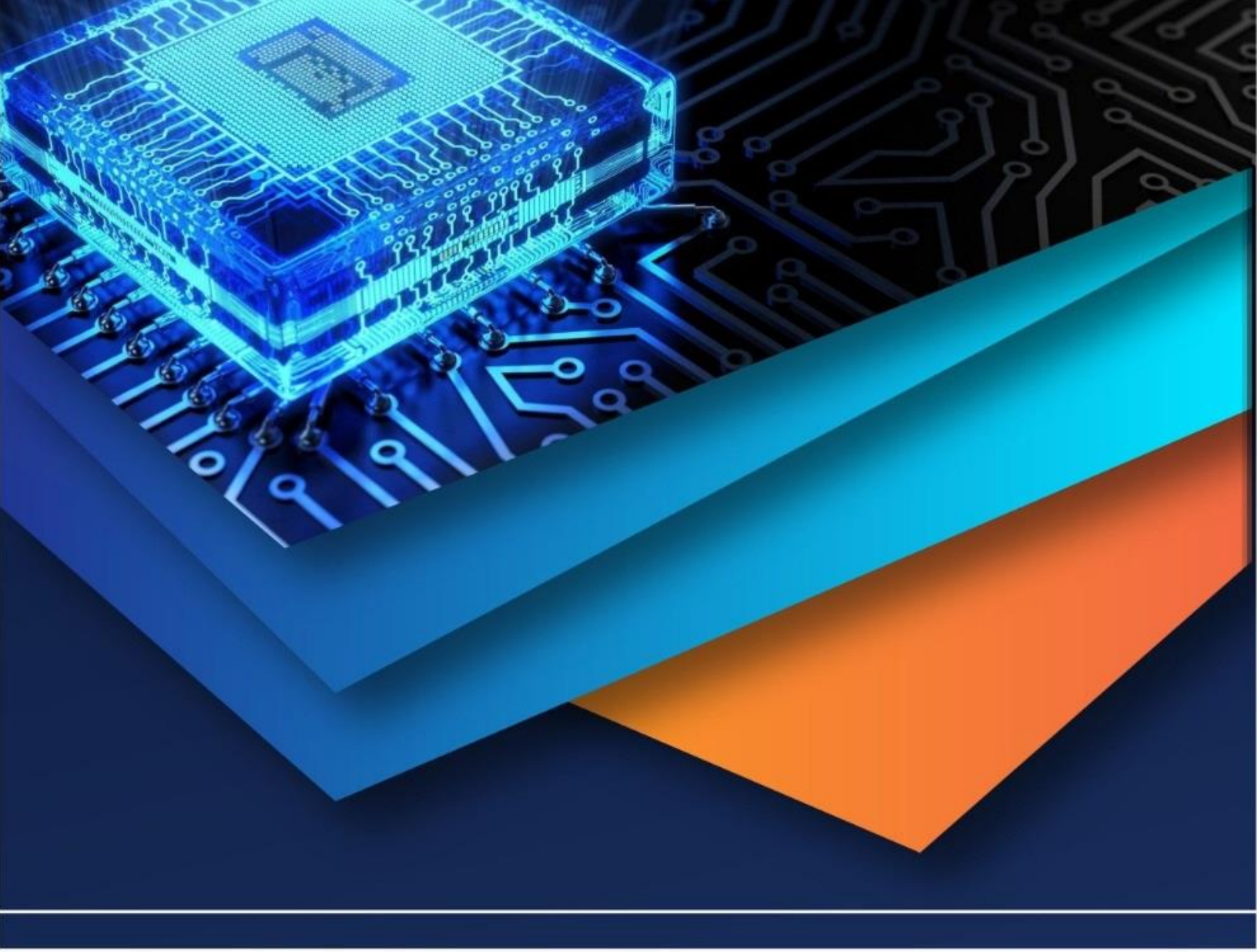

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