iJRASET
International Journal For Research in Applied Science and Engineering Technology

# INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

**Volume:** 9 **Issue:** IX **Month of publication:** September 2021

**DOI:** https://doi.org/10.22214/ijraset.2021.37929

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
*ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429*
*Volume 9 Issue IX Sep 2021- Available at www.ijraset.com*

# FinFET Response under Radiation and Bias Stress: A Review

Uma Bisht[1], Ankit Pawariya[2]
[1]*M.Tech. Scholar,* [2]*Assistant Professor, Department of Electronics and communication, CBS Group of Institutions, Jhajjar (Haryana), Maharishi Dayanand University, Rohtak*

***Abstract:*** ***Electronics devices are made on IC's, the basic building block of these IC's are transistors. Transistors are continuously upgraded to new forms from conventional BJT to the latest FinFET. The purpose of this paper is to provide a clear and exhaustive understanding of the state of the art, challenges, and future trends of silicon based devices to produced reliable output for a longer time period even in abnormal conditions like in space. The modeling techniques for the conventional transistor, different strategies have been proposed over the last years to model the FinFET behavior and increasing the storage capacity of the IC by increasing the number of transistors without occupying more space on the same IC. The behavior of the device is impacted by radiation, heat, and temperature, by which the overall performance of the devices is affected a lot.***
***Keywords: CMOS, MOSFET, FinFET, diode, transistor, subthreshold voltage, threshold voltage, electromigration, and charge trapping.***

## I. INTRODUCTION

**FinFET** is a multigate device. A Fin-shaped field-effect transistor has a fin-shaped body, so it is called FinFET. The channel (fin) of the FinFET is vertical. A simple MOSFET contains substrate, gate, source, and drain. But in the case of a multigate device, the MOSFET device can have a gate on two, three, or four sides of the channel. A double gate structure is made when we cover the channel with gate material from different sides. These devices come under the category of FinFETs. It is because of the shape of the gate which looks like a fin. The benefit of a FinFET device is that it has a high current density and faster switching time than a complementary metal oxide conductor (CMOS).

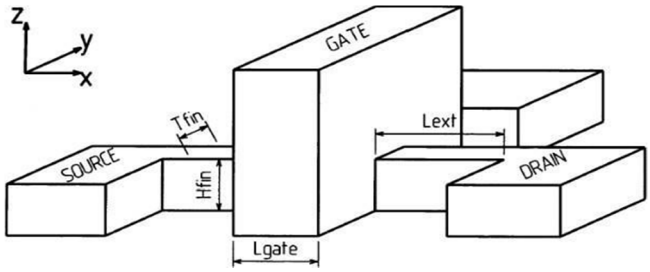


Figure 1 Schematic of a FinFET

FinFETs fabricated with conventional MOSFET technology with the suppression of short channel effects(SCE) and the reduction of parasitic resistances. The manufacturing technology has been so advanced that it allows higher control on transistor's channels. That's why FinFET has become the highly used semiconductor in ICs. FinFET physical structure
has greater computational power because of the higher density of Fin transistor on the same IC chip. In FinFET gate length is 22nm which is less than the conventional MOSFET[1], shorter channel length reduces the reliability of the device, but the gate oxide thickness and applied voltage inappropriate value can reduce the reliability issue in FinFET.

| Performance Parameter | CMOS | FinFET | % change in FinFET in comparision to CMOS |
|---|---|---|---|
| Average power in SRAM read operation(µW) | 124 | 8.76 | 92.93% reduction |
| Average power in SRAM write operation(nW) | 896 | 19.76 | 97.8% reduction |
| Average power in inverter (µW) | 12.8 | 5.2 | 59.83% reduction |

Table 1 Comparison table between CMOS and FinFET

©IJRASET: All Rights are Reserved

1) *Moore's Law and Scaling Theory:* It is an observation which suggests that the number of transistor available in an IC(integrated circuit) gets double in every two years. When the number of transistors increases on the same IC it reduces the cost of the devices also increases the processing speed of the devices.

By increasing the number of transistors in an IC following adages are observed in the performance of the device.

| Parameters | Before Scaling | After scaling | |
|---|---|---|---|
| | | Full scaling | Constant Voltage scaling |
| Channel length | L | L' = L/s | L' = L/s |
| Channel width | W | W' = W/s | W' = W/s |
| Gate oxide thickness | tox | tox' = tox/s | tox' = tox/s |
| Junction depth | Xj | Xj' = Xj/s | Xj' = Xj/s |
| Power supply voltage | VDD | VDD' = VDD/s | VDD' = VDD |
| Threshold voltage | VT0 | VT0' = VT0/s | VT0' = VT0 |
| Doping densities | $N_A$, $N_D$ | $N_A$',$N_D$' = s$N_A$ , s$N_D$ | $N_A$',$N_D$' = $s^2$ $N_A$ , $s^2$ $N_D$ |
| Oxide capacitance | Cox | Cox' = Cox/s | Cox' = Cox/s |
| Drain current | $I_D$ | $I_D$' = $I_D$/s | $I_D$' = s.$I_D$ |
| Power dissipation | $P_D$ | $P_D$' = $P_D$/$s^2$ | $P_D$' = s. $P_D$ |
| Power density | $P_D$/Area | $P_D$/Area' = $P_D$/Area | $P_D$/Area' = $s^3$. $P_D$/Area |

Table 2 change in the parameter of transistor before and after scaling

## II. LITERATURE SURVEY

An intrinsic semiconductor is a pure semiconductor in which no impurity atoms are added. In intrinsic semiconductors number of electrons and hole pairs generated due to thermal excitation or light excitation is equal. From the pure semiconductor, many devices are made like a diode, transistor.

Some of the active and passive components like a transistor, resistors, capacitors, op-amp, etc. are built on a silicon substrate.

The characteristics of a transistor depending on different aspects such as temperature, heat, operating time, doping concentration, radiation, etc. The stability of the transistor is very essential when operated in space applications. The variation in the output current due to applied voltage it should be according to the need of application and region of operation of the transistor.

1) *BJT:* Can be well understood as a back to back combination of diodes. Its voltage and current characteristics are similar to diode i.e. when applied voltage is less it is in an OFF state. In spite of a very old transistor, it is still used in some digital applications over MOSFET. The major drawback of this thermal runaway and instability in collector current.
2) *MOSFET:* MOSFET is a three terminal device. MOS capacitor is the heart of MOSFET. Physics of the parallel-plate capacitor can be used to understand the working of the MOS. A MOS capacitor that contains a semiconductor substrate of p-type, for the fabrication of n-channel MOSFET the substrate is used is p-type and for p-channel MOSFET the substrate or bulk is n-type. Figure 1.1 shows that the top plate of a parallel-plate capacitor is at a negative voltage with respect to the bottom plate. Between two plates, there is a layer of insulator material. With this setting of the electric field, the top plate contains the negative charge while the bottom plate contains a positive charge, and there is an induced electric field between the two plates. By applying different values of the gate voltage MOS capacitor goes to different regions of operation. The Gate terminal is connected to a negative voltage w.r.t the semiconductor substrate. With the help of the parallel plate capacitor, it is very much clear that the top metal plate will contain a negative charge and the dielectric present between metal and semiconductor get polarized by which an induced electric field will exist.

When the applied gate voltage is zero, p-region separates the drain and source terminals. It is very much like two diodes connected back to back. As source and drain is heavily doped $n^+$ regions and the p-type substrate is separating them.

A threshold voltage of a MOSFET is the value of the applied gate voltage at which the drain current starts flowing by taking care of $VDS$ value. When $VG$ is less than the threshold voltage ideally no current flows.

$$V_{TO} = \Phi_{FB} - 2\Phi_F - \frac{Q_{B0}}{C_{ox}} - \left(\frac{Q_{ox}}{C_{ox}}\right) - \left(\frac{Q_{it}}{C_{ox}}\right)$$

Subthreshold drain current of a MOSFET flows in a region when MOSFET is in a weak inversion region and the applied gate voltage is less than the threshold voltage. It is practically observed that the drain current is not zero.

©IJRASET: All Rights are Reserved

3) *Types of MOSFET:* In enhancement type MOSFET no pre-existing channel is present like depletion mode MOSFET. In enhancement type MOSFET, inversion layer is created when the gate voltage*is greater than or equal to the threshold voltage of MOSFET and the channel is having electrons at the interface greater than the holes in the substrate, that's why this layer is called the inversion layer. Vth is the threshold voltage of a transistor, for n type MOSFET, the threshold voltage is defined as the amount of voltage required to applied at the gate region such that an inversion layer formed between source and drain region with carrier density equal to the concentration of the majority carrier in the substrate. When an inversion layer is formed, only after applying proper voltage to drain and source terminal current can flow between the source and drain terminals. So we can say that threshold voltage is the minimum voltage required to turn on the transistor (when the gate voltage is less than the threshold voltage MOSFET is OFF device).
4) *CMOS:* By the use of CMOS DC power dissipation can be minimized. CMOS has a very high noise margin and high packing density so it is preferred over Bipolar IC. CMOS can be fabricated in any of three ways (a) p well (b) n well (c) twin well. Twin well is better in comparison to p well and n well because of higher packaging density. MOSFET is a very basic element in most of the silicon based technologies, including CMOS (Complementary MOS) and for most of the integrated circuits. MOSFET is having very small in size so they need a small area of a silicon IC chip. CMOS is one of the basic and important applications of MOSFET. Alone CMOS has dominated the integrated circuit technology for more than 30 years. CMOS technology has completely replaced NMOS and PMOS.

## III. DEGRADATION IN ELECTRICAL PROPERTIES OF TRANSISTOR

The main reason of degradation in transistor electrical property are mentioned below.

1) *Electro Migration:* When a high value of current density travel via metal interconnect, it is possible the momentum carried by current carried e- transferred to the ions of the metal. It happens due to the collision between the metal ion and current carrying electrons. Because of the momentum transferred to the metal ion, there might be a little drift in the position of the metal ion in the direction of momentum transferred. Such a drift causes the electromigration effect. For smaller channel length, the metal interconnection area also shrinks. In this case, the issue of electromigration increases.

When we use a device for a longer duration, this kind of drift keeps on accumulating. It keeps on worsening and causes $VTH$ shift in the aged device.

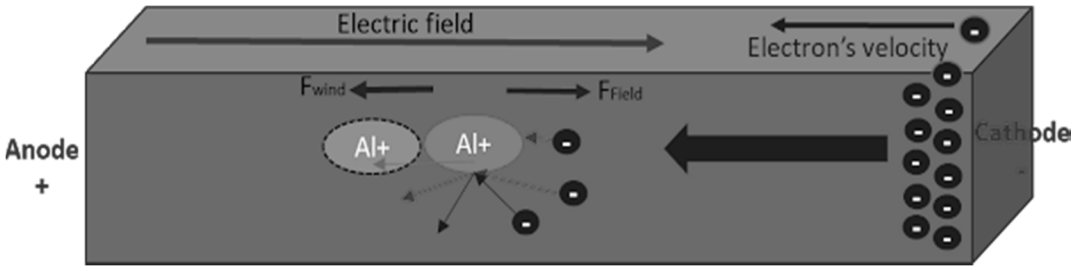



Figure 2 Electro Migration in the metal interconnect

2) *Charge Trapping:* A charge trap is an imperfection in the semiconductor that creates an electronic state locally near the imperfection site. It is distributed energetically in the bandgap of the semiconductors. The depth of the trap depends on the relative energetic position of the bandgap. These traps can be created in many ways. Electromagnetic radiation is one of them. It can be created because of structural defects and chemical impurities. These kinds of traps are known as intrinsic traps, while the traps generated by electromagnetic radiation, bias stress, or temperature gradient are known as extrinsic traps.

## IV. IMPACT OF RADIATION ON THE TRANSISTOR PARAMETERS

### A. *Threshold Voltage Shifts*

Since radiation interface trapped charge ($N_{it}$) and induce oxide trapped charge ($N_{ot}$) and therefore, it can cause $V_{th}$ to shift for both NMOS and PMOS. The effect of $N_{it}$ and $N_{ot}$ adds for PMOS and subtract for NMOS transistors. The number of traps, of both kinds, depends on various factors like temperature, post-irradiation time. That can vary the $V_{th}$ of device.

©IJRASET: All Rights are Reserved

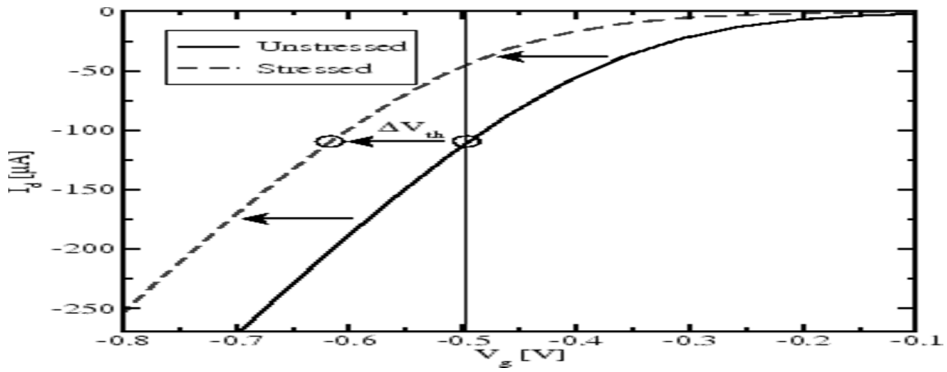



Figure 3 Threshold voltage shift in a MOSFET due to stress

*B. Sub-Threshold Slope*

*NIT* and *NOT* also have an impact on the Sub-threshold region of the transistor. Because of non-uniform deposition of charge, there will be the non-uniformity in Not which impact the device in the subthreshold region. When the device is in the saturation region its current variation is flat with respect to drain-source voltage but due to the sub-threshold effect, there is some change in drain current.

It can cause an increase in the leakage current and a lot of heat dissipation in the IC hence the device degradation.

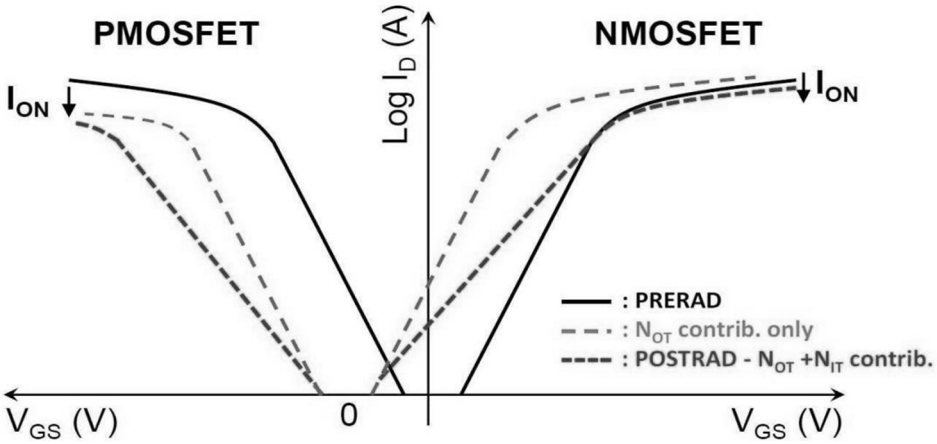



Figure 4 Ion shift in a MOSFET due to radiation

*C. Gate Oxide Stability and Breakdown*

Trapped induced by radiation also affect the leakage current through gate oxide and also can have an adverse impact on oxide breakdown voltage. It has been reported that the trapped charges reduce the oxide breakdown voltage and cause the higher leakage current. This occurs due to “electron trap-assisted” tunneling for TDI (total dose irradiation).

Figure 5 of charge trap in gate oxide

## V. CONCLUSION

Gamma radiation impact was observed on Si Bulk FinFET and characteristic variation is observed it is found that the threshold voltage is increased and gated leakage current is also increased by which its reliability of the device is decreased. By different biasing stress on FinFETs before radiation has generated an extra number of defects at the interface. So, when radiated the stressed device, because of the extra number of defects, it generates a relatively large number of interface traps and hence a positive shift in threshold voltage. Due to radiation, a large number of free electrons and holes are created by which leakage current is increased.

©IJRASET: All Rights are Reserved

## VI. WHAT IS NEXT?

The scope of electronics devices made by FinFET is very promising and will be helpful in complex computation. The problem due to radiation can be mitigated by using different methods like replacing substrate instead of silicon. But that element should be as economical, easily available, having better thermal stability than silicon.

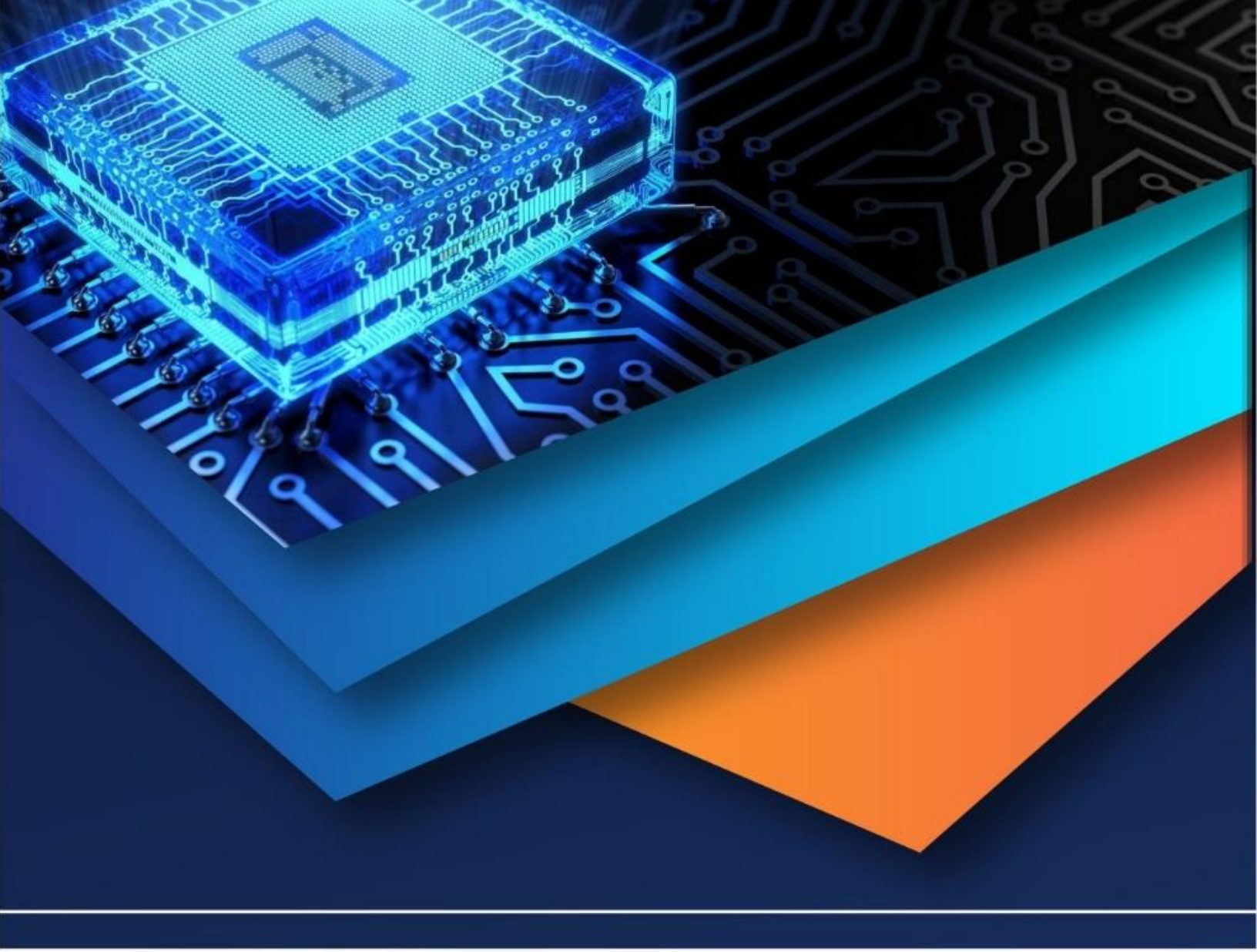
Here we observed a change in response of FinFET by exposing the transistor to gamma radiation. This can also be done for various radiation coming from space and observe the change in the behavior of the device.

FinFET is having a very small leakage current in comparison to MOSFET but this can be improved in the future by doing more research in this field. For this the transistors are can be tested for various applications, also by operating in different temperature range and different range of voltage is applied so that the performance of FinFET can be improved.

## REFERENCES

[1] Cheng T. Wang, Hot Carrier Design Considerations for MOS Devices and Circuits, Van Nostrand Reinhold, 1990.
[2] Y. Nissan-Cohen, J. Shappir, and D. Frohman-Bentchkowsky, \Trap Generation and Occupation Dynamics in SiO2 under Charge Injection Stress," J. Appl. Phys., vol. 60, no. 6, pp. 2024{2035, Sept. 1986.
[3] Brian Doyle, Marc Bourcerie, Jean-Claude Marchetaux, and Alain Boudou, Interface State Creation and Charge Trapping in the Medium-to-High Gate Voltage Range (Vd _ Vg _ Vd) During Hot-Carrier Stressing of n=MOS Transistors," IEEE Transactions on Electron Devices, vol. 37, no. 3, pp. 744{754, March 1990.
[4] L. Lipkin, A. Reisman, and C. K. Williams, \Hole Trapping Phenomena in the gate Insulator of As-Fabricated Insulated Gate Field E_ect Transistors," J. Appl. Phys., vol.68, no. 9, pp. 4620{4633, Nov. 1990.
[5] S. J. Wang, J. M. Sung, and S. A. Lyon, \Relationship Between Hole Trapping and Interface State Generation in Metal-Oxide-Silicon Structures,"Applied Physics Letters, vol. 52, no. 17, pp. 1431{1433, April 1988.
[6] S. Lai, \Two-Carrier Nature of Interface-State Generation in Hole Trapping and Radiation Damage," Appl. Phys. Lett., vol. 39, pp. 58, 1981.
[7] Y. Roh, \Interface Traps Induced by Hole Trapping in Metal-Oxide Semiconductor Devices," J. Non-Cryst. Sol., vol. 187, pp. 165{169, 1995.
[8] Eiji Takeda, Hitoshi Kume, Toru Toyabe, and Shojiro Asai, \Submicrometer MOSFET Structure for Minimizing Hot-Carrier Generation," IEEE Transactions on Electron Devices, vol. ED-29, no. 4, pp. 611{618, Apr. 1982.
[9] Y. H. Lho, K. Y. Kim, “Radiation Effects on the Power MOSFET for Space Applications,” ETRI Journal, vol. 27, no. 4, Aug. 2005, pp. 449-452. DOI: 10.4218/etrij.05.0205.0031
[10] J. R. Schwank, M. R. Shaneyfelt, D. M. Fleetwood, et al., “Radiation Effects in MOS Oxides,” *IEEE Trans. Nuclear Science*, Vol. 55, no. 4, pp. 1833-1853, 2008.
[11] H. L. Hughes, J. M. Benedetto, “Radiation Effects and Hardening of MOS Technology: Devices and Circuits,” *IEEE Trans. Nuclear Science*, vol. 50, number. 3, pp. 500-521, 2003.

©IJRASET: All Rights are Reserved



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

# INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Call : 08813907089 (24*7 Support on Whatsapp)