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4-bit Carry Look Ahead Adder Using MGDI Technique

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Abstract: ***Today's high-performance processor is built with arithmetic logic units that add and subtract key components. Design considerations related to low power and high performance digital VLSI circuits have become more prevalent in today's world. In order to develop low-power and high-performance processors, the designers need to design their adder circuits with the required speed and power dissipation for their applications. This topic introduces the concept of a adder using MGDI Technique. The Exact Speculative Carry Look Ahead Adder the use of the Modified-GDI (Modified-Gate Diffusion Input) is cautioned in this work. The delay, location and energy trade off performs a integral role in VLSI. We already comprehend that designs which are of CMOS fashion occupy extra area might also eat extra strength consumption. The switching conduct of the circuit reason the heating up of integrated circuits affects the working stipulations of the purposeful unit. The adders are the most important parts of countless applications such as microprocessors, microcontrollers and digital signal processors and additionally in actual time applications. Hence it is necessary to minimize the adder blocks to format a perfect processor. This work is proposed on a 16 bit carry seem to be in advance adder is designed through using MGDI gate and 4T XOR gates and a speculator blocks. The proposed MGDI raise Look Ahead adder occupies 68% much less region and the strength consumption and the propagation extend additionally considerably reduces when in contrast to the traditional carry Look Ahead adder why because the variety transistors extensively reduces from 1448 (Conventional) to 456 (Proposed CLA). The simulation consequences of the proposed format carried out in Xilinx.***

Keywords: Delay, power dissipation, voltage, transistor sizing.

I. INTRODUCTION

The main objective of VLSI design is to improve the efficiency and minimize the area and power consumption. Low power is an emerging phenomenon that can improve the overall performance of a battery. Modified- GDI is a technique that was introduced to enable fast low-power circuits with low-voltage input. This approach can improve the logic level swing and static resistance characteristics and lower the power consumption. Using the MGDI technique, we have created gate and XNOR gate for our design. These gates were designed to provide 4-bit carry look ahead adder. Modified Gate Diffusion I (MGDI) technique is a modified version of the General Gate Feedback (GDI) method. This procedure involves the use of NMOS and PMOS transistors to produce a modified gate. In recent superior applications of VLSI applied sciences in audio and video process, microprocessors and digital signal technique etc., arithmetic operations are used. Before, VLSI functions have been principally addicted to space, dependableness and fee alternatively of power. Demand for low strength increased and thanks to modern boom of digital product like portable cell phones, laptops and alternative gadgets needs excessive speed and low power consumption. The primary draw back in portable gadgets was that it ate up excessive power that end result in less battery lifestyles and caused failure in semiconducting material factors of the devices. To regulate the warmness dissipation, the machine needs excessive packaging charge and cooling necessities. Full-adder is a combinational circuit with three inputs. The fundamental two inputs are A and B, the 0.33 enter Cin represents the carry. The two outputs are selected by the Sum (S) and Carry (C). Sum offers the values of least full-size bit and Carry offers values of most substantial bits. A pair of XOR gates, a pair of NAND gates and one OR circuit the full adder circuit is constructed. The below are the sum and carry functions of conventional full adder and fig(1) shows the block diagram of 1-bit full adder.

SUM=A XOR B XOR C

COUT=AB + C (A+B)

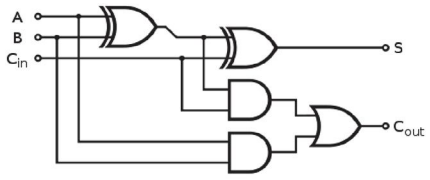

Figure. 1 Full adder block diagram.

Table 1. Truth table of full adder

INPUTS			OUTPUTS	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

II. OBJECTIVE

A. Design of single bit full adder using MGDI technique and comparative evaluation in the terms of power.
B. The graph of full adder the usage of three extraordinary MGDI techniques are applied in this project.
C. Speculative MGDI carry look ahead adder
D. Transmission gate full adder.
E. Pseudo NMOS full adder (Proposed design).
F. A full adder to be designed the use of traditional MGDI technique that is complementary CMOS structure. Then Transient evaluation is to be performed and propagation extend and common power consumption are to be calculated by the usage of the tool.
G. Pseudo NMOS technique is regarded to design the full adder. This proposed graph be optimized in terms of delay when in contrast to traditional CMOS design.
H. A full adder to be applied the usage of Carry Look Ahead adder which is based on the XOR gate architecture.
I. The Total Power and propagation delay extend are to be in contrast with the distinct full adder designs

III. BACKGROUND

A single bit full adder operation and also the reality desk is explained in CMOS VLSI trend textbook. The expression for the adder is carried out in the paper for trendy CMOS approach and for pseudo NMOS approach [1]. Analysis and contrast of 4 architectures with actually one of a kind logic designs (Conventional, transmission gate, fourteen semiconductor units and GDI based totally technique) for transistor counts, electricity dissipation, prolong and electricity lengthen product. It is carried out in virtuoso Cadence. The region optimized via thinking about the applicable transistors dimension for PMOS and NMOS [2]. The goal is to scale back power and prolong of a full adder with the aid of one bit full adder patterns and techniques. A comparative evaluation is tested for electricity and lengthen with definitely awesome range of transistors that is employed to amplify the battery life. The adder circuit is designed and carried out in the virtuoso platform [3]. The overall overall performance of eleven 1-bit full adder cells supported specific frequent sense designs vicinity unit evaluated. The work consists of analysis usual overall performance of a range of good judgment designs as accurate as enter take a look at sample that location unit analysed wondering about the lengthen and power-delay product. Cadence Virtuoso ecosystem is employed for growing schematics. All the analyses proven that 10-Transistor full adder selections sensible lengthen performance, represents greater prolong product and consumes lower electrical energy as in contrast to whole eleven full adder [4]-[5]. A comparison of special full adder circuits is analysed. Full adder circuits area unit relatively utilized in digital style. The a range of types of full adder like trendy CMOS, EXOR and EXNOR, ignore transistor unit common sense gate diffusion method had been performed. Among these, GDI strategy took much much less vary of transistors and so fed on lots less power. In GDI – 14T, 12T and its supported MUX is implemented. The electricity consumption was once once lots less for 12T whereas larger output is offered for 10T. Simulation was performed 90nm science with mentor snap shots device [6].

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IV. METHODOLOGY

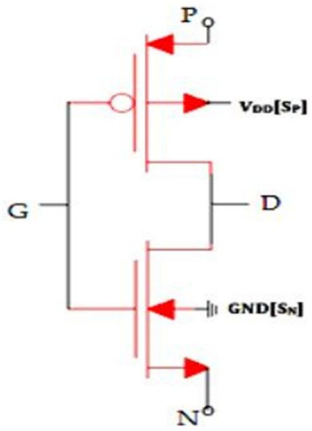

Fig. 1.Modified GDI cell

Table I. Functions implemented byusing MGDI cell

N	SN	P	SP	G	OUTPUT	FUNCTION
0	0	1	1	A	$\bar{A}$	NOT
B	0	0	1	A	AB	AND
B	0	A	1	A	A+B	OR
B	0	A	1	S	$A\bar{S}$+BS	2X1 Multiplexer

There are many architecture to implement a full adder. Every architecture offers some advantages at the same time they have some demerits. So, a designer has to concentrate on a particular parameter before implementing a design approach. During this Design different types of full adders are simulated and designed.

A. Existing Method

he traditional inexact speculative adder for n-bit addition is given in Fig. 2 In this figure, the n-bit input are divided into 4-bit blocks with the cost of x = four For the x-bit adder, the blocks feed the cost of operands. Unlike the conventional ISA architecture, the adder unit has been changed with 4-bit CLA ensures the excessive velocity working conditions. In the following paragraphs, explanations with details of blocks alongside with a variety of sub modules of the present adder are given. Adder Blocks and Speculators: Before discussing the circuits, arrangements and functions of the ESA, it is required to be aware of some of the notations. The addition operands for addition are named as A and B for an n-bit adder with A = { 0, 1, ... −1} and B ={ 0, 1, ... −1}; Here, the sum output are expressed as S = {0,1, ...−1}. Fig. 2(b) represents the speculator block at gate level illustration which is used in this paper as a speculator. This block is based totally on CLA logic to speculate the output lift for every 4-bit adder block. Speculation is carried out for 'r' MSB bits of each block where r is much less than the measurement of block, input elevate for each speculator block is zero (or 1) which introduce superb (or negative) errors respectively. The output carry, which is denoted as, from each speculator block is fed as an enter elevate for the adder block succeeding it, as proven in Fig.2. Now, every 4-bit adder block need no longer wait for the enter elevate from the preceding 4-bit adder block. Instead, all such adder blocks function concurrently additions on receiving enter contains from the worried speculator blocks are by and large three blocks these are the adder, speculator and compensator. In the above circuit x bit adder skill it is four bit elevate Look Ahead adder it internally consists of carry technology circuit and also it consists of 4 XOR gates and additionally OR and AND logic gates to generate sum and raise [8-12]. In previous the next full adder can wait till the lift propagated to it because of this the operation or pace may be reduced. Due to this motive one can designed a speculator block to generate the carry to the next stage. The compensator block can generate the corrected sum consequences for the given inputs. By the use of CMOS Technology the above method requires 1448 transistors for a sixteen bit addition. In the above technique it consists of four blocks, every block consists of adder of bit measurement 4, compensator and speculator. All these blocks are designed by way of the use of common sense gates.

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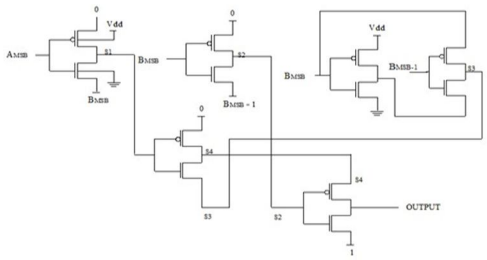

Figure. 2 Speculative Carry Look Ahead Adder Using MGDI Technique.

B. The Proposed Exact Carry Look Ahead Adder

Because of the use of MGDI gates, the proposed technique the variety of transistors can significantly decrease from 1448 to 456 transistors solely primarily based on MGDI technique. Due to this the dynamic power consumption reduces and velocity of the operation additionally increases. The following part will provide an explanation for and suggests the proposed Exact Speculative Carry Look Ahead Adder. In this to get the raise for the next stage a speculator and a two enter or gates are used. Here the whole good judgment gates are designed through using MGDI technique and as an alternative of using 12 transistors, the XOR gates use only 4 transistors to generate the sum bits and the CLA adder, in its inside circuit it consists of 5, 4, three and two inputs based totally AND and OR gates. For instance reflect on consideration on 5 inputs AND gate, to format this it requires 12 transistors in pull up and pull down paths and to get the right output an inverter is attached to it. Hence it will increase the plan place and additionally propagation lengthen increases and pace additionally reduced. In order to keep away from all these types of trade off in the proposed method all the blocks are sketch with only NMOS and PMOS transistors pairs called as MGDI technique. The following will explain the interior blocks of raise Look Ahead adder.

To decrease the strength consumption as nicely as the transistor depend further, any other technique for growing a full adder is used, known as Gate Diffusion Input (GDI). For designing a 1-bit full adder the use of GDI logic, only 5 PMOS and 5 NMOS transistors are required. Because of the use of MGDI gates, the proposed technique the range of transistors can significantly reduce from 1448 to 456 transistors solely based on MGDI technique. Due to this the dynamic energy consumption reduces and velocity of the operation additionally increases. The following part will provide an explanation for and suggests the proposed Exact Speculative Carry Look Ahead Adder. In this to get the lift for the next stage a speculator and a two input or gates are used. Here the total good judgment gates are designed with the aid of using MGDI approach and rather of the use of 12 transistor, the XOR gates use only four transistors to generate the sum bits and the CLA adder, in its interior circuit it consists of 5, 4, 3 and 2 inputs based AND and OR gates. For instance reflect on consideration on 5 inputs AND gate, to design this it requires 12 transistors in pull up and pull down paths and to get the right output an inverter is attached to it.

V. RESULTS AND DISCUSSION

ADDER	PARAMETER	CMOS	GDI	MGDI
	Total Power Dissipation in micro Watt	300X106	724.76	690.2
4-BIT CLA	Propagation delay in ns	165	98	72.44
	Transistor count	294	246	120

Table. 2 Results.

For simulating and comparing the performances of 1 bit full adder with different design topologies, Cadence Design Suite 6.1.6 for GPDK 90nm CMOS technology operating in Virtuoso environment at room temperature was used. For the analysis, the supply voltage VDD was set at 1.8 Volt for each of the full adder. During the simulation, the inputs (A, B, C), pulses with different periods were given which is VPULSE in this software, where the pulses were varied from 0 Volt to 1.8 Volt. Here, in order to compare and inspect the different simulated full adder topologies, the width and length of PMOS and NMOS were set at an indistinguishable value for each of the adder. Length was set at 90 nm.

Width of PMOS and NMOS were set at 2.75 um and 2 um respectively. The width of the PMOS was calculated by parametric analysis of Wp (A variable for the width of PMOS) versus average propagation delay with respect to a CMOS inverter. With that analysis it was found that the average propagation delay is minimum for the PMOS for the width of 2.75 um. Keeping the CMOS inverter as a reference the width of the PMOS in the design are set accordingly. Transient analysis was done to verify the adding process by observing how sum and carry is changing with the given input (A, B, C) values. Delay was also calculated by monitoring the transient response. Performing DC analysis the power consumptions by the adder circuits were obtained.

Type of 16 bit CLA	Technology	Operating Clock Frequency	Device Count	% of Area utilization
CMOS based CLA	90 nm	224.57 MHz	1448	--
Proposed - MGDI based CLA	90 nm	344.64 MHz	456	68 %

Table 3: Comparative analysis of conventional CMOS and proposed CLA

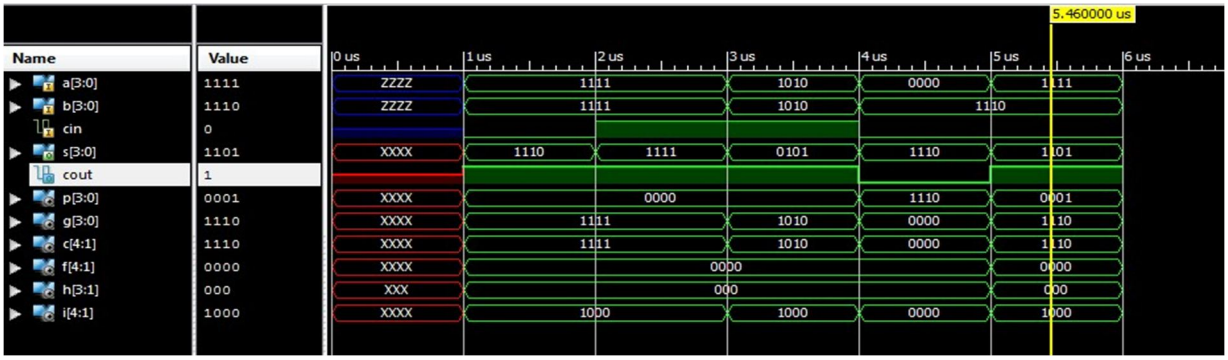

Fig.5 : Simulation result of 4 bit Exact Speculative Carry Look Ahead Adder

From the Table 3, in phrases of lengthen carried out of transient analysis, transmission indicates the great overall performance among all others but it has giant amount of strength consumption. The conventional CMOS full adder offers the full swing voltage but the lengthen is extra due to the parasitic capacitances and also power is more due to static leakage current. In the proposed layout i.e., the Pseudo NMOS design is implemented by using using the equal expression used in the traditional CMOS adder but with a one of a kind technique. In the proposed graph the area and lengthen is optimized when in contrast to the traditional CMOS adder circuit, but has the pull-up system is constantly ON there will be more static current which can be eradicated via the use of dynamic circuits thinking in the future.

VI. CONCLUSION

Low area and high speed speculate CLA adder type of the Adder logic was presented. This design has been proposed to increase the speed of the operation and reduce power consumption and reduce the area when compare to all other types of adders. Experimental results showed that the proposed one with a maximum frequency of 344.64 MHz and the conventional adder operates at a frequency of 224.57 MHz in 90nm ASIC. And Parallelly the proposed method reduces the transistor count drastically from 1448 to 456 transistors only i.e., 68% lesser then the existing method. By using this MGDI technique the power consumption and area reduces when compared to the CMOS technology. The design works with a considerably good role in the design of consumer electronics as well as future trending electronic gadgets for IoE and many other modern-day applications. However, the power issue can be eliminated by some extent using suitable design approaches.

Here in the paper, special full adder circuits are designed and simulated for power consumption and delay. The proposed full adder is the Pseudo NMOS full adder which is faster than the traditional CMOS full adder. The place of Pseudo NMOS full adder is lesser than the CMOS traditional full adder as in less transistors are used. Comparatively, the transmission gates affords advantages in both power consumption and delay. For distinct applications, a unique full adder structure is used. In the proposed full adder extend is optimised but the power consumption is increased. This can be resolved by using the use of sleep transistors to reduce the static energy consumption.

The high performance adder referred to as Synchronous Carry Generate Adder/Carry look-ahead adder is designed by means of the use of existing strategies (CMOS and GDI) and proposed MGDI technique. The functionalities of MGDI primarily based designs have been verified. It is observed from the Table II. that MGDI based totally designs provides less power dissipation, high velocity and require much less no. of transistors. Hence, it is concluded that MGDI based totally adders can be used in high overall performance purposes and can be used in the multipliers.

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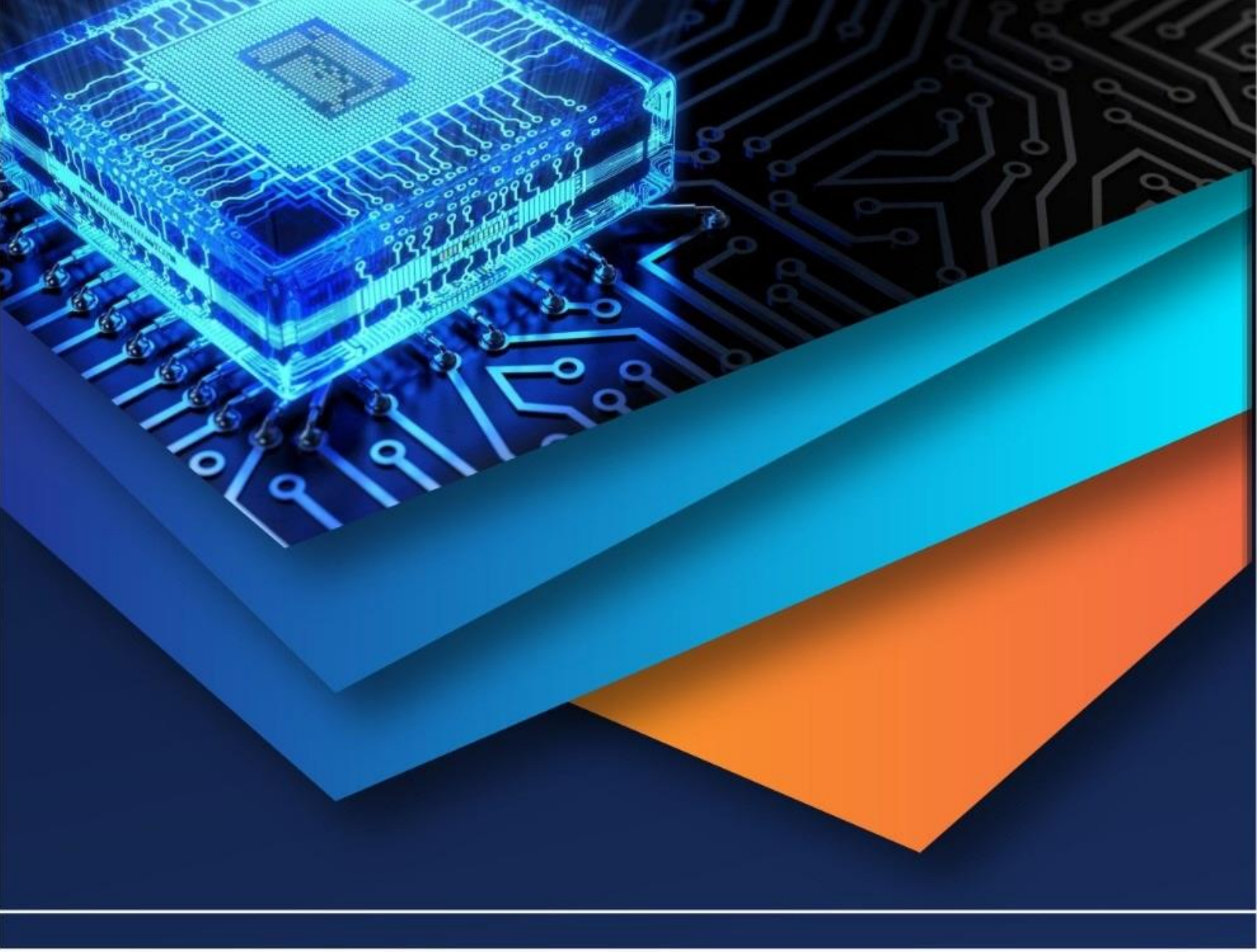

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