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Alternative Criteria of Voltage Stability Margin for the Purpose of Load Shedding

Praveen Kumar[1], Dr. Sunil Singh[2]
[1]*PG Student [Electrical energy system], Dept. of EE, College of technology, GBPUA&T Pantnagar , Uttarakhand, India.*
[2]*Professor, Dept. of EE, College of Technology, GBPUA&T Pantnagar , Uttarakhand, India.*

Abstract: Voltage instability takes on the form of a dramatic drop of transmission system voltages, which may lead to system disruption. During the past two decades it has become a major threat for the operation of many systems and, in the prevailing open access environment, it is a factor leading to limit power transfers. The objective of this paper is to present new method of under voltage protection with maximum utilization of system capabilities.

I. INTRODUCTION

Power system stability is the ability of electrical power system to regain a state of operating equilibrium after being subjected to disturbance. There are three classes of power system stability namely

1) *Rotor Angle Stability:* Which may be a small–disturbance angle stability or transient stability.
2) *Frequency Stability:* Which may be short-term or long-term. Voltage stability - which may be large disturbance voltage stability or small disturbance voltage stability, and both of them may be short term or long term in nature.

Voltage stability is in respect of the ability of power system to maintain steady state voltage at all the buses in the system during normal state and after being subjected to a disturbance. To limit the consequences and prevent development of disturbances, the sound diagnosis of abnormal situation and application of the well-matched preventive actions are needed. It is the principal task of automatic disturbance limiting devices. In many cases, the last line of defense is to initiate load shedding but the under voltage relay used to diagnose the abnormal condition and shedding load the stability margin causes a problem, because the undervoltage criterion is not very discriminative. The under voltage relay operates much below the unstable region and hence the max load capability is not utilized.

II. SCOPE

This project presents a new method of estimating the voltage stability margin, which utilizes local measurements and applies criterion which is based on the very definition of the voltage stability. The under *voltage* relays failed to recognize the unstable region and trip the load way above the max power transfer point hence we have to trip load way more than the required and non reliability problem increases.

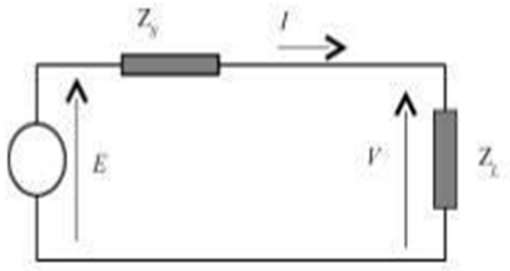


FIGURE-1

Here we are using new criteria and implementing the same to 14 bus system to access the voltage unstable point by measuring source impedance and its ratio with the load impedance and tripping of load when their ratio reaches unity. From this simple circuit we can see that the maximum power transferring capacity is reached when Z_s and Z_L ratio reaches the unity and that is also the point when power transferring capacity of source is void and the voltage collapse starts.

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III. BACKGROUND

Voltage stability has been defined by the IEEE Power System Engineering Committee in the following way: "Voltage stability is the ability of a system to maintain voltage so, that when load admittance is increased, load power will increase, and so that both power and voltage are controllable."

The voltage stability problem is best explained by the equivalent model used because however large and complex the system is it can be reduced to Thevenin equivalent easily by taking the open circuit voltage and short circuit current which we did by introducing a three phase to ground fault at the bus in study.

Then the load power and load voltage can be given by simple equations shown below-

$$V_l = \frac{E \times V_l}{\sqrt{Z_l^2 + Z_s^2 + 2Z_l Z_s \cos\beta}}$$

$$S = \left[\frac{E^2 \times Z_l}{Z_l^2 + Z_s^2 + 2Z_l Z_s \cos\beta}\right]$$

$$\beta = \emptyset_S - \emptyset_L$$

where $\emptyset_S$ and $\emptyset_L$ are phase angle of Z_s and Z_L

for 14 bus system we implemented the same thing and plotted the plot between voltage and power and similarly for Z_s and Z_l

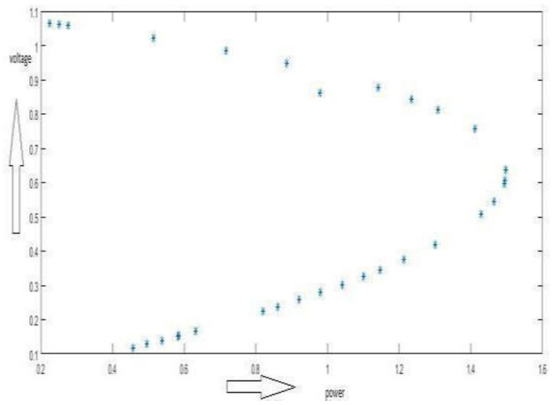


FIGURE-2
Voltage to power (nose curve)

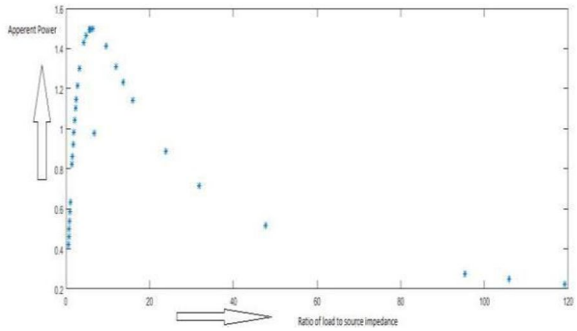


FIGURE-3
Apperent power vs ratio of load to source impedance

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The figures confirm the well-known fact that the critical level of the is unity, which marks the voltage stability limit. At that point, the load power reaches maximum and become

$$S_{mx} = \left[\frac{E^2}{2Z_s(1+\cos\beta)}\right]$$

and the critical voltage has the level

$$V_C = \frac{E}{(2+2\cos\beta)^{0.5}}$$

IV. PREVENTION OF VOLTAGE COLLAPSE

There are various method to prevent the voltage collapse but the aims is particularly same

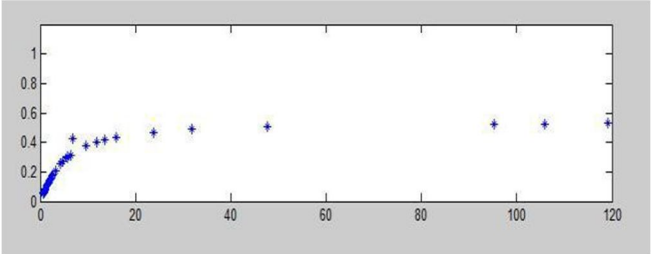


FIGURE-4
Voltage vs ratio of load to source impedance

1) The ratio Z_L and Z_S must be always greater than the critical level of unity .In fact ,the minimal level ought to be selected in such a way that the expected sudden increase of Z_L, or decrease of Z_S should not cause instability.
2) The value of V should be high enough not to make the motors stall

Usually for sensing and tripping of load we are using undervoltage relays which is based on tripping of load when undervoltage reaches beyond a set voltage limit generally set as 0.85E which we can see from above figure is a obviously a drawback as the power factor changes relay will operate way before the actual voltage collapse and power transferring capabilities of system remain underutilized.

In practical applications, load shedding is initiated by the under voltage relays However ,this solution has an obvious drawback, which is clear while looking at figure above For

a given $\left[\frac{Z_L}{Z_S}\right]$ the level of voltage depends to a large degree on the angle . Therefore, if assuming a fixed level of the undervoltage relay setting let it be-0.85E the relay as seen from figure-4 will trip way before the max value. To avoid this, the adaptive setting of the undervoltage relay may be adopted. To overcome the poor discrimination capabilities of under voltage relay we should exploit β dependence of voltage but the continuous measurement of Z_s is posing problem hence in this project we used the improved measurement of Thevenin impedance which is based of the definition of voltage stability.

V. ESTIMATION OF VOLTAGE STABILITY MARGIN

Estimation of the stability margin may be based on the very definition of the voltage stability. If, for the equivalent circuit one calculates the derivative of apparent load power against the load admittance, the following result is obtained:

$$\frac{dS}{dY} = \frac{V^2[1-(Z_sY)^2]}{1+(Z_sY)^2+2Z_sY\cos\beta}$$

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Where Y=1/Z_L

If both sides of the equation are divided by the value of V^2 , one gets

$$\frac{dS^*}{dY^*} = \frac{1-(Z_s Y)^2}{1+(Z_s Y)^2 + 2Z_s Y\cos\beta}$$

Where

$$\frac{dS^*}{dY^*} = (Y/S)$$

then from above equation $\left[\frac{Z_L}{Z_s}\right]$

can be calculated as

$$\frac{Z_L}{Z_s} = \frac{M+1}{-M\cos\beta + [(M\cos\beta)^2 - M^2 + 1]^{0.5}}$$

$$M=\left[\frac{dS^*}{dY^*}\right]$$

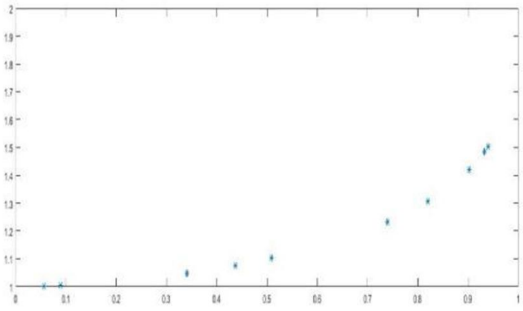


FIGURE-5
M vs ratio of load to source impedance at β=73

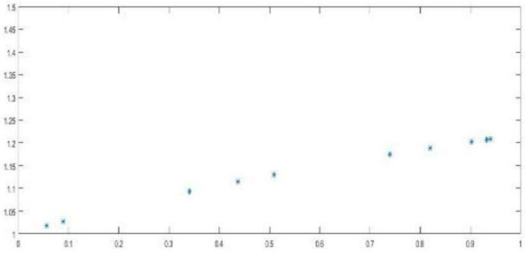


FIGURE-6
M vs ratio of load to source impedance at β=80

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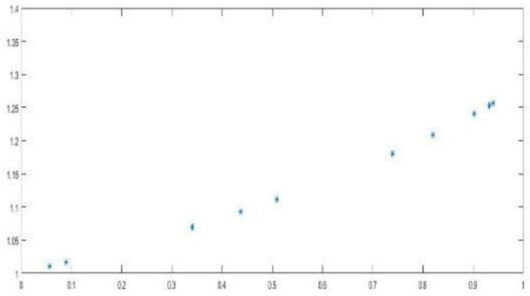


FIGURE-7
M vs ratio of load to source impedance at β=87

The relations between $\left[\frac{Z_L}{Z_s}\right]$ and M (Fig) depend on the angle The value of may be obtained by means of measuring the load phase angle and estimating the source phase angle .The accurate value of $\emptyset_c$ depends on the actual configuration of the system, but in most practical cases, one may assume that it is equal to 80±7 . It means, that the phase angle of the equivalent Thevenin source impedance may vary between 73 and 87.

One may note that even if the source impedance angle is estimated with the error ±7 the value of

$\left[\frac{Z_L}{Z_s}\right]$

is determined accurately enough to make a decision related to load shedding. The accuracy becomes particularly high if the measured factor M is small (below 0.6) and increases with an increase of the load phase angle Alternatively, if the value of E is known, what unfortunately is a rare case , may be calculated using the above derived equation .The final result becomes

$$\frac{Z_L}{Z_s} = \frac{1}{\left[1 - M\left(\frac{E}{V}\right)^2\right]^{0.5}}$$

The whole approach is based on the measuring variation of the power S and the load admittance Y in fact, variation of the load admittance is almost continuous It is caused by natural tripping of load, and it also results from the operation of the transformer tap-changing devices. However, it always occurs in smaller or larger steps. Therefore, the factor may be calculated by the following formula:

$$\left(\frac{dS^*}{dY^*}\right) = \frac{(S_2 - S_1)(Y_2 + Y_1)}{(S_2 + S_1)(Y_2 - Y_1)}$$

M=

where

S_2, Y_2 load and admittance at the end of change (time);
,load and admittance at the beginning of change (time).

VI. CONCLUSION

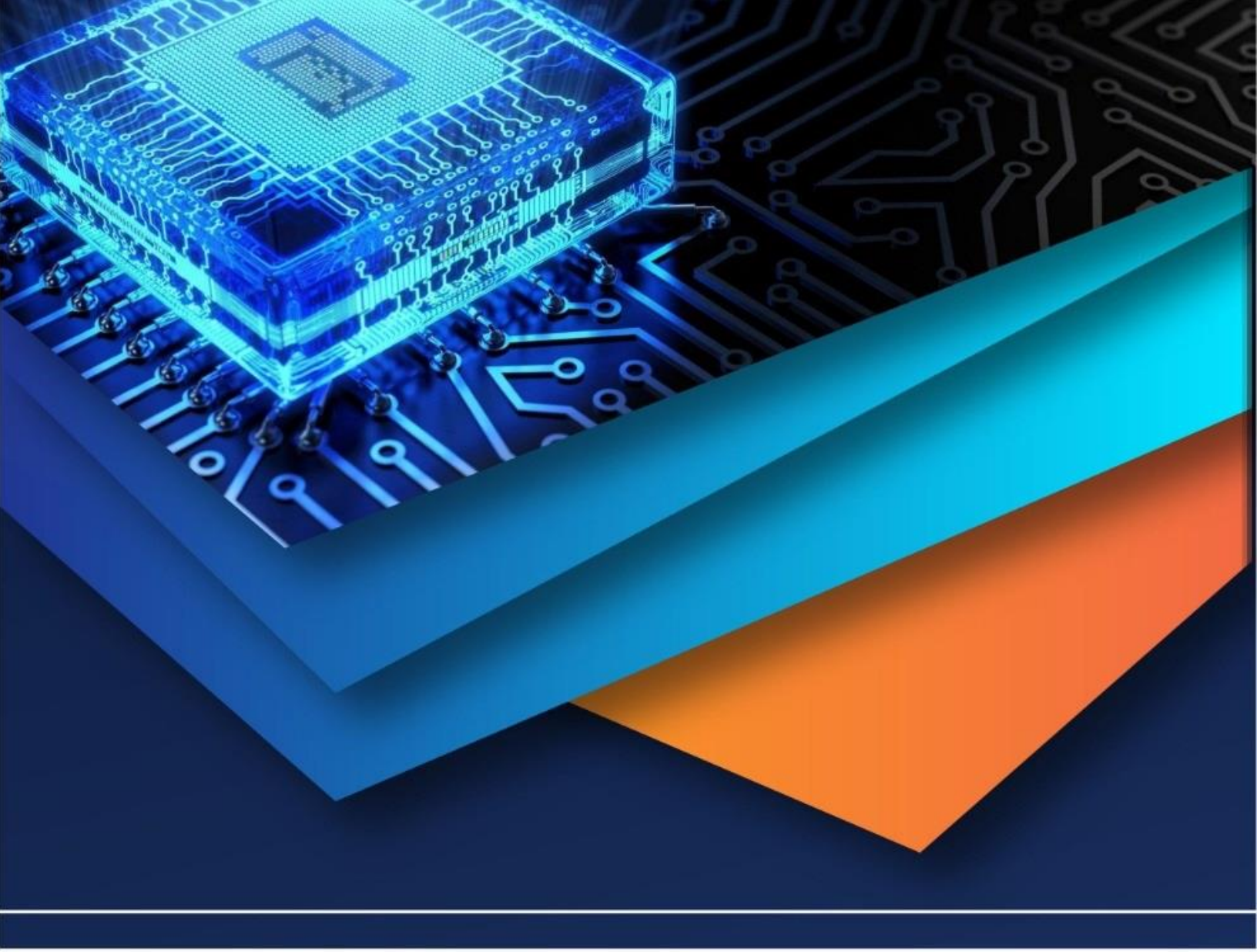
In this project, we implemented a method to find load to source impedance ratio for any given loading condition and based on it estimated the inception of the voltage instability point to a sufficient degree of accuracy. This was implemented for a standard 14 bus IEEE system for loads
attached to 13th bus and 14th bus , and it was found out that
14th bus encountered voltage instability earlier than 13th bus. Further, this load to source impedance ratio online measurements can be fed as a control signal to the relays controlling the circuit breaker attached to the load bus as well as to control tap changing transformers. This allows better utilization of power at the load bus in case of overloaded conditions.

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