iJRASET
International Journal For Research in Applied Science and Engineering Technology

# INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

**Volume:** 9 **Issue:** XI **Month of publication:** November 2021

**DOI:** https://doi.org/10.22214/ijraset.2021.38363

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
*ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.429*
*Volume 9 Issue XI Nov 2021- Available at www.ijraset.com*

# Design and Analysis of CMOS Phase Lock Loop (PLL) Using VLSI Technology

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***Abstract:*** ***This paper proffers comparative research of Complementary MOSFET (CMOS) of the Phase Lock Loop (PPL) circuit. Our approach is based on hybrid design Phase Lock Loop (PLL) circuits combined in a single unit. A phase-locked loop (PLL) is used in space communication for synchronization purposes also very useful in time to digital converters and in instrumentation engineering. A phased lock loop (PLL) is a control system that makes an output signal whose frequency depends on the input phase difference. The phase detector takes the phase of an input signal and compares it with the phase procured from its output oscillator regulates the frequency of its oscillator to manage the phase matches. Different techniques like analogue and digital simulation with the help of mathematical/logical connections are found in Research to create the Phase Locked Loop (PLL). This limitation can be overcome by replicating the circuit block whose supply voltage is being reduced to manage the same throughout. This paper includes design features for low power phase-locked loop using Very-large-scale integration (VLSI) technology. The signal from the phase detector controls the oscillator in a feedback loop. As such: an operational device the PLL has a wide range of applications in computers sciences, telecommunication, and electronic system applications; we aim to design and examine the phase lock loop circuit in multiple technologies and examine their power capacity. By using the hybrid structure of NMOS and PMOS, here we have achieved the circuit of Phase Lock Loop (PLL) using VLSI technology.***
***Keywords: Technology, CMOS, Phase lock loop, Micro wind, Voltage control oscillator, VLSI technology.***

## I. INTRODUCTION

Phase Lock Loops (PLLs) are very versatile and preferred over other methods of maintaining phase lock such as injection locking. For clock- &-data recovery Monolithic phase-locked loops have been used in the communication system, clock generation & distribution in microprocessors, and frequency organization in a wireless application. The Phase-locked loop (PLL) is a feedback system shown in the figure. Mobile phones contain up to 5 PLL's as it is basic building brick used in communications systems. Another essential utilization is in motor speed control and for optical disk drives (ODD's) as found in DVDs and CD players.

Microwind is Electronic design automation software containing IC (Integrated Circuit) designs from the idea. Microwind blends traditionally separated front-end and back-end chip design into an integrated flow, quickening the design cycle and shortened design complexities. It directly couples mixed-signal implementation with digital implementation, transistor-level extraction, circuit simulation, and verification. We have carried simulations and outcomes were examined on 0.12nm, 12nm, 32nm, 45nm, 65nm, and 90nm Microwind using EDA (Electronic design automation) tool.

The Microwind 3.1 Software employed in the paper permits us to design and simulate an integrated circuit at the physical description level. To view and simulate analogue ICs and common logic, Microwind libraries are used. It also incorporates all the commands for a mask editor as well as original tools never gathered before in a single module such as 2D and 3D process view, Verilog compiler, tutorial on MOS devices. The electrical extraction of the circuit is automatically fulfilled and the analogue simulator delivers voltage and current curves instantly also we can access Circuit Simulation by pressing one single key.

## II. BLOCK DIAGRAM

The basic Phase Lock Loop (PLL) can be analog or digital. A phase locked loop (PLL) is used for different purposes in various sectors such as telecommunication and instrumentation. In the microwave range they are used in frequency synthesis and phase recovering among others. To maintain a well-defined phase and hence frequency relation between two independent signal sources, phase-locked loop can be used. Basic PLL consists of three elements: a phase detector, a loop filter and a voltage-controlled oscillator (VCO) as shown in figure 1. As it called as wireless transmitter and receiver, it must be able to produce a large frequency range to up convert and down convert the outgoing and incoming data.

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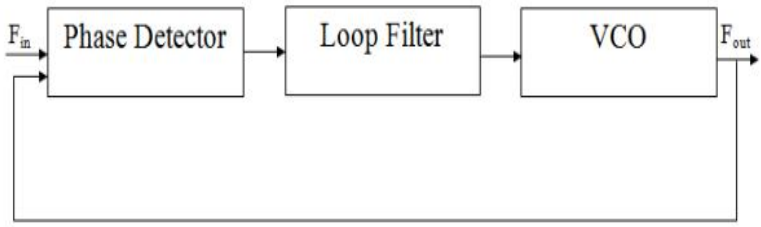


Fig 1. Block Diagram of Phase Locked Loop (PLL)

Phase detector produces a DC voltage, which is proportional to the phase difference between the input signal having frequency of $f_{in}$ and feedback (output) signal having frequency of $f_{out}$.

A Phase detector is a multiplier and it produces two frequency components at its output − sum of the frequencies $f_{in}$ and $f_{out}$ and difference of frequencies $f_{in}$ & $f_{out}$.

An active low pass filter produces a DC voltage at its output, after eliminating high frequency component present in the output of the phase detector. It also amplifies the signal.

A VCO produces a signal having a certain frequency, when there is no input applied to it. This frequency can be shifted to either side by applying a DC voltage to it. Therefore, the frequency deviation is directly proportional to the DC voltage present at the output of a low pass filter.

## III. PHASE LOCK LOOP (PLL)

There are standard implementations with various logic styles that have been used in the past to design Phase Lock Loop (PLL) and these are used for comparison in this paper. Although they all have similar function, the way of producing the intermediate nodes and the outputs, the loads on the inputs and intermediate nodes and the transistor count are varied. The fundamental distinction between the pass-transistor logic design and also the complementary CMOS logic design is the main aspect of the pass logic electronic transistor network which is connected to some input signals rather than the facility lines. the phase locked loop using 45nm technology. This PLL is designed with Microwind 3.1 software using 12 nm design rule.

### *A. Experimental Setup*

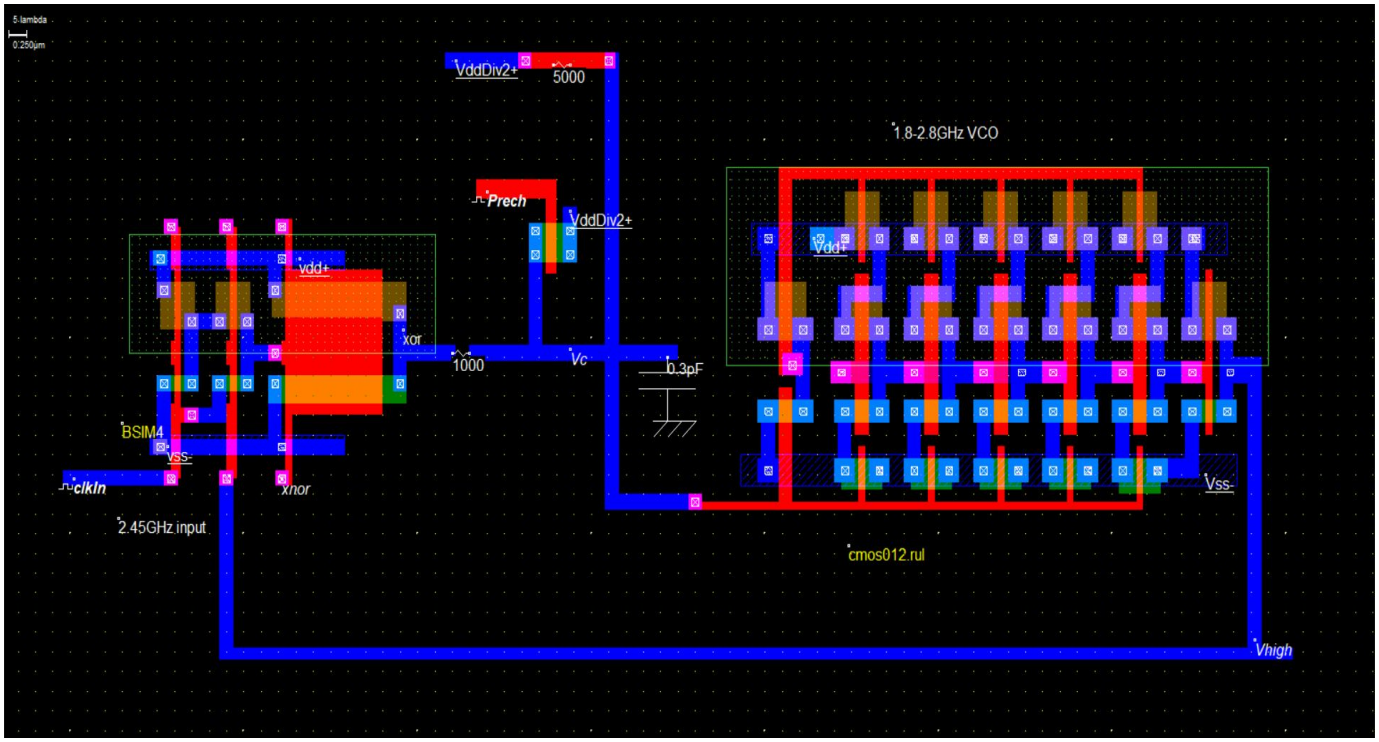


Fig 2. Phase Lock Loop

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### *B. Simulation and Result*

The simulation results are obtained by verifying the functionality of the full adders in digital schematics and for these Phase Lock Loop (PLL) the layouts are drawn in Microwind and waveform analysis.

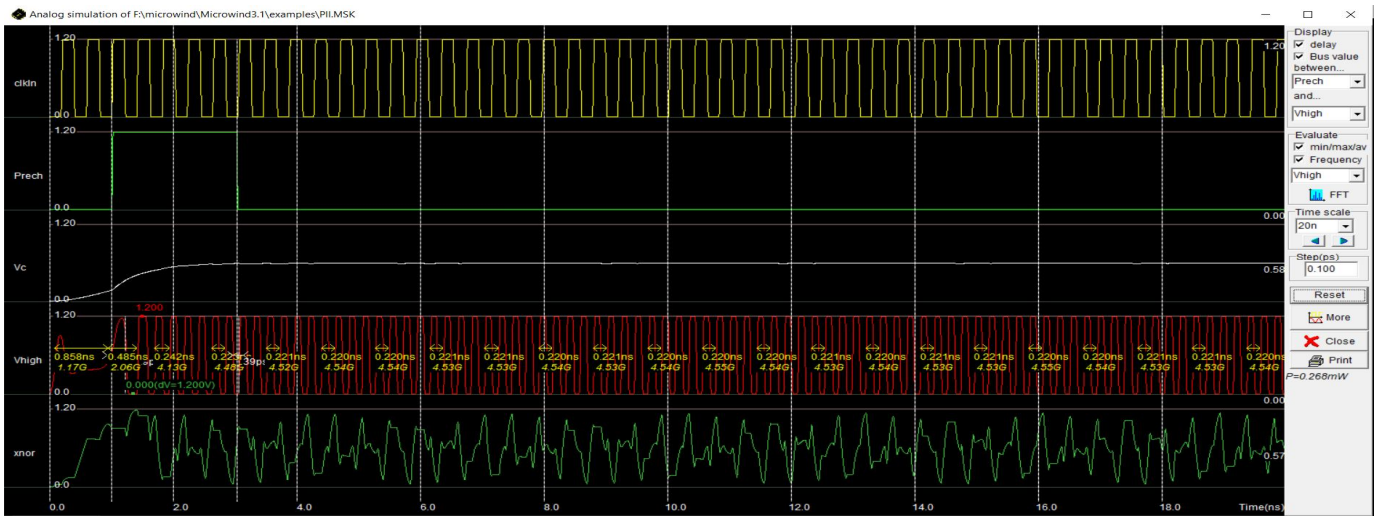


Fig 3. Voltage vs time

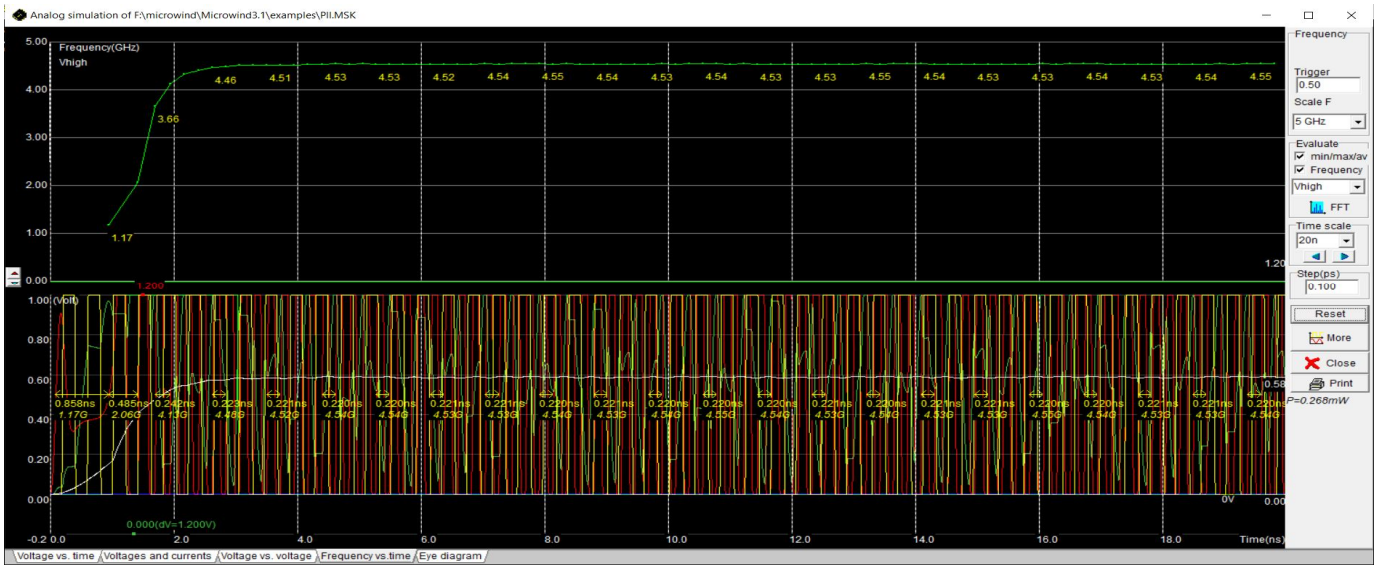


Fig 4. Frequency vs time

### *C. Comparison of Phase Lock Loop (PLL) in power*

| Sr. No. | Technology | Dynamic Power |
|---|---|---|
| 1 | 0.6µm | 6.416 mW |
| 2 | 0.12µm | 0.161 mW |
| 3 | 1.2µm | 6.260mW |
| 4 | 0.18µm | 0.403 mW |
| 5 | 0.25µm | 0.987mW |
| 6 | 32nm | 0.211 µW |
| 7 | 0.35µm | 1.834mW |
| 8 | 45nm | 2.074µW |
| 9 | 65nm | 30.554µW |
| 10 | 90nm | 0.268mW |

Table 3. Comparison of power using various technologies

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## IV. CONCLUSIONS

The CMOS Phase Lock Loop (PLL) in different logic styles are designed and simulated. From the simulation results it is observed that the Dynamic power is get varied by using different technologies. We can gain access to Circuit Simulation by pressing one single key. The electric extraction of the circuit is automatically performed and the analog simulator produces voltage and current curves immediately. As Phase Lock Loop (PLLs) are extensively used in communication application such as frequency synthesis for missile tracking, noise stability is the most important factor which can be analysed with the components of filter. The Software Microwind 3.1 used in this paper allows us to design and simulate an integrated circuit at physical description level.

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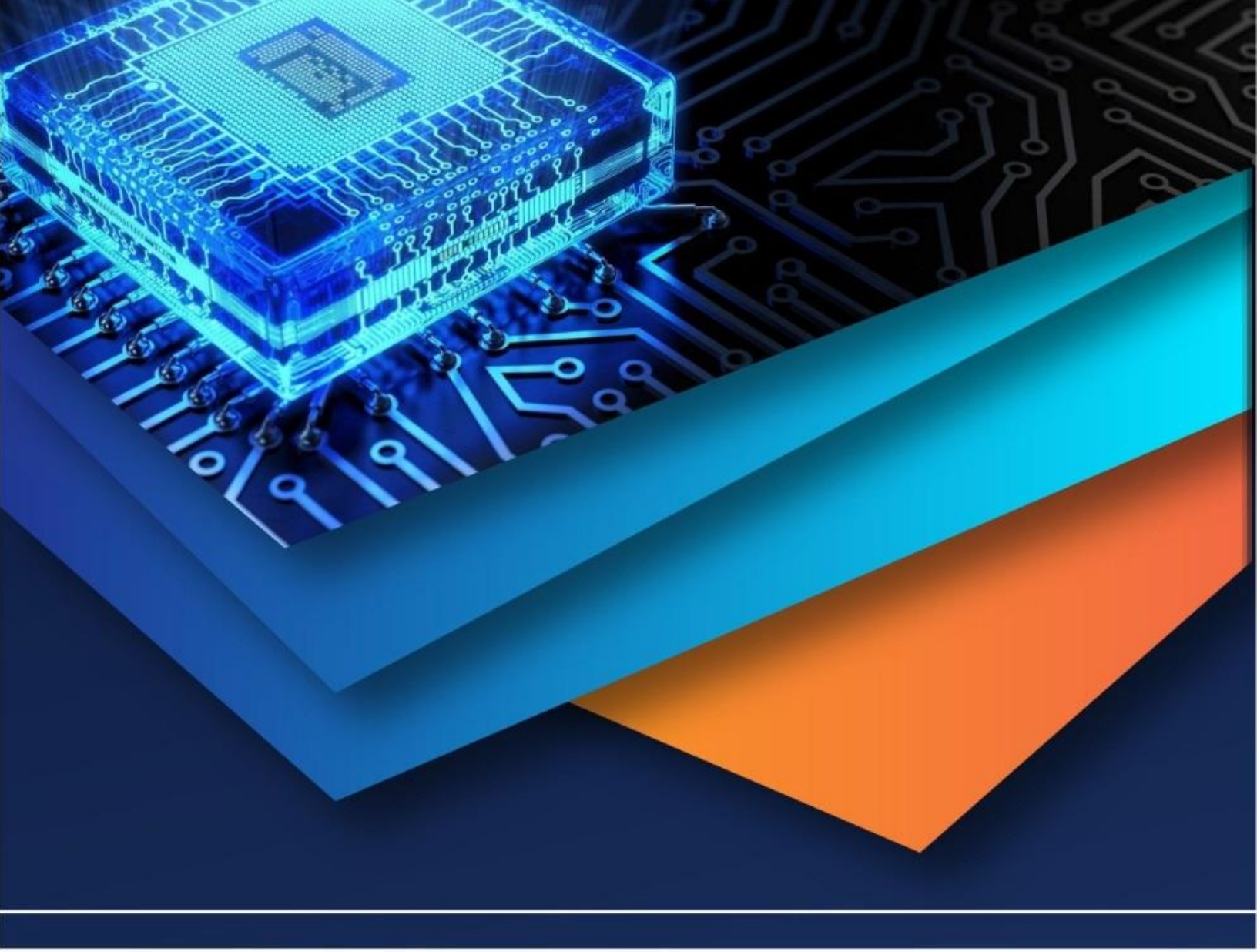

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