iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 4 **Issue:** II **Month of publication:** February 2016

DOI:

www.ijraset.com

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Volume 4 Issue II, February 2016
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Comparison of Driver-Interconnect-Load System with Doped and Neutral Graphene Nano-Ribbon in Nano Scale Regime

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Abstract— In the progressively growing VLSI area graphene nano-ribbon interconnects are widely used by scientists for interconnection purpose in VLSI/ULSI chips. In the work which has been presented in this paper graphene nano-ribbon (GNR) interconnects with multi layers have been used to find out the propagation delay of a Driver-Interconnect-Load system. Two forms of graphene nano-ribbon have been used for the study such as multi layer graphene nano-ribbon (MLGNR) with doping and MLGNR without doping (neutral). The study has been done beyond 16 nm and comparison has been made with the result of 16 nm technology node. TSPICE software has been used to obtain results.

Keywords— Driver-interconnect-load system, FinFET, Interconnect, Multi layer Graphene nano-ribbon, Propagation delay.

I. INTRODUCTION

In recent technology culture graphene nano-ribbon has been observed as a good candidate for making interconnects due to its properties [1][2][3][4] and large mean free path [5] and also can be used in many other applications [6]. Researchers have already started their work in the direction of graphene and its applications [7]. The performance of graphene interconnect can be enhanced by doping and study on this aspect has already been done by many researchers [8][9]. In this paper effect of doping on propagation delay of a driver-interconnect-load system (DIL) using graphene interconnect has been studied and compared with the performance of driver-interconnect-load system with neutral multi layer graphene nano-ribbon (MLGNR) interconnect beyond 16 nm and also the improvement in delay has been studied over the values of propagation delay obtained by Agnihotry in [16] at 16 nm.

The MLGNR is doped with AsF5 in order to increase its conductivity [10] and this is due to the fact that by doping density of carriers increases which makes mean free path more than that of neutral MLGNR, also spacing between the GNR layer increases due to doping [10][11]. By making the specular edges of GNR conductance can also be increased but the work in this paper is showing the study of propagation delay of a DIL system by only considering doped MLGNR interconnect.

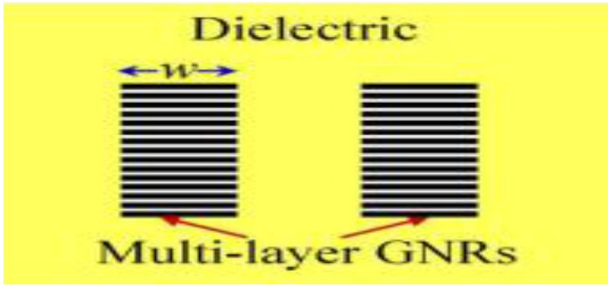

Fig. 1 Schematic view of neutral multilayer GNRs [9] .

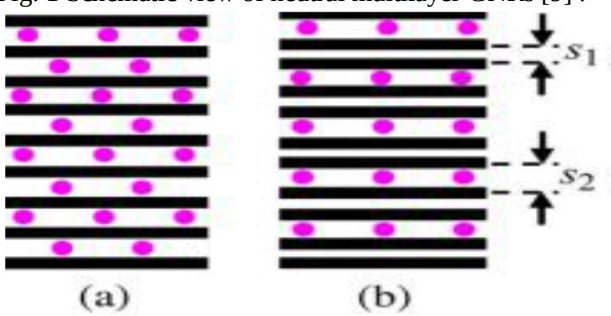

Fig. 2 Schematic view of two types of intercalated GNR [12].

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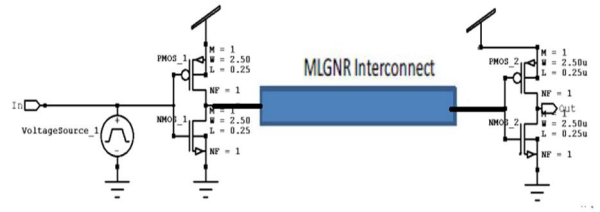
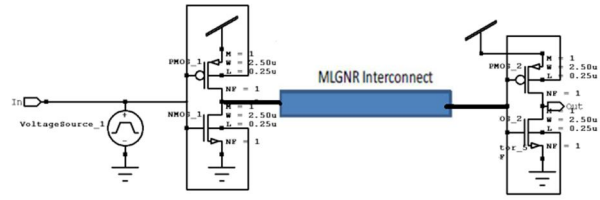
II. DRIVER-INTERCONNECT-LOAD (DIL) SYSTEM

This work has used four DIL systems which are shown in Figure 3. Figure 3 (a) is showing the DIL system which comprises of CMOS driver and load stages, (b), (c), and (d) DIL system carries short gate (SG), independent gate (IG) , and low power (LP) FinFET as driver and load stages.



(a)



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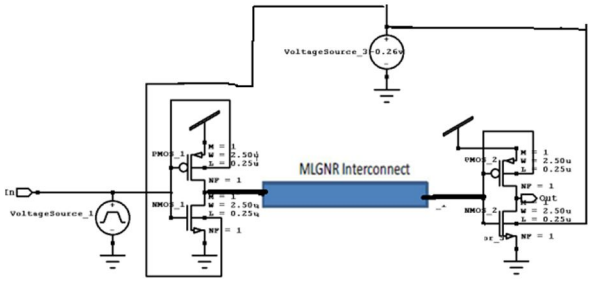

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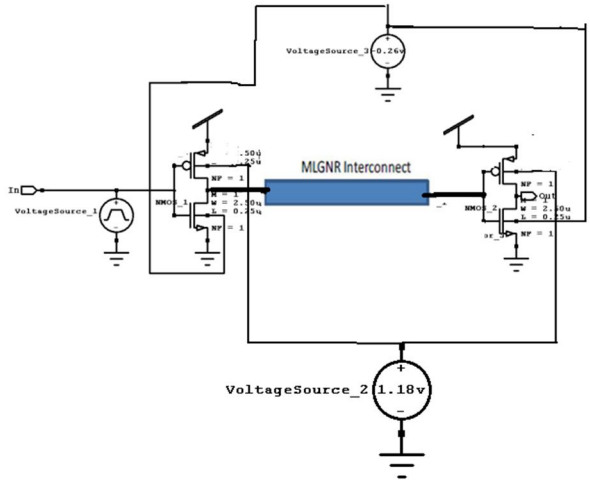

(d)

Fig. 3 Driver-interconnect-load system using (a) CMOS driver-load (b) SG FinFET driver-load (c) IG FinFET driver-load (d) LP FinFET driver-load.

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In SG FinFET the front and back gates of PMOS and NMOS transistors are connected with each other, in IG FinFET (n-type) front and back gates of PMOS transistor are short with each other and back gate of NMOS transistor is providing with another voltage source, and for LP FinFET both gates are provided with a different potentials in the case of PMOS and NMOS transistors [13].

Doped and neutral MLGNR has been used in this work, and for a doped MLGNR EF = 0.6eV, inter layer spacing 0.575 nm, and mean free path 1.03 μm [14][8] has been taken and for a neutral MLGNR EF = 0.1eV, inter layer spacing 0.34 nm, and mean free path 0.4 μm has been taken[15][8][18]. The study has been done in three operating regions such as super threshold region, near threshold region, and sub threshold region[16][19][20].

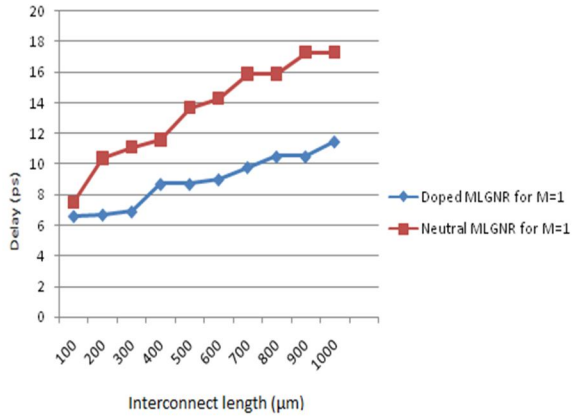
III. Result and Discussion

The set up which has been used for simulation is a DIL system shown in Figure 3. Performance characteristic of DIL system in terms of propagation delay has been studied with the variation of length (100μm, 200μm, _ _ _, 1000μm) and width (10nm, 20nm, _ _, 50nm) of MLGNR. The effect has also been noticed for different number of devices connected in parallel.

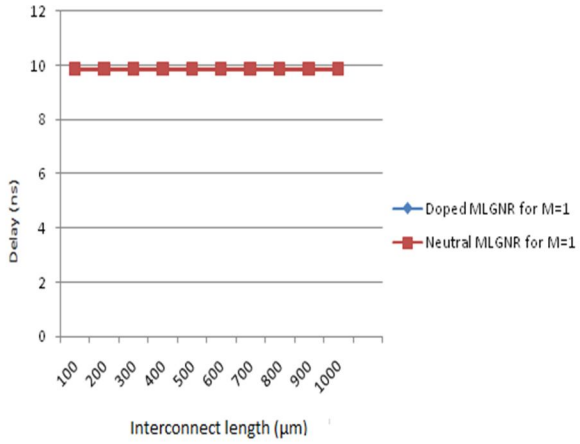
Figure 4 shows the delay variation with respect to the length of the interconnect. In [16] Agnihotry has shown the effect of propagation delay for doped and neutral MLGNR at 16 nm technology node and concluded that at 16 nm doped MLGNR has less delay as compared to neutral MLGNR.

During my research work it has been found that the DIL systems shown in Figure 3 practically performed similar in terms of propagation delay. Therefore graphs which are shown in this paper are similar for every DIL system which has been considered in the work.

Figure 5 shows delay variation with the variation of width and it has shown that delay will decrease with the variation of width. From the study it is also clear that delay will not change its value with length as well as with width in near threshold and sub threshold regions.



(a)



(b)

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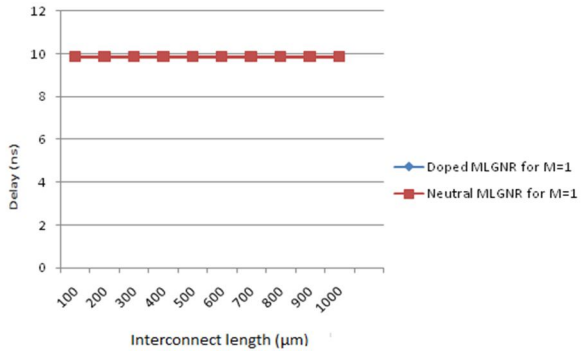

(c)

Fig. 4 Comparison of doped and neutral MLGNR in (a) super threshold region, (b) near threshold region, and (c) sub threshold region for GNR layer = 3.

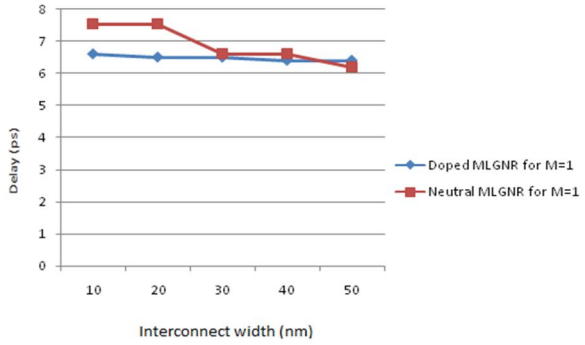

Fig.5 Delay variation with respect to width of doped and neutral MLGNR in super threshold region for GNR layer = 3.

TABLE 1.

PERCENTAGE IMPROVEMENT OF PROPAGATION DELAY OF DIL SYSTEM BEYOND 16 NM OVER 16 NM NODE FOR GNR LAYERS =3

% improvement of delay at GNR layer = 3						
	Doped MLGNR beyond 16 nm vs doped MLGNR at 16nm			Neutral MLGNR beyond 16 nm vs Neutral MLGNR at 16nm		
	M=1	M=3	M=6	M=1	M=3	M=6
CMOS DIL	99.53	99.62	99.67	99.57	99.51	99.57
SG FinFET DIL	99.38	99.62	99.64	99.47	99.51	99.57
IG FinFET DIL	99.77	99.73	99.69	99.75	99.65	99.60
LP FinFET DIL	99.78	99.74	99.74	99.76	99.66	99.66

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TABLE 2.

PERCENTAGE IMPROVEMENT OF PROPAGATION DELAY OF DIL SYSTEM BEYOND 16 NM OVER 16 NM NODE FOR GNR LAYERS =10

% improvement of delay at GNR layer = 10						
	Doped MLGNR beyond 16 nm vs doped MLGNR at 16nm			Neutral MLGNR beyond 16 nm vs Neutral MLGNR at 16nm		
	M=1	M=3	M=6	M=1	M=3	M=6
CMOS DIL	99.59	99.64	99.73	99.53	99.66	99.71
SG FinFET DIL	99.46	99.64	99.71	99.47	99.66	99.70
IG FinFET DIL	99.78	99.75	99.75	99.75	99.76	99.73
LP FinFET DIL	99.79	99.75	99.78	99.78	99.76	99.77

TABLE 3.

PERCENTAGE IMPROVEMENT OF PROPAGATION DELAY OF DIL SYSTEM BEYOND 16 NM OVER 16 NM NODE FOR GNR LAYERS = 20

% improvement of delay at GNR layer = 20						
	Doped MLGNR beyond 16 nm vs doped MLGNR at 16nm			Neutral MLGNR beyond 16 nm vs Neutral MLGNR at 16nm		
	M=1	M=3	M=6	M=1	M=3	M=6
CMOS DIL	99.59	99.65	99.61	99.58	99.66	99.57
SG FinFET DIL	99.46	99.65	99.61	99.52	99.66	99.57
IG FinFET DIL	99.78	99.76	99.76	99.76	99.76	99.74
LP FinFET DIL	99.79	99.76	99.78	99.80	99.76	99.75

IV. CONCLUSIONS

Study of driver-interconnect-load (DIL) system along with multi layer graphene nano-ribbon interconnect has been studied and it has been concluded that when doped multi layer graphene nano-ribbon (MLGNR) interconnect has been used in the driver-interconnect-load system the speed is much better than the DIL system using neutral multi layer graphene nano-ribbon interconnect. This paper also presents the improvement of propagation delay of doped and neutral MLGNR beyond 16 nm over at 16 nm

technology from which it has been concluded that the overall performance of the system under test shows better results when used beyond 16 nm.

Also the calculated value of propagation delay has not shown any change with respect to length and width in near threshold and sub threshold region. The numbers of graphene layers which have been used in the work are 3, 10, and 20. And the performance of DIL system for large number of layers is better than the DIL system using multi layer GNR of less number of layers [17].

Therefore from the overall results the main thing which can be concluded here is that for the VLSI/ULSI circuits doped multi layer graphene nano-ribbon interconnect is a very good candidate for interconection purpose.

V. ACKNOWLEDGMENT

This work has been performed within the research programe in Shobhit University, Meerut. I am very thankful to Prof.(Dr) R.P.Agarwal for being my research guide.

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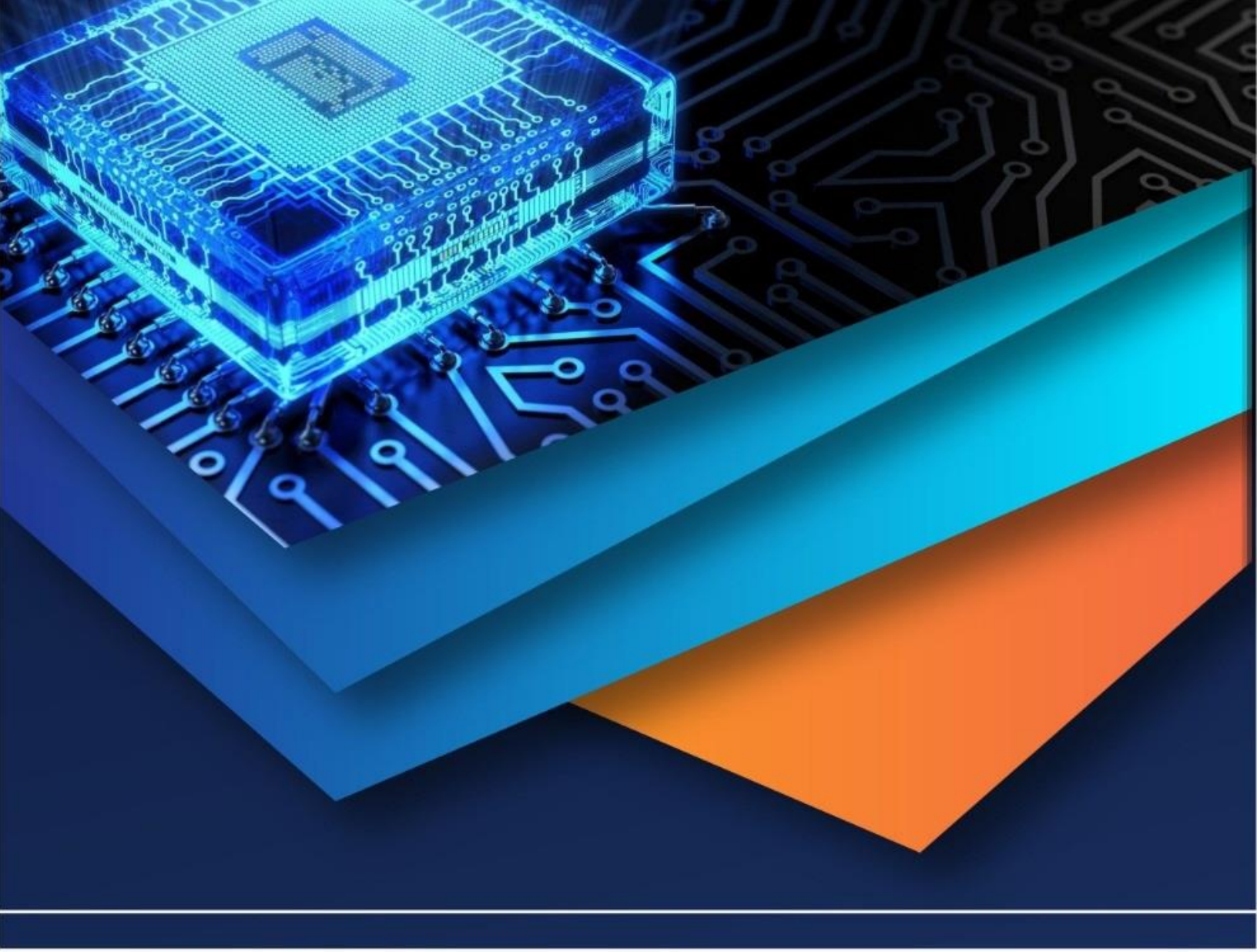

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