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Design and Implementation of FFT Processor for OFDMA System Using FPGA

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Abstract: Orthogonal Frequency Division Multiplexing(OFDM),is a frequency-division multiplexing(FDM) scheme utilized as a digital multi-carrier modulation(MCM) method.A large number of closely-spaced orthogonal sub-carriers are used to carry data. The data is divided into several parallel data streams or channels, one for each sub carrier. Each sub-carrier is modulated with conventional modulation scheme (such as QAM or PSK) at a low symbol rate, maintaining total data rates similar to conventional single-carrier modulation schemes in same bandwidth.In the receiver down link module of Orthogonal Frequency Division Multiple Access(OFDMA) system, there is needed an alterable points FFT Processor. Therefore, it is meaningful to design a FFT processor for the FFT processor which input data points could be alterable. In this paper, we select the 2D Fourier transform algorithm as the kernel algorithm, use VHDL language to present in detail a design of two-stage pipeline structure, use Xilinx and ModelSim SE for the simulation, and verify on the spartan3E500 or Vertex-6 chip FPGA.

Keywords: OFDMA, FFT, MCM, FPGA

I. INTRODUCTION

In modern communication systems Orthogonal Frequency Division Multiple (OFDM) plays a crucial role, in next generation wireless communication systems such as WiMAX and 3G-LTE standard. The OFDMA PHY is based on OFDMA modulation, which comprises of OFDM modulation as well as subcarrier allocation. Therefore it is significant to focus more attention on wireless communication technology.

The FFT block plays very crucial role while receiving multiple carriers frequencies and thus needs variable point FFT processor algorithms such as Radix-2, Decimation-In-Time FFT and 2D FFT have been chosen. In order to ensure precision, the floating-point system is used in design. The proposed architecture of FFT processor enhances the system performance in terms area and computational complexity.

A. Fourier Transform

Discrete Fourier Transform(DFT)is widely used in communications,Radar,Antenna arrays,GPS navigation,Voice processing,Image processing and sonar systems.In different areas of signal processing also has an important position.

The Discrete Fourier Transform (DFT) of the N-point input X(k) is defined as follows:

$$X(k)=\sum_{n=0}^{N-1}x(n)W_N^{nk} \quad k=0,1,\ldots N-1$$

$$W_N^{nk}=e^{-j2\pi/N}$$

Where N is transform length, is twiddle factor

An algorithm for the machine calculation of complex fourier series in 1965 is an optimized fast algorithm and increase the computational efficiency of the DFT. The algorithm Is divided in to time based(DIT) and based on frequency (DIF)Fast fourier transform.Both the DIF and the DIT FFT reorder the data from normal to bit reversed order(or the converse).The basic idea of these algorithms are that the N point FFT is divided in to smaller and smaller parts until only two points FFT(Radix-2).

Long FFTs are quite often used for frequency analysis and communications applications.These long word lengths require more

memory architecture because long word lengths require more memory bandwidth for matrix transpositions.The architecture is implemented using two shorter length FFTs(lengths N1 and N2)to calculate an FFT of length N=N1XN2.

The two-dimensional (2D) FFT of $N = N_1 \times N_2$ is defined as follows:

$$X[k_1 N_2 + k_2] = \sum_{n_1=0}^{N_1-1} [e^{-j\frac{2\pi n_1 k_2}{N}} (\sum_{n_2=0}^{N_2-1} x[n_2 N_1 + n_1] e^{-j\frac{2\pi n_2 k_2}{N_2}})] e^{-j\frac{2\pi n_2 k_1}{N_1}}$$

where $0 \le k_1 \le N_1 - 1$; $0 \le k_2 \le N_2 - 1$.

II. ARCHITECTURE DESIGN

For the variable point FFT processing, if cascade method and pipeline structure was used" ping-pong" memory architecture adopted in the design, each level need a lot of memory, so the system becomes too large. Therefore,I n this paper used 2D FFT algorithm to design the FFT processor, not only improved the system level of the parallelism, but also reduced the demand for memory systems.

A. The Overall design of the FFT Processor

The FFT module is the core part in the OFDMA system, IEEE Std802.16-2005 defined clearly: the core module of OFDMA physical layer is the FFT module,which can be used in the FFT points are 2048 points(back compatible with IEEE Std802.16-2004),1024 points,512 points and 128 points. The design about variable point FFT processor is just based on FFT module in OFDMA system application.

According to the idea of two-dimensional Fourier algorithm,i.e N=128,N1=2,N2=64,from 128=2*64.We find that when achieve 128-point FFT,Firstly the data is arranged in 64 lines and 2 rows,Secondly the input data will transform the 64 points FFT,then the result multiplies twiddle factor,Thirdly,let the result do 2 points FFT. Similarly, calculation of the 512-point FFT firstly do the 64 points FFT,then transform further 8 points FFT;The same way to calculate the 1024 and 2048 points FFT.In Fig:1. We see that the architecture of the over all design described by VHDL language and block diagram of the over all design of the FFT processor as shown in Fig:2.

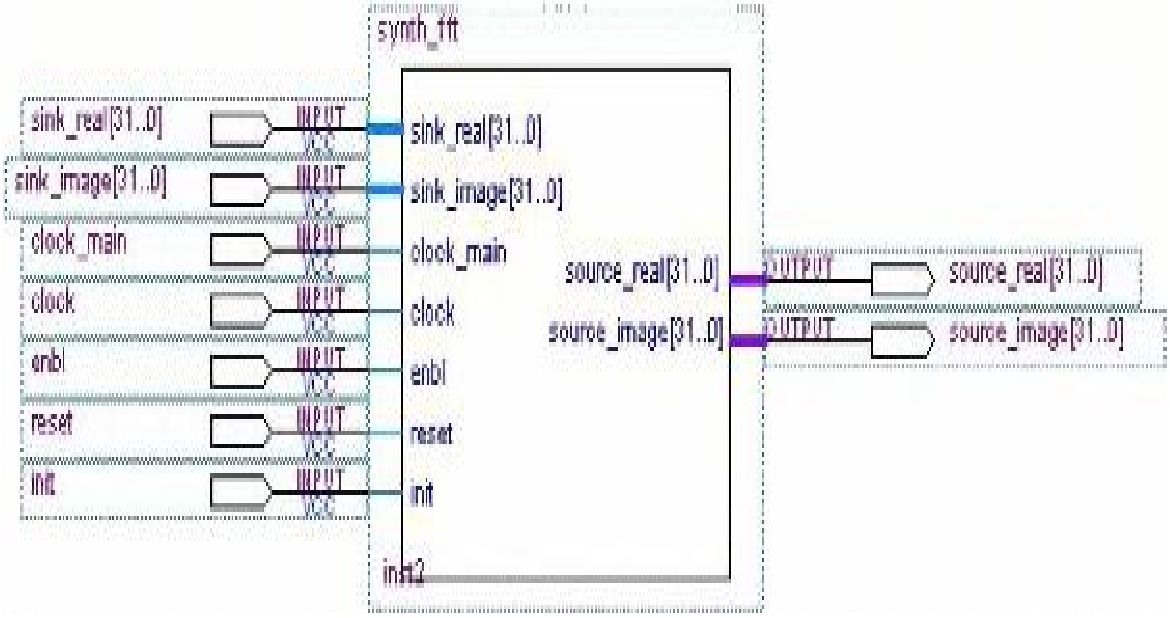

Fig:1.The architecture of the overall design

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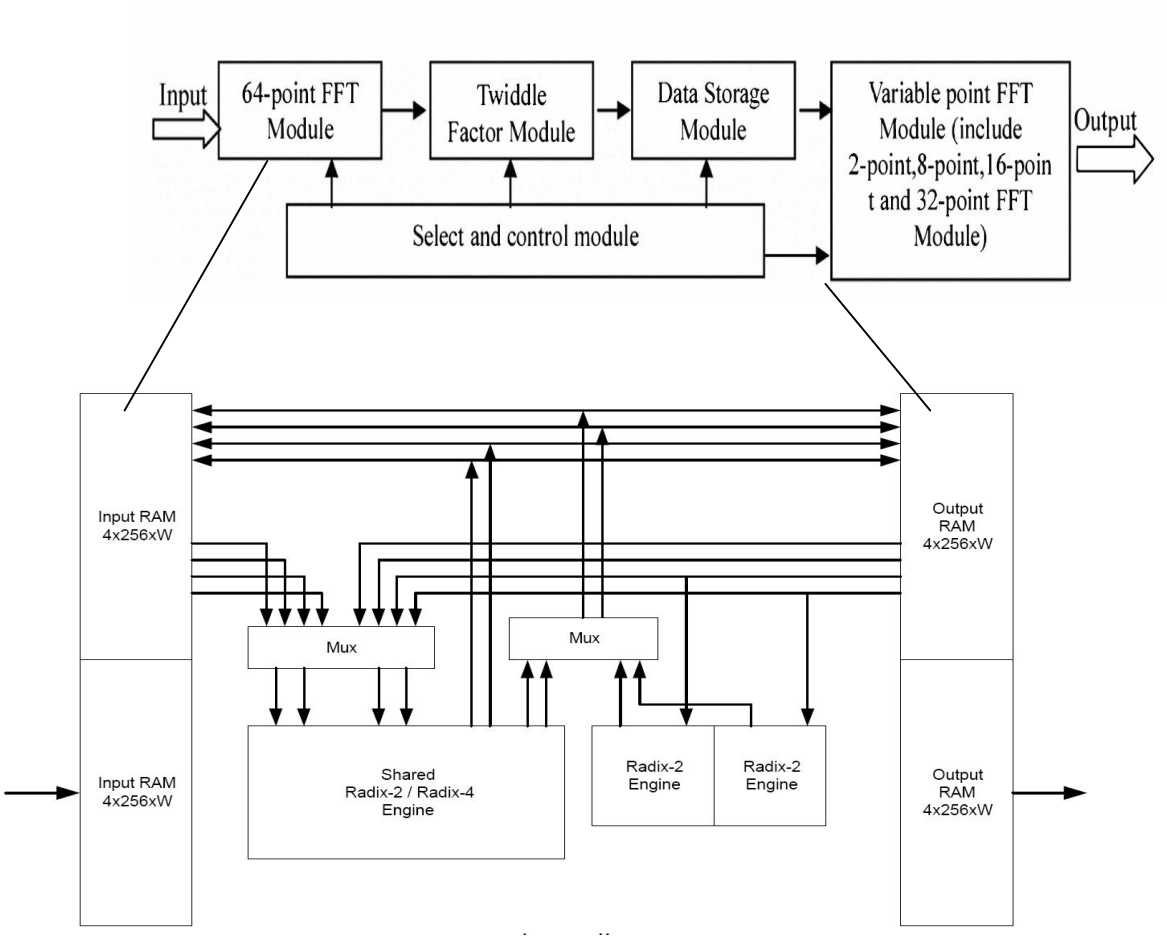


Fig:2.Block digram of the over all design of FFT processor

B. 64-Point FFT module

This module is the most frequently used in the design. Four kinds of input data length all must first pass through the 64 points FFT module. Block diagram of this part is shown in Fig:3.

The same idea in the module based on 2D Fourier transform algorithm is composed of two 8-point FFT modules. So 8-point FFT module is the kernel in this part, its performance affects the whole design. The 8-point FFT processor architecture consists of a single radix-2 butterfly (which is referred as the butterfly processing element),a dual-port FIFO RAM, a co-efficient ROM, a controller and an address generation unit. For ex: The input data is [1 -1 0.5 -3 2 -2.5 0 4] and the result of 8-point FFT module and the result of the 8-point FFT module match that from Matlab. And the result error is with in the allowable range. Therefore, it's acceptable to adopt the 8-oint FFT processor as the kernel module of the 64-point FFT module.

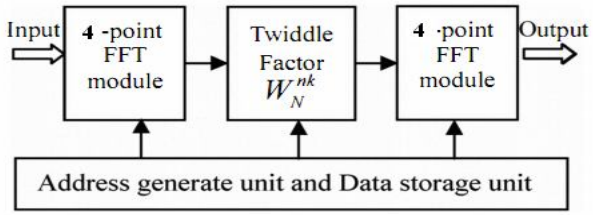


Fig:3.Pipeline structure of the 64-point FFT processor

C. Select and control module

This part is the kernel to complete the alterable data length In the design.It is based on the input data points to select the results stored In the middle data memory,and then choose the way to next flow.A three bits signal 'mode' is chosen as the mode signal(N_select(2..0).When mode=000, means to choose 8 points FFT module,to complete the 512-point FFT;when mode -100,means to choose 128-FFT module,to complete the 8192-point FFT;Equally:when the mode=110,means to completed 32768 point FFT;when mode=111,means to complete the 65536 point FFT. The N-point transform selection values are given in the following table:

N_select(2..0)	000	001	010	011	100	101	110	111
Size of Transform	8	16	32	64	128	256	512	1024

Tab:1. N-point table

III. SIMULATION AND IMPLEMENTATION

The input data length of our proposed FFT processor is a parameter which can be decided by itself at the range of 128,512,1024 and 2048 points.Take 1024 points FFT as an example.At first,the 1024 points FFT is coded by MATLAB language.After the chosen FFT algorithm is valid,the architecture of the processor was modeled in VHDL language and functionally verified using Xilinx software and timing simulation using using modelsim SE software.When verify the timing simulation,a testbench file included the TEXTIO package was written to read input data and write FFT result,parts of the procedure as follows

File vector_file: text open read_mode is "F:\test_f_FFT\input.txt";

File vector_file: text open write_mode is "F:\test_f_FFT\result.txt";

Figure 4 is the FFT waveform which the input points changing to 1024-point mode,it shows that after a latency of 21.175us the FFT results start to output.The results of the simulation were seen to match the theoretical calculation of Matlab,result error with in the allowable range,therefore,the design and implementation is right and meet the standard IEEE802.16E FFT requirements.

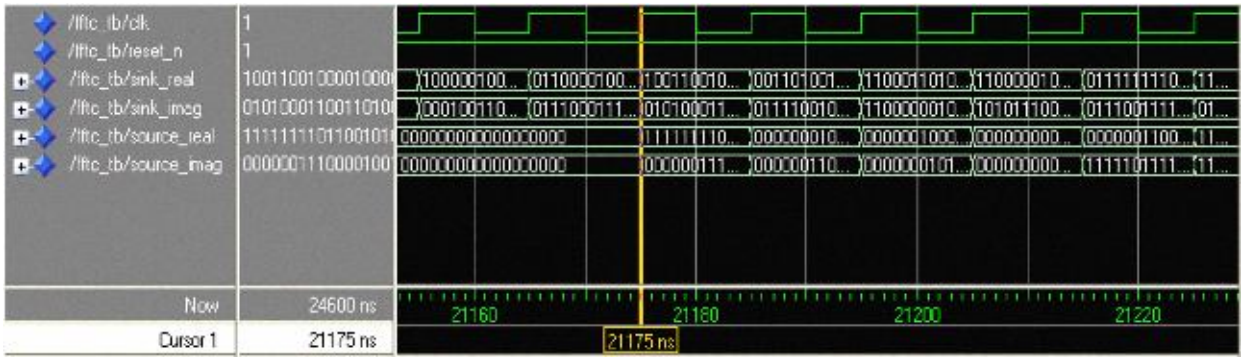


Fig:4.Simulated waveform of the 1024-point FFT

IV. CONCLUSION

In this paper,a variable point FFT processor was designed using FPGA and was applicable to OFDMA system successfully. With the so much development of techniques of digital transmission of data as of current FPGAs possibility to do systems of digital transmission integrated in a single chip. To do use of those modern technologies the complete structure it was developed for the transmitter and for the receiver OFDM, that use FFT (I) to do the modulation. Several forms were analyzed of implementing that modem OFDM in a FPGA, and chosen the most efficient and versatile.

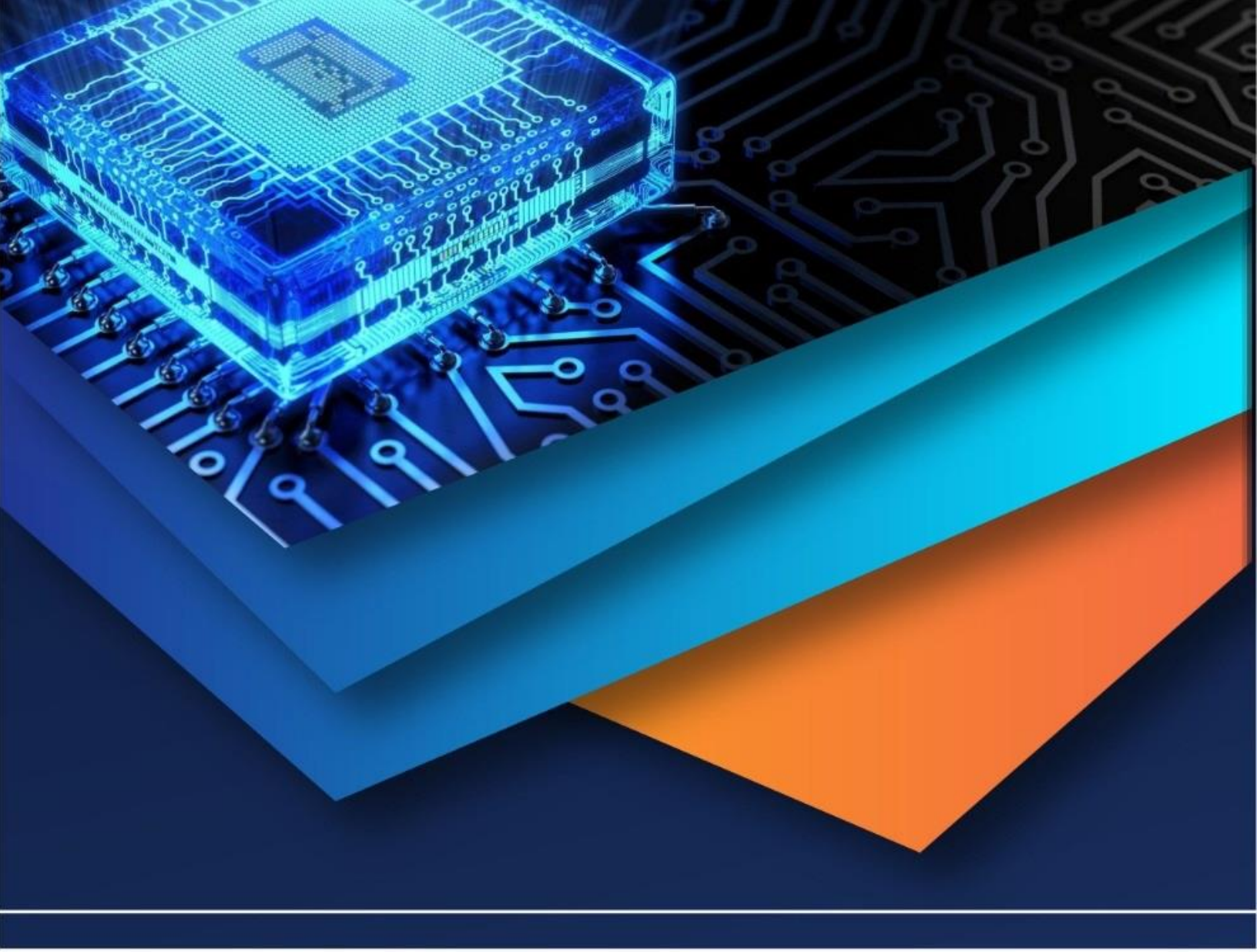
As contribution, the present work, supplies a code in complete and functional VHDL for a modem OFDM with 31 subcarrier, using a 64-points FFT, radix-4 with CORDIC, at a rate of 12.5 Mbps.For that, it was developed and analyzed several functional blocks of a modem and the chip occupation was compared in hardware of the several parts that compose it.

In that analysis, one of the parts that more highlight is the controller that organizes and manipulates the data in order to perform the

modulation in a correct way. This system reveals extremely complex so that to improve better performance (work in a larger frequency) it is necessary to re-analyze all the design.

REFERENCES

[1] Bahai, A., and B. Saltzberg. Multicarrier Digital Communications: Theory and Applications of OFDM. New York: Kluwer Academic/Plenum Publishers, 1999
[2] Van Nee, R.,& R.Prasad.OFDM Wireless Multimedia Communications. Boston: Artech House, 2000
[3] Couch II, L. W. Digital and Analog Communication Systems. New Jersey: Prentice-Hall, 1997
[4] Keller, T., and L. Hanzo. "Adaptive Multicarrier Modulation: A Convenient Framework for Time-Frequency Processing in Wireless Communications." Proceedings of the IEEE 88.5 (2000) 609 - 639
[5] OFDM Wireless Technology, Eric Lawrey and Craig Blackburn. 2000. James Cook University. < http://www.eng.jcu.edu.au/eric/thesis/Thesis.htm >.
[6] IEEE Std 802.16e-2005 and IEEE Std 802.16-2004/Cor1-2005
[7] Zhang Zhu-jun,"Optimum Design of FFT Processor with Cascade Structure Based on FPGA",J.Nanjng University of Science and Technology,2009 in press.



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