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International Journal For Research in  
Applied Science and Engineering Technology



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# **INTERNATIONAL JOURNAL FOR RESEARCH**

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

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**Volume: 4      Issue: III      Month of publication: March 2016**

**DOI:**

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# A Power Equalizer for Shaded PV Module

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**Abstract:** This paper deals with a photovoltaic (PV)-module embedded power-electronics topology derived from a battery equalizer. The photovoltaic equalizer is a promising response to the problems of partial shading in photovoltaic modules. Equipped with a network of transistors, this system can connect itself to the unshaded cells of the photovoltaic module, gather their excess current, and share it with the shaded cells. The topology does so by equalizing the overall energy of the PV module through the use of buck-boost converter. The parameters and operating points of individual solar cells change depending on the solar cell temperature and the level of solar irradiance. The proposed model can provide realistic behaviour of partially shaded photovoltaic module required in simulation tools used in the development of a microinverter. The model was confirmed by measurements performed on the tested photovoltaic module. All simulations are validated through measurements.

**Keywords—** Partially shaded photovoltaic module, solar cell, micro-controller 8051, Analog-to-Digital Converter, Buck-Boost-type power converter, LDR

## I. INTRODUCTION

Proper models of partially shaded photovoltaic (PV) modules are indispensable for proper evaluation of electricity production in PV systems that are shaded by vegetation or neighbouring objects. It is a well-documented fact that partial shading of a photovoltaic array reduces its output power capability. Photovoltaic (PV) installations are a familiar reference in this landscape, ranging from small (less than 5 kW) residential plants to larger (thousands of kilowatts) grid-connected PV fields. They can also compose hybrid power systems, along with other renewable energy sources [1], [2]. PV systems are roughly composed of two parts: the PV modules and their power electronics (PE) applications. While dispersed between these two parts, all PV research themes seek to improve productivity, power, efficiency, safety, and reliability. The biggest reliability issues of PV systems is the difference between its expected and actual power outputs.

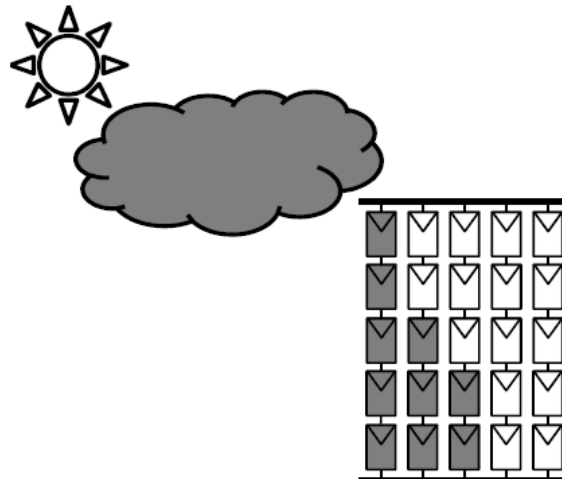


Fig.1 PV system under partially shaded conditions caused by passing cloud

## II. BASIC BLOCK DIAGRAM OF PV CELL

The main foundation of any solar panel starts from the forming of a single solar cell, which are taken in appropriate quantity and are connected in series-parallel fashion to form the solar panel of rated values of voltage and current (Solanki, 2014). Before going into an in-depth analysis of the solar panel and the actual MPPT structure and its operation, it is very much important to know about the internal components of the solar cell, in order to obtain a basic understanding for the working of MPPT algorithm in the PIC controller in the proposed system. The basic definition is given as “Solar cell is a basic fundamental element of a solar panel which performs the function of converting solar energy into useful electrical energy at standard values of solar insolation and temperature” (Walker, 2006).

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The general block diagram of a solar PV cell includes the following things (Solanki, 2014):

- Current Source.
- Shunt Resistance.
- Series Resistance.
- A Diode.

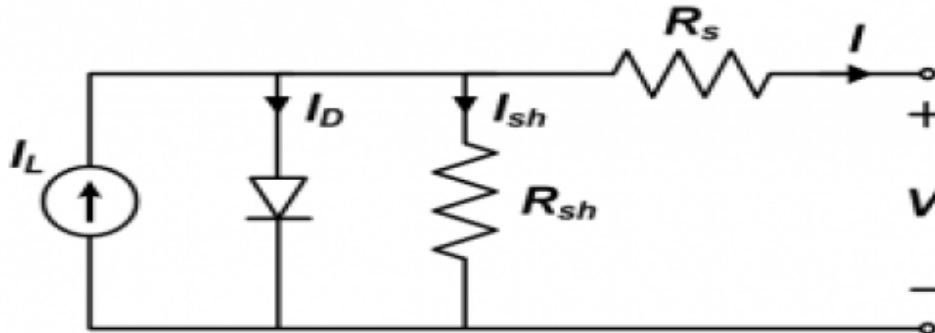


Fig.2 Equivalent diagram of solar PV cell

Fig-1: Equivalent diagram of solar PV cell. The above equivalent circuit diagram of solar PV cell signifies that solar cell is a current generating device with a diode connected in anti-parallel direction in order to resist the back-flowing currents and provides protection to the solar cell. Whereas the series resistance provides evidence of contact resistance i.e. between metal contacts and Silicon material, and shunt resistance provides the resistance due to the power loss caused due to manufacturing defects in a PV cell (Harjai, Bhardwaj, & Sandhibirgha, 2008). The voltage that we get across the PV cell is known as the PV cell voltage and that will increase with the increase of cells connected in series, whereas the current can be maximized by connecting PV cells in parallel fashion. By this series-parallel combination we can obtain a solar panel on which we track the maximum power point and utilize its energy for power generation and other purposes (J.Surya Kumari, 2012). The basic building block of any solar panel depends on the series-parallel configuration of the individual solar cells which decides its current, voltage, and power ratings.

### III. PV MISMATCH AND CURRENT RESEARCH

PV mismatch is a wide and often complex area of study. This section details the terminology and phenomena addressed in this paper.

#### A. PV Module

A PV module can be considered a voltage-controlled current source connected in parallel with a diode [10]. The output current depends on the available sunlight and the temperature of the module. Its output characteristics may be described by a graph called current–voltage ( $I-V$ ) curve, shown in Fig. 1.

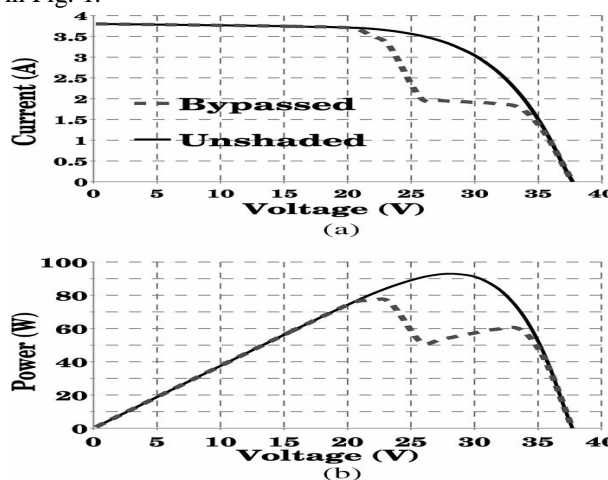


Fig.3 current–voltage ( $I-V$ ) curve

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The unit used to measure the available power which can be drawn from the sun is called irradiance and expressed in W/m. maximize the power output of the PV plant, either its current or its voltage is controlled to stay as long and as close as possible to the maximum power point (MPP) [9].

### B. Shadows in PV Systems

A shadow is a random phenomenon that filters the light that shines over a PV module. It can be considered as 2-D, having a length and a depth. Its length is equivalent to the number of cell groups covered by the shadow, while its depth, also called shading factor (SF), describes how much power carried by light, or irradiance, has been filtered. An SF of zero means that there is no shadow, while an SF of one means that the totality of the irradiance is filtered. Both of these dimensions are random phenomena. They depend on the environmental conditions, the shape of the objects surrounding the PV module, and the seasons of the year. The impact of a shadow with an SF of 0.5 and a length of 1 (one shaded cell group) is illustrated by its  $I-V$  curves in Fig. 1. In Fig. 1, at the operation point 35 V and 1.6 A, all cell groups are producing but their current is limited by those shaded. At the operation point 20 V and 3.8 A, only the unshaded cells are producing. The shaded ones are in reverse bias, protected from destruction by bypass diodes. Either way, part of the power is post due to the shaded conditions [8].

To avoid this situation, several authors have proposed dedicated power electronics systems, which are embedded in the PV module.

### C. PV Embedded System

Every PV embedded system (PES) seeks to make the current and voltage of the PV cells different while keeping them connected together. By doing so, they weaken the impact of the shadow over the entire module, even though it still has a Fig. 4. PV equalizer topology. strong local impact over the PV cells. This is called the power independence principle [8]. There are two families of PES: series and parallel. The *series PES* manipulate the operating point of each cell group separately. They are called distributed maximum power tracking systems in the current literature [2]. The *parallel PES* balance the current production by connecting the cell groups to one or several inductors, thus erasing local power points. Return energy architecture [3], [4], generation control circuit [5], or PV equalizer [8] are its three main examples in the current literature. The advantages and disadvantages of each approach have already been studied in previous work [8]. The PV equalizer has been shown as among the most efficient parallel PESs, depending on the shadow [7].

### D. Proposed PE Topology

The topology proposed in this paper is shown in Fig. 4. Even though it is similar to the battery equalizer in [11], their functionalities, sizing, and limits are different. The step-up dc/dc converter and its MPPT control technique are modeled in this part by a current source. The topology and its implementation challenges are analyzed in further details in Section V. The proposed equalizer has eight transistors ( $K2-K9$ ), ten diodes ( $D1-D10$ ), four capacitors ( $C1-CIV$ ), and an inductor  $L$ . The PV module is represented by four cell groups ( $PVI-PVIV$ ). The transistors are voltage bidirectional but current unidirectional due to the diodes, which impose one single current flow. Its single inductor can be charged by the available voltage of any unshaded cell group(s). The stored energy is then used to support the shaded cell group(s) by connecting the inductor in parallel to them, thus creating an alternative path to the excess MPPT current. In normal operating conditions, the switching pattern imposes rapid variations in voltage and current to the cells. To filter these, each cell group has a capacitor connected to it.

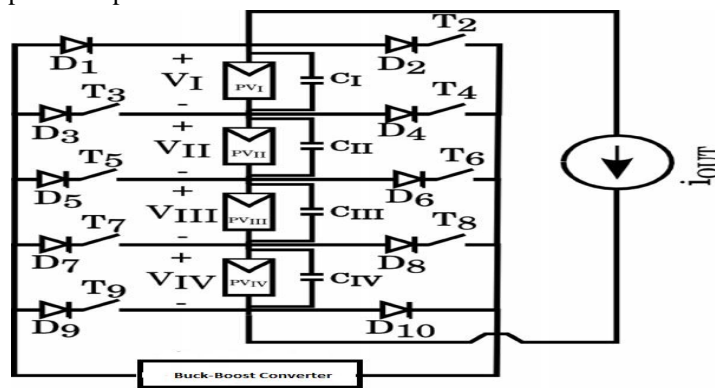


Fig.4 Diagram of Proposed PE Topology



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### E. Equalizer System

The PV equalizer is a parallel PES inspired from its equivalent battery equalizer [5]. Its topology is shown in Fig. 5. The diodes (D) impose the current flow, allowing it to be controlled by the transistors (T). The Buck-Boost Converter works as an energy buffer, instantaneously stocking the surplus current from the unshaded cells. The capacitors (C) are used to filter voltage fluctuations on the cell groups (PVI to PVIV). The dc/dc converter connected in series with the equalizer imposes the overall current, represented by  $I_{OUT}$ . Its value is constantly changing as to seek the optimum power point of the PV module. To avoid any interferences, the equalizer switches must work at a frequency five to ten times higher than its dc/dc converter counterparts.

Due to its concept, the architecture of this system is scalable. It can be used to design applications for many different voltage levels ranging from PV cells to entire plants. The advantages of the equalizer and its improvements in comparison with other state-of-the-art applications are studied in detail in [8]. It is not the objective of this paper to restate what was previously explained. However, some details of the principles of operation of this systems are described below to justify the contributions of this study.

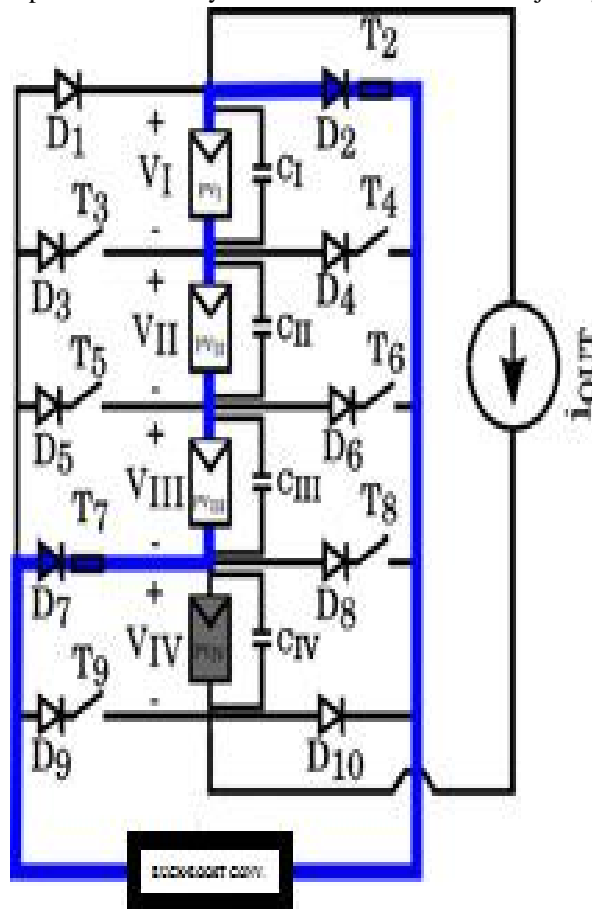


Fig.5 operation of PE topology under shaded condition of 4<sup>th</sup> cell

### IV. BRIEF DETAILS ABOUT MICRO-CONTROLLER 8051 CONTROLLER

There are four input output ports available P0, P1, P2, P3. Each port is 8 bit wide and has special function register P0, P1, P2, P3 which are bit addressable means each bit can be set or reset by the Bit instructions (SETB for high, CLR for low) independently. The data at any port which is transmitting or receiving is in these registers. The port 0 can perform dual works. It is also used as Lower order address bus (A0 to A7) multiplexed with 8 bit data bus P0.0 to P0.7 is AD0 to AD7

respectively the address bus and data bus is demultiplex by the ALE signal and latch which is further discussed in details.

Port 2 can be used as I/O port as well as higher order address bus A8 to A15. Port 3 also have dual functions it can be worked as I/O as well as each pin of P3 has specific function.

P3.0 – RXD – /Serial I / P for Asynchronous communication

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Serial O / P for synchronous communication.

P3.1 – TXD – Serial data transmit.

P3.2 – INT0 – External Interrupt 0.

P3.3 – INT1 – External Interrupt 1.

P3.4 – T0 – Clock input for counter 0.

P3.5 – T1 – Clock input for counter 1.

P3.6 – WR – Signal for writing to external memory.

P3.7 – RD – Signal for reading from external memory.

When external memory is interfaced with 8051 then P0 and P2 can't be worked as I/O port they works as address bus and data bus, otherwise they can be accessed as I/O ports

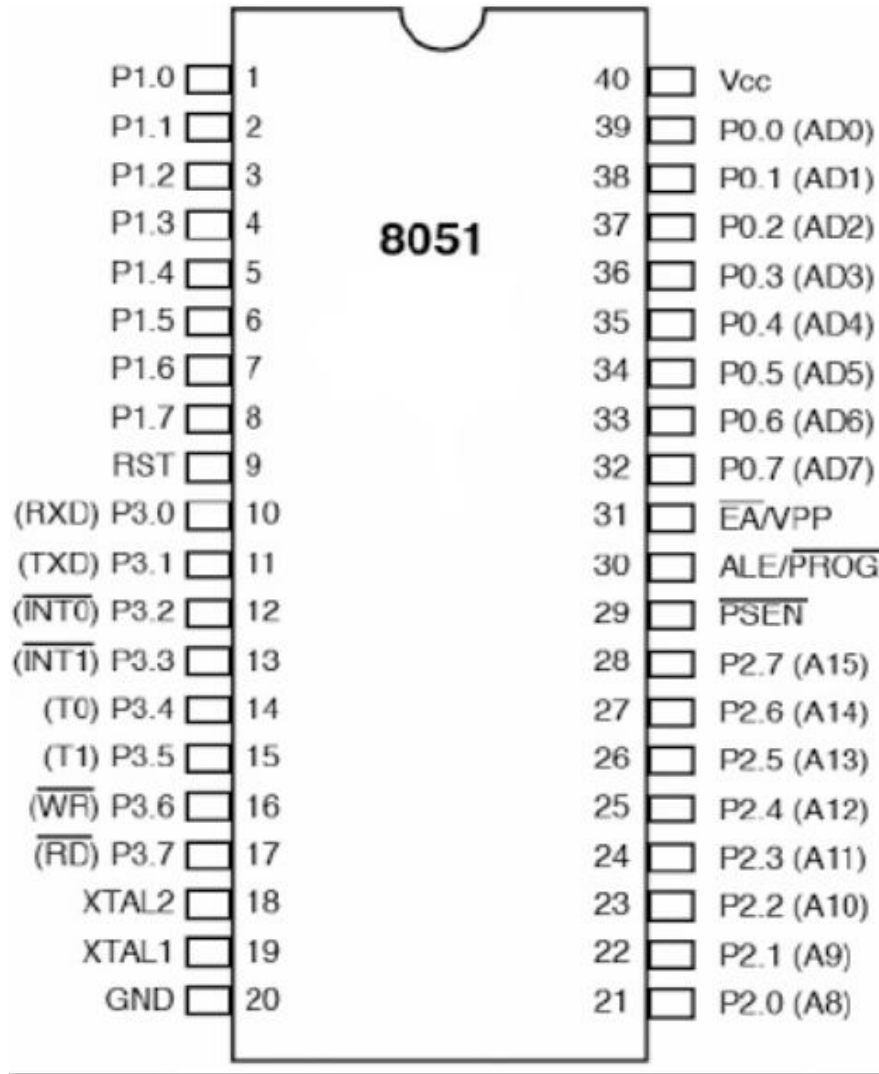


Fig.6 Pin Diagram of Micro-controller 8051

### V. PCB DESIGNING OF PROPOSED PE TOPOLOGY

Before performing the hardware implementation of proposed PE topology

on a practical basis, there is a need to design the whole hardware structure on PCB designing software which is provided in the diagram given below:

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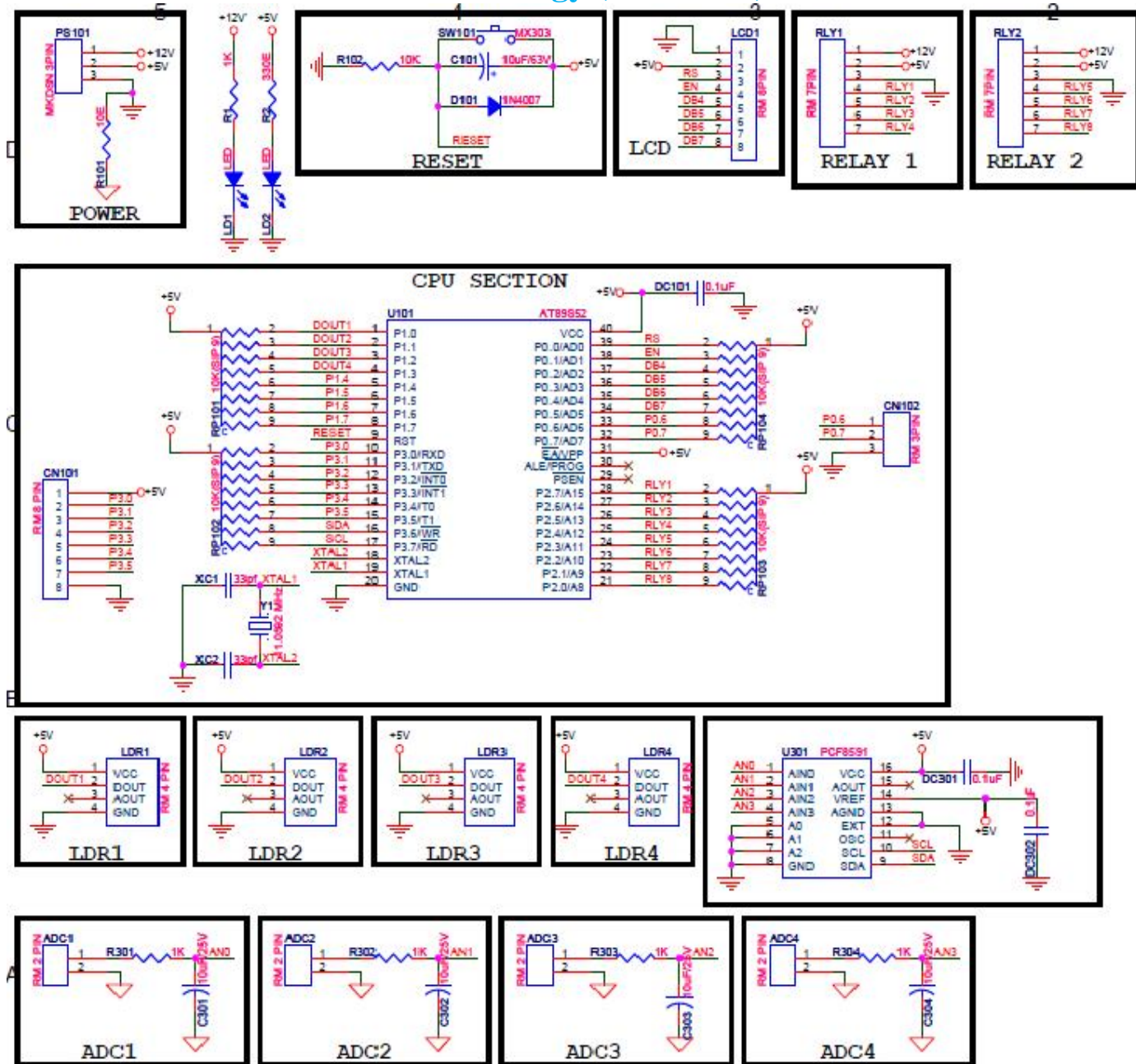


Fig.7 Design of Proposed PE Topology On PCB Designing Software

In this diagram, power circuit and reset circuit is used for on and off purpose respectively. There are four ADC circuit are used for converting analog quantity i.e irradiance to digital quantity because microcontroller works on digital quantity. There are two relay circuits which are used as switches. There are four LDRs are used for sensing the irradiance on PV Module. Here microcontroller 8051 are used for giving the signal to relay circuits.

### VI. RESULT AND DISCUSSION

The result of proposed power equalizer under partially shaded condition of PV module is compared with the simple series connected PV module under partially shaded condition and it is found that with the use of power equalizer for partially shaded PV module gives much greater power compared to simple series connected PV module under partially shaded condition

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I. Table Showing The Comparison With And Without PE Topology

Sr no	Conditions	With topology (power) watt	Without topology (power) watt
1	1 cell shaded	1.0179	0
2	2 cell shaded	0.6786	0
3	3 cell shaded	0.3393	0

### VII. CONCLUSION

A PV equalizer system is an extremely flexible power electronics structure embedded on a PV module. Its main objective is to mitigate the effects of partial shading by sharing the excess current of the unshaded cells with the shaded ones. An embedded PE structure designed for compensating the effect of partial shading in PV modules has been studied in this paper. Its topology is based on a battery equalizer, giving it its name: PV equalizer. The proposed equalizer redistributes the produced energy between the unshaded and the shaded PV cell through the use of one single inductor. The result of proposed power equalizer under partially shaded condition of PV module is compared with the simple series connected PV module under partially shaded condition and it is found that with the use of power equalizer for partially shaded PV module gives much greater power compared to simple series connected PV module under partially shaded condition.

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