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Interleaved Bridgeless Boost Converter Using Predictive Control with PFC Technique

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Abstract: ***We deal with a three-level quasi-two-stage single-phase power factor correction (PFC) converter that has flexible output voltage and improved conversion efficiency. The proposed PFC converter features sinusoidal input current, three level output characteristic, and a wide range of output dc voltages. It will be very suitable for high-power applications where the output voltage can be either lower or higher than the peak ac input voltage, e.g., plug-in hybrid electric vehicle charging systems. The involved dc/dc buck conversion stage may only need to process partial input power rather than full scale of the input power, and therefore the system overall efficiency can be much improved. The Three-Level Quasi-Two-Stage Single-Phase PFC Converter with Flexible Output Voltage and Improved Conversion Efficiency is simulated using MATLAB/SIMULINK.***
Index Terms: Power Factor Correction (PFC), Flexible Output Voltage, Improved Conversion Efficiency.

I. INTRODUCTION

Power Factor Correction (PFC) shapes the input current of the power supply to be in synchronization with the mains voltage, in order to maximize the real power drawn from the mains. In a perfect PFC circuit, the input current follows. The input voltage as would an equivalent resistor, with no added input current harmonics. This document is intended to discuss the topology and operational mode for high power PFC applications (>300W), and provide detailed design equations with examples. Power Factor Correction (PFC) shapes the input current of the power supply to be in synchronization with the mains voltage, in order to maximize the real power drawn from the mains. In a perfect PFC circuit, the input current follows the input voltage as a pure resistor, without any input current harmonics. This document is to introduce a design methodology for the CCM PFC Boost converter, including equations for power losses estimation, selection guide of semiconductor devices and passive components, and a design example with experimental results.. However, the main power switches in these bridgeless topologies are still under high-voltage stress and the DCM operation also implies that they are only suitable for relatively low-power applications because of the high peak current in the boost inductor

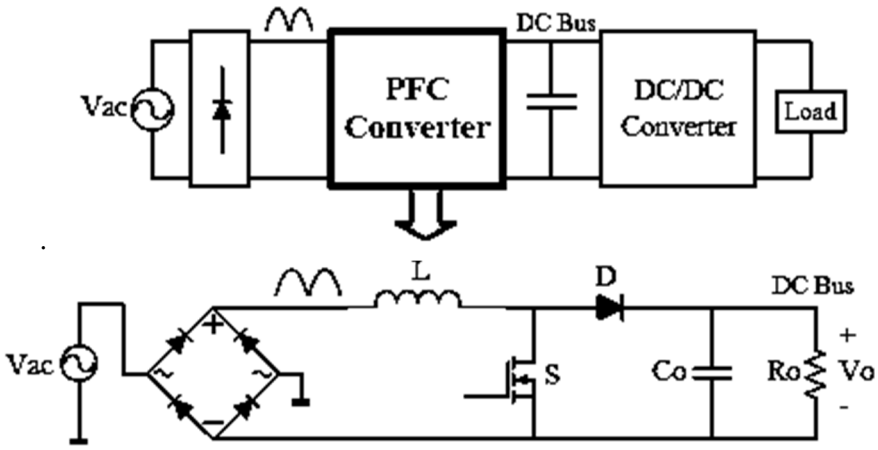

Figure 1: PFC converter

II. PFC MODES OF OPERATION

The boost converter can operate in three modes: continuous conduction mode (CCM), Discontinuous Conduction Mode (DCM), and Critical Conduction Mode (CrCM). By comparing DCM among the others, DCM operation seems simpler than CrCM, since it may

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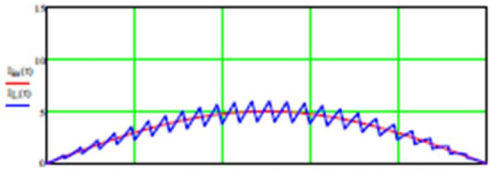
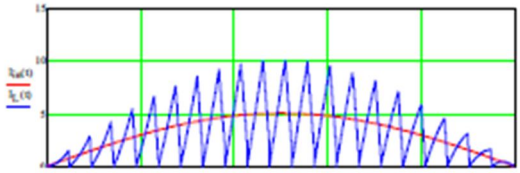
operate in constant frequency operation; however DCM has the disadvantage that it has the highest peak current compared to CrCM and also to CCM, without any performance advantage compared to CrCM. For that reason, CrCM is a more common practice design than DCM, therefore, this document will exclude the DCM design. CrCM may be considered a special case of CCM, where the operation is controlled to stay at the boundary between CCM and DCM. CrCM usually uses constant on-time control; the line voltage is changing across the 60 Hz line cycle, the reset time for the boost inductor is varying, and the operating frequency will change as well in order to maintain the boundary mode operation. CrCM dictates the controller to sense the inductor current zero crossing in order to trigger the start of the next switching cycle. The inductor current ripple (or the peak current) in CrCM is twice of the average value, which greatly increases the MOSFET RMS currents and turn-off current.



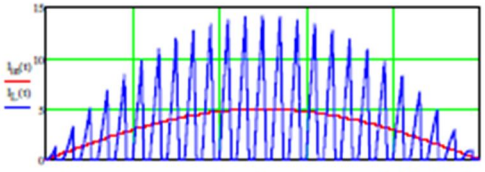
Continuous Conduction Mode (CCM)

On the other side, CCM encounters the turn-on losses in the MOSFET, which can be exacerbated by the boost rectifier reverse recovery loss due to reverse recovery charge, Qrr. For this reason, ultra-fast recovery diodes or silicon carbide Schottky diodes with extreme low Qrr are needed for CCM mode. In conclusion, we can say that for low power applications, the CrCM boost has the advantages in power saving and improving power density. This advantage may extend to medium power ranges, however at some medium power level the low filtering ability and the high peak current starts to become severe disadvantages. At this point the CCM boost starts being a better choice for high power applications.



Critical Conduction Mode (CrCM)

Since this document is intended to support high power PFC applications, therefore a CCM PFC boost converter has been chosen in the application note with detailed design discussions and design examples for demonstration.The current ripple (or the peak current) in CrCM is twice the average value, which greatly increases the RMS currents and turn off current. But since every switching cycle starts at zero current, and usually with ZVS operation, turn on loss is usually eliminated.



Discontinuous Conduction Mode (DCM)

III. WORKING OF PFC

Single-phase AC/DC converters are one of the most common power conversion systems and can be found in many industrial as well as residential applications, e.g., variable speed drive, electric vehicle chargers, and power supplies for consumer electronics. In order to meet the ever more stringent grid codes like the IEC61000-3-2 harmonic limits, high-power factor and sinusoidal current regulation are required for basically all such applications as long as their power ratings exceed 75W.

Presently, single-phase power factor correction (PFC) converters are a very popular solution to ensure the compliance of such regulations because of their simplicity, cost effectiveness, and good current shaping capability.

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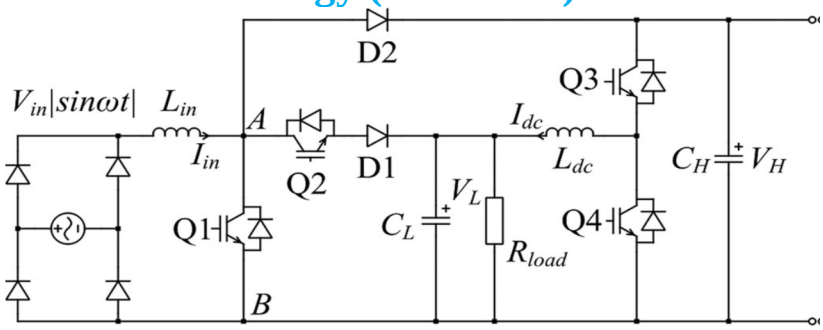

Figure.2 Circuit diagram of the proposed three-level PFC converter for single phase PHEV chargers.

However, most of the existing single-phase PFC converters are of boost type and can only provide an output voltage that is higher than the peak voltage of the ac input. Wide range of output voltage is indeed desired in some applications like in Plug-in Hybrid Electric Vehicle (PHEV) charging systems where the terminal voltage of battery packs may vary between 100V and 600V, depending on their configuration and state-of-charge. In this case, a second stage dc/dc buck converter has to be implemented to further step down the PFC output voltage, which undoubtedly decreases the system overall efficiency.

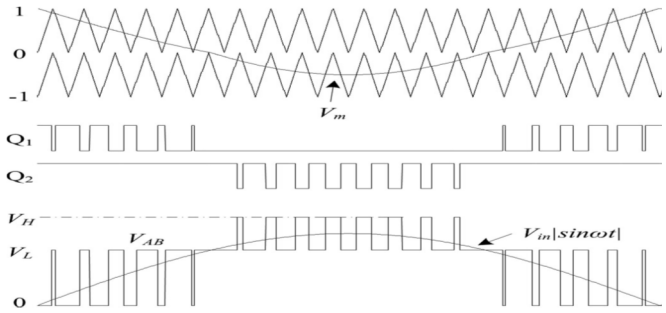

Figure.3 Idealized operating waveforms for the proposed three-level PFC Converter.

Is the root reason that why the dc/dc converter may only process partial input power and higher conversion efficiency can be obtained through the proposed topology. The idealized operating waveforms during these two modes are presented. In order to ensure smooth transition between the low- and high-voltage level commutations, an offset is injected into the carrier of the pulse-width modulation (PWM) for Q2.

Compared with the conventional boost PFC, the proposed converter will have slightly higher conduction losses because of the series connection of Q2 and D1. However, its switching losses can be greatly reduced due to its three-level output that splits the high dc bus voltage into two low voltage portions. Moreover, efficiency gain from the dc/dc converter is also significant because it only converts the input power that flow through D2. To estimate the percentage of input power λ that is converted by this buck stage, it is assumed that the power converter is lossless and harmonic free.

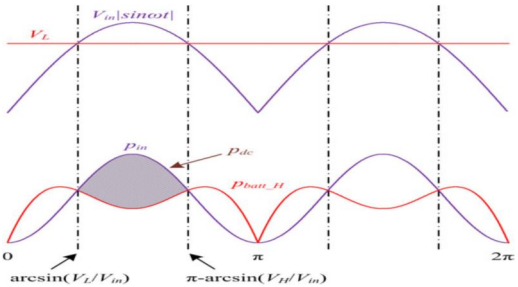

Figure.4 Instantaneous power distribution in the PFC converter and the buck Converter, given fixed gird voltage, output voltage, and dc-link voltage.

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IV. PRACTICAL IMPLEMENTATION

A. Simulation Study

Simulation study was carried out in MATLAB/Simulink environment and the circuit parameters are listed in. The steady-state operation waveforms are presented. It can be seen that Q1 and Q2 operate alternatively and may produce. The desired three-level converter pole voltage *V*AB. The high level bus voltage is not constant because the dc-link capacitor needs to absorb the system double line frequency harmonic.

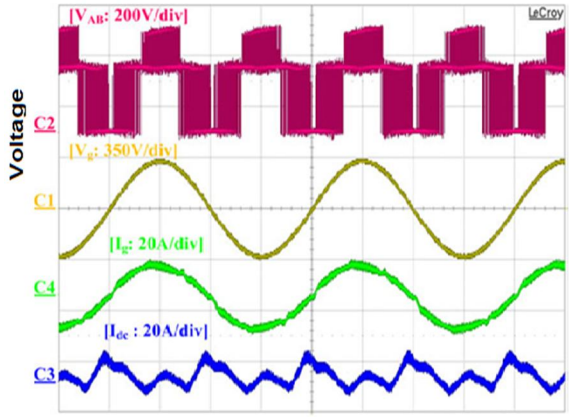

Figure.5 Experimental steady-state waveforms under 230-V/2-kW operation,
C1: grid voltage, C2: converter pole voltage, C3: buck converter current, and C4: grid current.

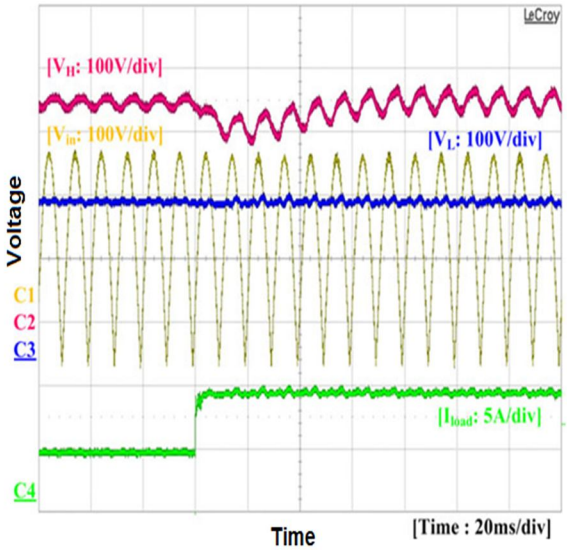

Figure.6 Experimental load step-up waveforms, C1: input voltage, C2: high dc bus voltage, C3: load voltage, and C4: load current.

Mentioned previously, this is because the intermittent operation of the buck converter may impose disturbances to the system and affect the input current regulation under high-line operation. The proposed PFC converter is also compared with a conventional two-stage solution, i.e., a boost PFC cascaded with a dc/dc buck converter, and its circuitry is obtained by removing D1 and Q2. Therefore, the proposed three-level PFC will have higher cost than the conventional one, and it is complicated with one fast recovery diode (D1), one switch (Q2), and one isolated gate driver.

B. Control Technique

The proposed control topology was first tested with standard 230-V/50-Hz high-line ac input and its corresponding steady state experimental waveforms are presented. It should be noted that there is very slight current distortion during the mode transition period.

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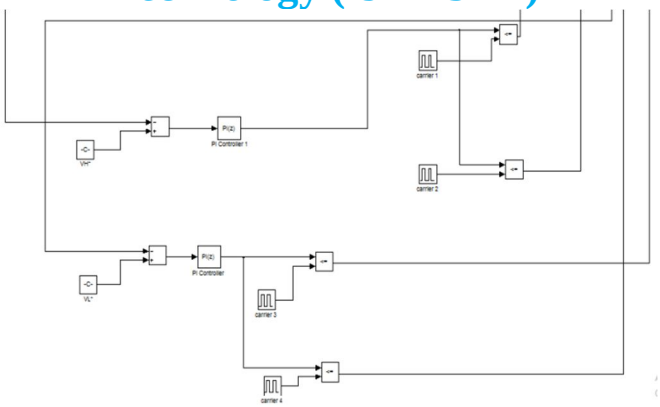

Fig.4.2 Control technique

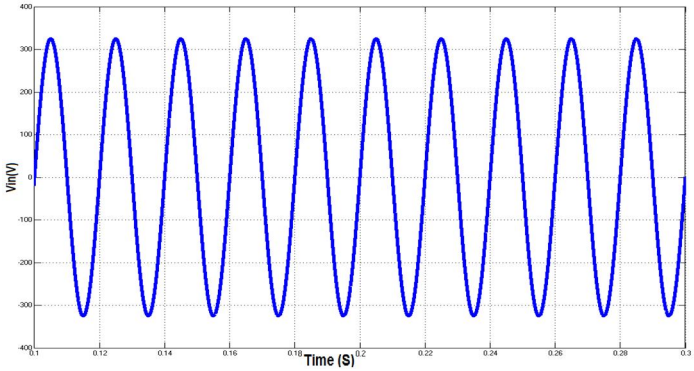

Fig.4.3 Input voltage

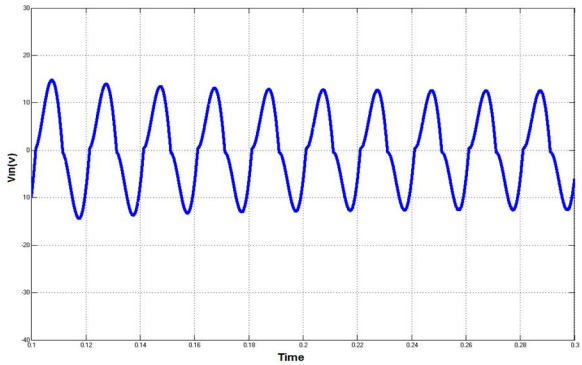

Fig.4.4 Input Current

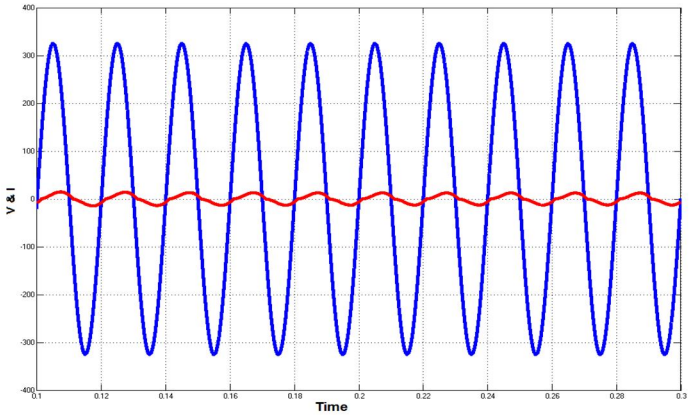

Fig.4.5 Input voltage & current in mux

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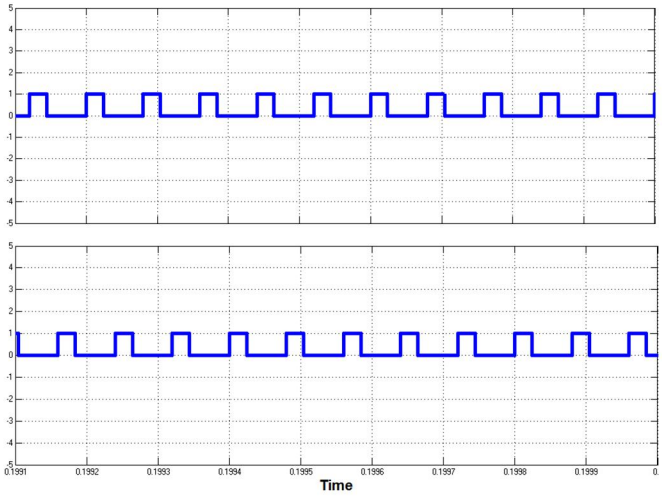

Fig.4.6 Gate pulses

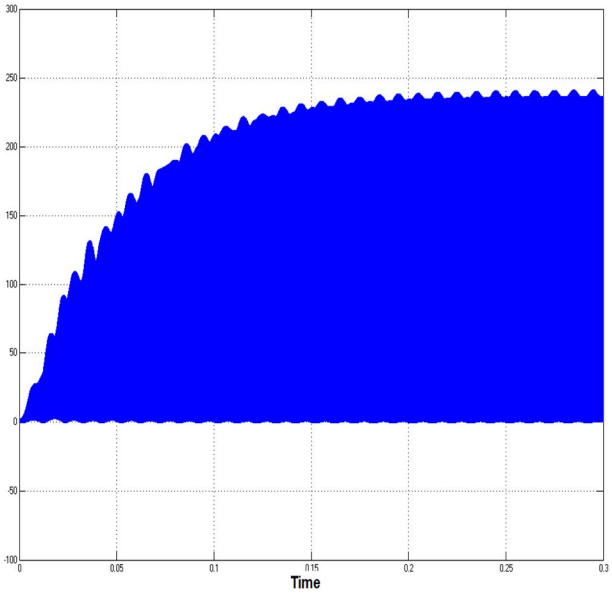

Fig 4.7 Vab

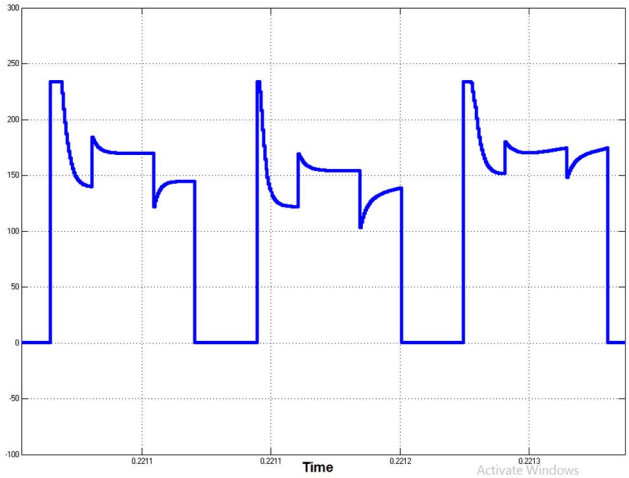

Fig.4.8 Vab zoomed view

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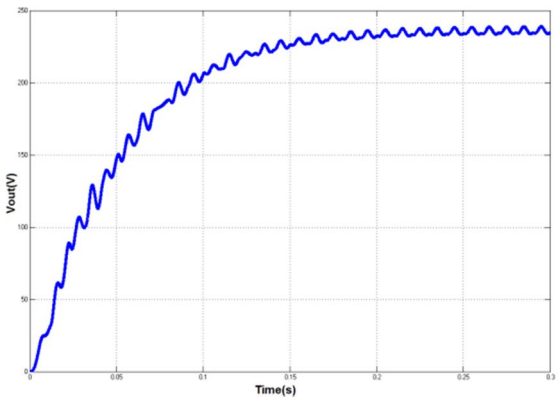

Fig.4.9 Output voltage

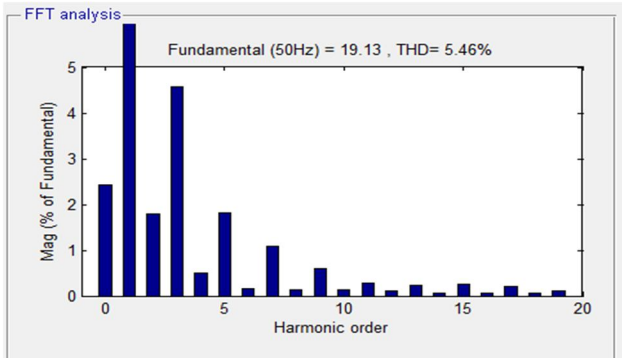

Fig.4.10 THD for input current

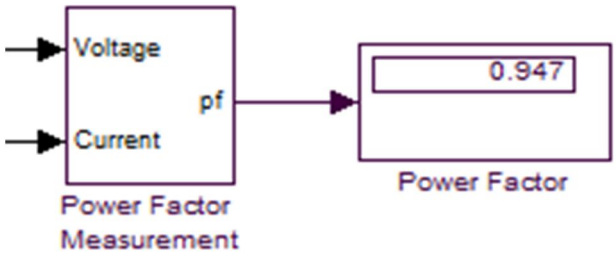

Fig.4.11 Power factor

V. CONCLUSION

In this paper, a three-level quasi-two-stage single-phase PFC converter has been presented. It has flexible output voltage and can be used for single-phase PHEV charger applications, where the battery voltage can be either lower or higher than the peak ac input voltage. The proposed converter features high quality input current, three-level output voltage, and improved conversion efficiency.Therefore, the grid current can be well regulated with low THD and high-power factor. Experimental results obtained from a 2-kW laboratory prototype have been presented in the paper, which are in good agreement with the theoretical analysis. The efficiency curves under universal input conditions were recorded from a commercial power analyzer, and it is found that the proposed PFC may have 1% efficiency gain under high-line operation as compared to a conventional cascaded two-stage solution. This efficiency improvement is partly contributed by the reduced switching voltage in the PFC stage, and also partly by the reduced power conversion in the dc/dc buck stage.

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BIOGRAPHY

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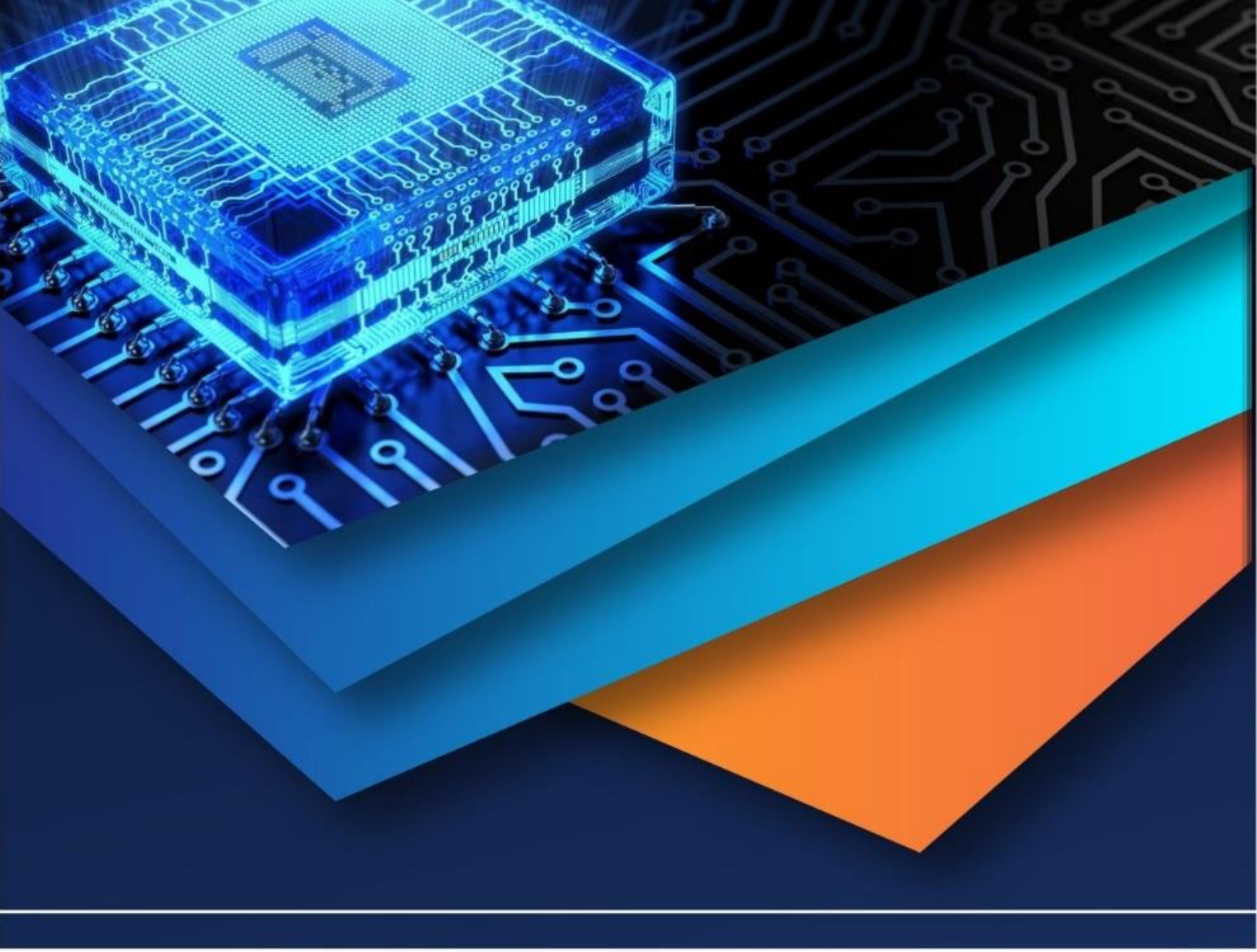

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