iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 4 **Issue:** V **Month of publication:** May 2016

DOI:

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Comparative Study on Implementation of Digital Arithmetic Circuit

Lavanya B K[1], Sumiksha[2], Jose Alex Mathew[3], Praveen Kumar Konda[4], Savidhan Shetty[5], Praveen Kumar M[6]
[1,2]*M.Tech in VLSI Design & Embedded Systems,* [3]*HOD,* [4,5,6]*Assistant Professor*
[3,4,5,6]*Dept. Electronics & Communication Engineering ,Sahyadri college of Engineering & Management, India*

Abstract: Multiplier and adders play's an important role in many applications, basically we need to reduce the delay, power, area in any VLSI design implementation, so we need consider suitable algorithm of multipliers and adders. In this paper we have compared different multiplier and adder algorithms such as vedic, KOM and parellel prifix adder.
Keywords – KOM, vedic multiplier, parallel prefix adder

I. INTRODUCTION

In today's digital era, multipliers and adders play an very important role, where in many researchers have tried to design these multipliers and adders which satisfy the following criteria such as speed, low power consumption, area for implementation. They perform convolution, fast Fourier transforms. Depending on the components basis multipliers and adders divided into various class. one of the basic factor which is been considered during the designing of the multipliers and adders are its delay, speed, area.

II. MULTIPLIERS

Multiplier plays an important role in all digital circuit design .Multiplier is one of the fast and reliable component used for any operations. Depending on requirement of applications multiplier architecture is been selected .Different types of multiplier architecture are available.

A. Vedic Multiplier

Vedic mathematics is mainly based on 16 aphorism (sutras). Ancient system of Indian mathematics was given by a name called Vedic mathematics, the word veda means store-house of all knowledge. The word vedic is derived from the word veda. Aapplications introduces by Vedic Mathematics for Arithmetical computations, theory of numbers, compound multiplications, algebraic operations, factorizations, simple quadratic and higher order equations, simultaneous quadratic equations, partial fractions, calculus, squaring, cubing, square root, cube root, coordinate geometry and wonderful Vedic Numerical code. Multiplier designed by making use of Vedic Mathematics is one of the fast and low power multiplier. We can reduce the complexity, execution time and power, by using this technique in the computation algorithms. Sr Bharati Krushna Tirthaji Maharaj rediscovered an ancient system of calculation which was from Vedas known as "Vedic Mathematics". The Vedic Mathematics is popular because of its simplicity and flexibility in carrying out the calculations mentally.
Two main Sutras for multiplication are
Urdhva- Tiryagbhyham
Nikhilam Navatashcaramam Dashatah.

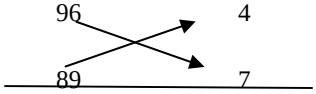
1) Nikhilam Navatashcaramam Dashatah: Nikhilam algorithm is a sutra or method coming from Vedic mathematics. It is used to perform efficient multiplication for small inputs. Nikhilam algorithm performs multiplication operation by converting large multiplication to small multiplication along with some addition, subtraction and shifting operations. Although Nikhilam Navatashcaramam Dashatah sutra can be applied to all cases of multiplication, it is more suitable when the numbers involved in multiplication are large and this formula can be very effectively applied in multiplication of numbers, which are nearer to bases like 10, 100, 1000.i.e. to the powers of 10 The power of 10 from which the difference is calculated is called the Base. These numbers are considered to be references to find out whether given number is less or more than the Base. These numbers are considered to be references to find out whether given number is less or more than the Base.

The algorithm of this sutra is explained as follows.
The base to be chosen is 100 as it is nearest to and greater than both these two numbers i.e.,(100-96 = 4 and 100-93 = 7).
The right hand side (RHS) of the result is found by finding the product of numbers of Column2 i.e., 7*4 = 28). The left hand side (LHS) of the product can be found by cross subtracting the second number of Column 2 from the first number of Column or vice versa i.e., (93 -4) = 89 or (96-7) = 89.

©IJRASET: All Rights are Reserved

The final result is obtained by concatenating RHS and LHS which is 8928.

96*93
Nearest base = 100
96 (100-96)
93 (100-93)
Column 1 Column 2
96 4



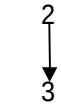
89 7
89 28
Result = 8928
Multiplication using Nikhilam Sutra.

2) Urdhva-Tiryagbyham Sutra(UT): Among the 16 suthra UT is among it, which is an efficient multiplication operation which is used for all kind of multiplication. This type of sutra are applied for binary multiplication. UT sutra work on the principle of vertical and crosswise multiplication. During the multiplication operation suppose if any carry is been generated then this carry will added with next operation obtained result, during the initial state the carry is considered to be 0.

The following are the steps used to show the UT sutra.
In order to find the unit place we need to multiply the unit place of the given number which is been known as vertical multiplication.
We need to cross multiply the given number and then we need to add the product. The obtained product, if it contains two digits then the place digit is considered as an carry then this carry is used for next operation of multiplication.
Vertical multiplication is done, and then carry of the previous step is added to the obtained product.

Example
22*33

1) 2 2



3 3
2*3=6

2) 2 2

3 3
2*3=6
2*3=6
6+6=12, 1: carry

3) 2 2

3 3
2*3=6+1=7

22*33=726

B. Karastubha-Ofman Multiplier

KOM which is known as karastuba ofman multiplier. This algorithm was been discovered by the "AnatoliiAlexeevitchKaratsuba ". KOM performs the multiplication operation faster. This algorithm will reduces the number of bits during the multiplication process, when we compare KOM algorithm with classic algorithm it is considered to be faster. recursive operation is been performed in KOM algorithm. Recursion is occurred until the number become very small and computation can be performed clearly.
KOM is given in equation by

$$P_{KOM} = P_L Q_L + (P_L Q_H + P_H Q_L) S^{n/2} + (P_H Q_H) S^n \quad .....(1)$$

Where S=2 for an binary systems
P and Q operands are the size of the n-bits which is been considered during the multiplication process.

©IJRASET: All Rights are Reserved

$P = 0011_{(2)}$
$Q = 1001_{(2)}$
S=2 for binary numbers n=4 bits
$P_L = 11_{(2)}$ and $P_H = 00_{(2)}$
$Q_L = 01_{(2)}$ and $Q_H = 10_{(2)}$
$P_LQ_L = 11_{(2)} \times 01_{(2)} = 0011_{(2)}$.
$(P_LQ_H + P_HQ_L)\ S^{n/2} = (11_{(2)} \times 10_{(2)} + 00_{(2)} \times 01_{(2)})\ S^2$
$= (0110_{(2)} + 0000_{(2)})\ S^2 = 011000_{(2)}$;
Shifted left by 2 bits.
$(P_HQ_H)\ S^n = (00_{(2)} \times 10_{(2)})\ S^4 = 00000000_{(2)}$ $(P_LQ_H + P_HQ_L)\ S^{n/2} = 011000_{(2)}$
Above obtained product is been decomposed into $01_{(2)}$ and $1000_{(2)}$
to make $01_{(2)}$ as 4 bit Zero extension is used.

KOM architecture shown in below figure

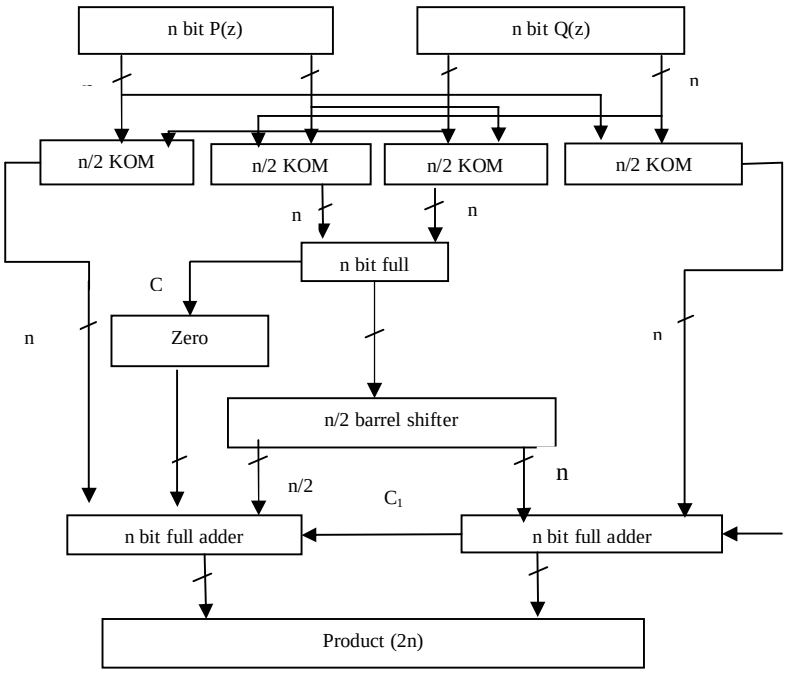


Figure1. KOM architecture

In the above architecture we make use of an barrel shifter, barrel shifter is used in order to shift the bits by 2 place towards the left. Zero extension is been used in order to make the 2 bit obtained as 4 bit. KOM architecture performs the operation with comparatively less delay in any system which in turn reduces the delay and hence increases the performance.

III. ADDERS

Adders are used to perform the addition of two operand, among the different adders like ripple-carry adders Carry-skip adder, carry-select adder and carry-increment adder the frequently used adders in VLSI implantation is parallel prefix adder.

A. Parallel Prefix Adder

In high speed application devices it makes use of an parallel prefix adder. It performs parallel addition operation; making use of such adder will reduce the delay and logic complexity along with area and power.
Parallel prefix adder computation is been carried out by 3 important steps:
By making use of number of inputs, generate and propagate signals have been computed.
Prefix computation have been computed.
Calculating the total sum of given inputs.

©IJRASET: All Rights are Reserved

Volume 4 Issue VI, June 2016
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

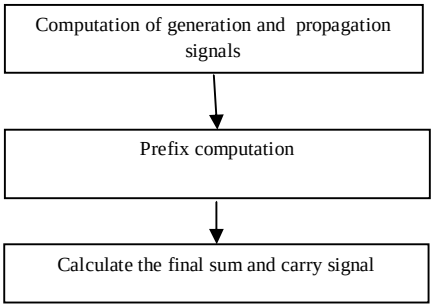


Figure 2 Parallel-Prefix adder mechanism

The block diagram have been explained as follows :
Intial we need to calculate propagate and genarate signal from the given inputs.propagation signal have been obtained by making an XOR operation for an given inputs. Generate signal have been obtained by making an AND operation for an given inputs.
Which is given in below equcation:

$$Gi = Xi \,.\, Yi \qquad \text{.....(2)}$$
$$Pi = Xi \oplus Yi \qquad \text{.....(3)}$$

In the second step we cosider two cells ,Gray cell and Black cell.Gray cell computes only a carry genarate signals and the Black cell computes both the carry generate and propagate signals by using an expression given below:

$$Gi{:}j = Gi{:}k + Pi{:}k \,.\, Gk{-}1{:}j \qquad \text{.....(4)}$$
$$Pi{:}j = Pi{:}k \,.\, Pk{-}1{:}j \qquad \text{.....(5)}$$

In the 3rd step the carry which is been genarated in the secong stage XOR rd with the intial propagate signal,which can be writtin by using equcation:

$$Si = Pi \oplus Ci{-}1 \qquad \text{.....(6)}$$

B. Kogge-Stone Adder

Kogge stone adder is one type of parallel prefix adder whose operation similar to that of carry look a head adder .Here black cell is connected in vertical which produces both carry propagate and generate signal. The carry generate signal are produced in last stage of second step using grey cells. To produce the sum, the carry which is been genarated in the secong step XORed with the intial propagate signal.
Carry Stages: log2 n
The number of cells: nlog2 n
Maximum:fan-out:2

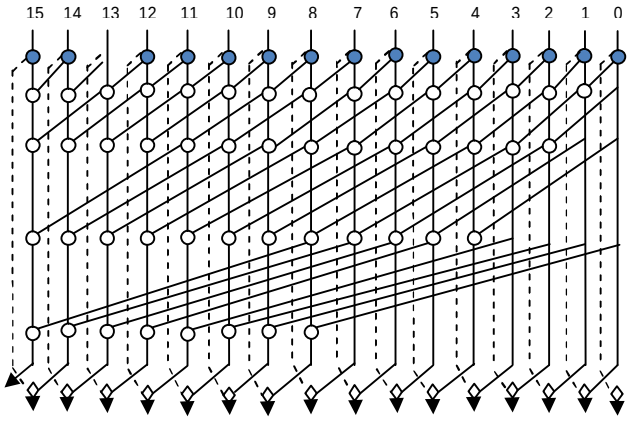


Figure 3 16-bit Kogge-Stone Adder

C. Brent Kung Adders

By making use this adder we can reduce the area and also avoid the burst of wires. Here we perform odd and even

©IJRASET: All Rights are Reserved

computations where odd computation performed first and later even. First we need to calculate the prefix for 2-bits which in turn is used calculate prefix for 4 bit and so on. In order to find the carries to each bit computed prefix is been fed-back. To calculate the sum the carry generated will be XORed with initial propagate signal

Carry Stages: 2log2 n-1;

The number of cells: 2(n-1)-log2 n;

Maximum fan-out: 2.

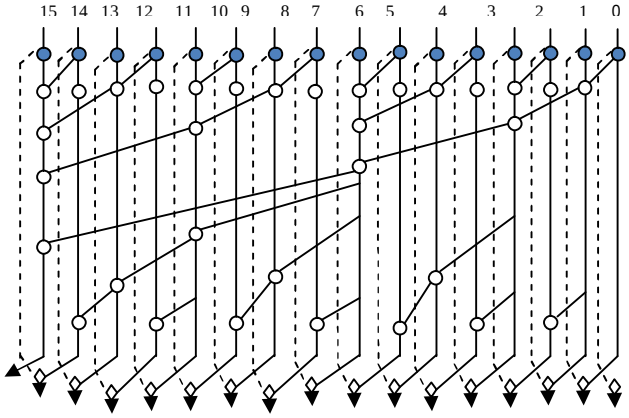


Figure 4 16-bit Brent-Kung Adder

D. Han-Carlson Adder

This adder is an network between 2 different types of parallel prefix adder which is KSA and BKA .it have been viewed as an dense version of KSA. Here carry merging operation have been performed on even bits and carry generate and propagate operations on or bits . To produces the true carry bits both odd and even bits recombined, then these carry bits are XORed with initial propagate signal to calculate the sum.

Carry Stages: $\log_2 n$

The number of cells: $(n/2).\log_2 n$

Maximum fan-out: n/2

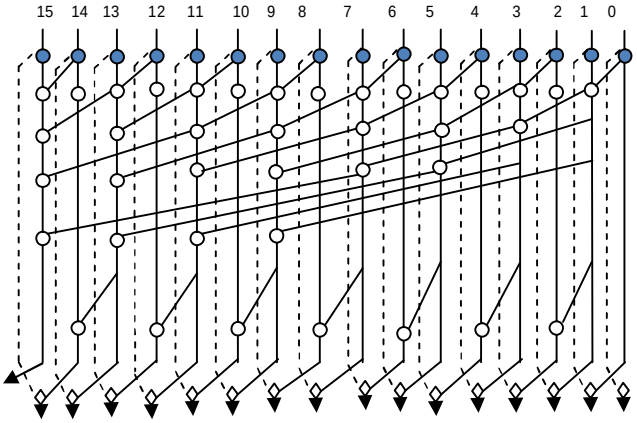


Figure 5 16-bit Han-Carlson adder

IV. COMPARISON OF DIFFERENT MULTIPLIERS AND ADDER

Bits	Name	Slices	Speed	Delay	Power
8	Vedic	225	118.203MHz	8.460ns	9.29mW
8	KOM	277	154.64 MHz	11.86ns	6.311 mW

Table 1 Different Multipliers

©IJRASET: All Rights are Reserved

Name of adder	Inputs (Bits)	Delay (ns)	Area (um^2)	Power (mW)
Kogge-Stone	16	9.4	1723	140.228
Brent-kung	16	10.4	2609	100.5192
Ladner-Fischer	16	9.9	4336	107.9553
Han-carlson	16	9.9	-	109.24903

Table 2 Different Adders

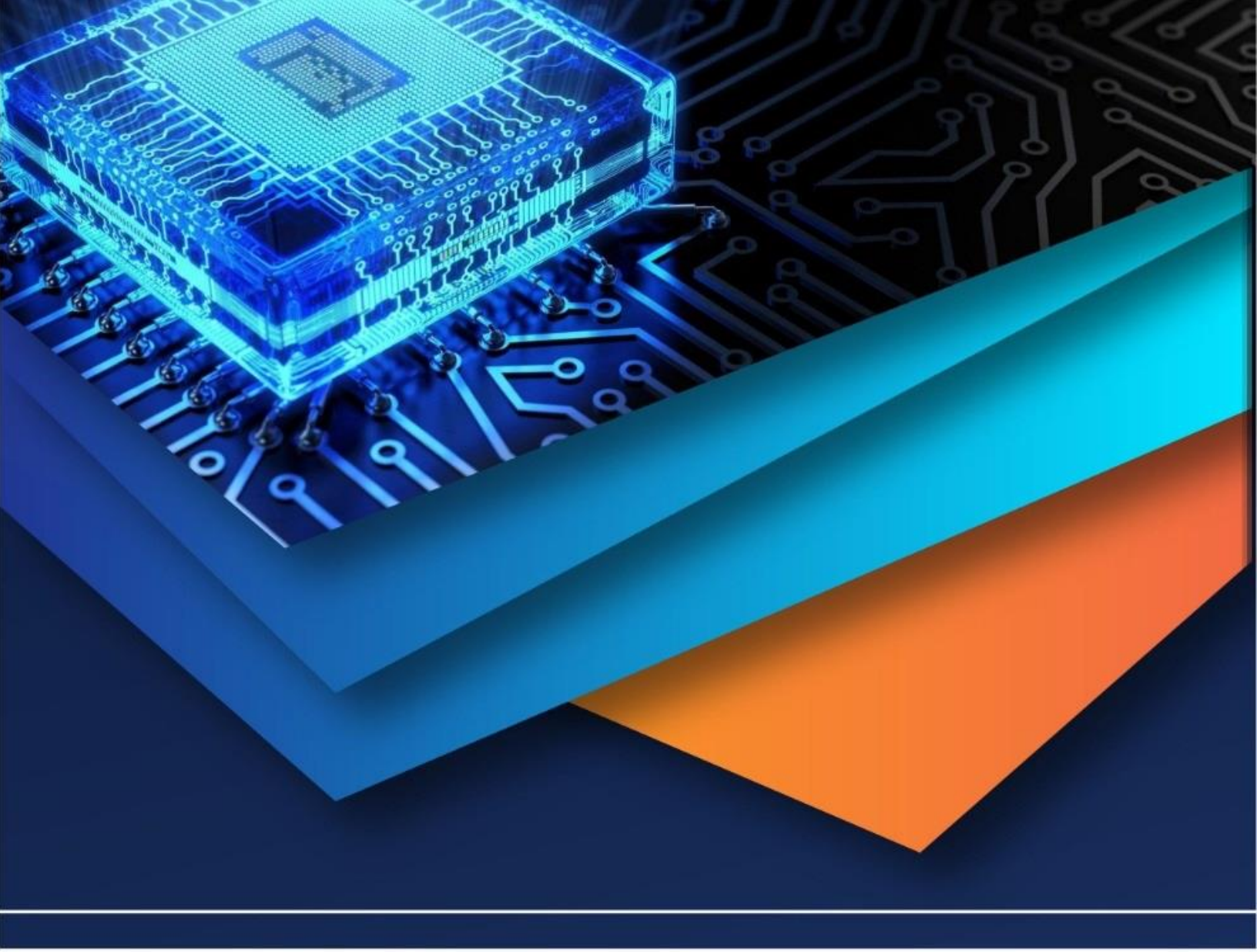
V. CONCLUSION

From the observation of different algorithms we can conclude that kom multiplier gives more delay and less power consumption when it is compared to the vedic multiplier. By comparing different adder we can conclude that Kogge-Stone has least logic levels but hard to Propagate and generate. Han-Carlson has more logic levels but fewer cells Kogge-Stone adder is the best among the others, because it has less delay and area compared with other adders.

REFERENCES

[1] Murugesan G. and Lavanya S," Design And Implementation Of High Speed Multiplier Using Vedic Mathematics," ARPN Journal of Engineering and Applied Sciences , VOL. 10, NO. 16, SEPTEMBER 2015
[2] Nagarjun B and Poonam Sharma, "Design and FPGA Implementation of a simple time efficient KOM Multiplier," IOSR Journal of Electronics and Communication Engineering (IOSR-JECE) e-ISSN: 2278-2834,p- ISSN: 2278-8735.Volume 9, Issue 5, Ver. V (Sep - Oct. 2014), PP 35-3
[3] Marco Bodrato," Notes on Low Degree Toom-Cook Multiplication with Small Characteristic,"
[4] Piyush S. Kasat, Devendra S. Bilaye, Harish V.Dixit, Rahul Balwaik, and Amutha Jeyakumar, " Multiplication Algorithms for VLSI – A Review,"International Journal on Computer Science and Engineering (IJCSE), Vol. 4 No. 11 Nov 2012
[5] D J McLaren, "Improved Mitchell-based Logarithmic Multiplier for low-power DSP applications," Proceedings of IEEE International System On Chip Conference, pp. 53-56, September 2003.
[6] GeetaRani and Sachin Kumar, "Delay Analysis of Parallel-Prefix Adders," International Journal of Science and Research (IJSR) Volume 3 Issue 6, June 2014
[7] Bharti B. Tiple and RupaliSuraskar, "Design of Improved High Performance of High Valency Ling Adder," International Journal of Innovative Research in Computer and Communication Engineering (An ISO 3297: 2007 Certified Organization) Vol. 4, Issue 2, February 2016
[8] Srinivasasamanoj.R,, M. Sri Hari and B. RatnaRaju, " High speed VLSI implementation of 256-bit Parallel Prefix Adders International Journal of Wireless Communications and Networking Technologies," Volume 1, No.1, August- September 2012
[9] RajithaChandragiri and P. VenkataLavanya, "Design and Testing Of Prefix Adder for High Speed Application by Using Verilog HDL," International Journal of Computational Engineering Research,Vol, 03,Issue, 8,August 2013

©IJRASET: All Rights are Reserved



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Call : 08813907089 (24*7 Support on Whatsapp)