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Design of a High Speed 32-Bit Parallel Hybrid Adder for Digital Arithmetic System

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Abstract*—Addition is a heavily used basic fundamental arithmetic operation that figures prominently in any digital logic system, digital signal processor, control system and scientific applications. Addition is a very hardware intensive subject and one as users are mostly concerned with getting low smaller area and higher speed. In ALU, adders play a major role not only in addition but it also performing many other basic arithmetic operations like subtraction, multiplication, etc. Hence, realization of an efficient adder is required for better performance of an ALU and therefore the processor. This paper presents the design of 32-bit Parallel Hybrid Adder architectures consists of Ripple Carry Adder, Carry Look Ahead Adder and Carry Select Adder. The time delay and area have been analyzed. Results will show the variation of area and speed for different designs. The designed adder consists of parallel implementation of 8-bit Ripple Carry Adder and 8-bit Carry Look Ahead Adder together to form 32-bit Parallel Hybrid Adder. The 32-bit Parallel Hybrid Adder is synthesized for XC3S1600 of Spartan-3E FPGAs implemented in 90nm technology.

***Keywords*— Area Efficient, CLA, CSA, Low Propagation Delay, RCA**

I. INTRODUCTION

The saying goes that if one can count, you one control. Addition is a fundamental operation for any digital system, digital signal processor or control system. A fast and accurate operation of a digital system is greatly influenced by the performance of the adders. Adders are also very important component in digital systems because of their extensive use in other basic digital operations such as subtraction, multiplication and division. Hence, improving performance of the digital adder would greatly advance the execution of binary operations inside a circuit compromised of such blocks. The performance of a digital circuit block is gauged by analysing its power dissipation, layout area and its operating speed. Addition is the most important operation in any digital system. All other arithmetic operations, like subtraction, multiplication and division are deeply related to the addition; hence, the design of a fast, accurate and low power binary adder translates to gain in simulation speed and an increase in battery life for portable computing systems.

A. Statements of Problem

Day by day IC technology is getting more complex in terms of design and its performance analysis. A faster design with lower power consumption and smaller area is implicit to the modern electronic designs. Unceasing advancement in microelectronics design technology makes improved use of energy, encrypt data successfully, communicate information much more steadfastly, etc. Adders generally have extended latency, huge area and consume substantial amount of power. Hence high speed adder design has become an important part in VLSI system design. Everyday new approaches are being developed to design high speed adders at technological, physical, circuit and logic levels. Since the adder is generally the slowest element in a system, the system's performance is determined by performance of the adder. Also adders are the most area consuming entity in a design. Therefore, optimizing speed and area of an adder is a major design issue nowadays. However, area and speed are usually conflicting constraints so that improving speed results in larger areas and vice-versa. Also area and power consumption of a circuit are linearly correlated. So a compromise has to be done in speed of the circuit for a greater improvement in reduction of area and power.

B. Objectives

The objectives of this project are as follow:

1) To study Parallel Adders.
2) To obtain comprehensive overview of different adder's delay and area constraints.

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3) To design of 32-bit Parallel Hybrid Adder includes -
4) Design of 8-bit hybrid adder using Ripple carry adder & Carry Lookahead adder
5) To reduce propagation delay i.e. increases the speed of adder.

II. LITERATURE REVIEW

Padma Devi et al 2010 proposed [1] modified carry select adder designed in different stages. Results obtained from modified carry select adders are better in area and power consumption. Shivani Parmar and Kirat Pal Singh 2012 [2] propose a scheme which reduces the delay, area and power than conventional CSA. The overall improvement in Modified CSA shows better results in terms of area power and delay. Hence, proposed modified CSA is being used for power and area efficient devices. V. Kokilavani and K. Preethi [4] propose seven different carry select adders were implemented and their performances were analysed. The hybrid carry select adder comprising the proposed carry select and section-carry based carry Lookahead configurations is the fastest.

III. PARALLEL ADDERS

Parallel adders are digital circuits that compute the addition of variable binary strings of equivalent or different size in parallel. There are different types of adder which are mentioned as follow.

A. *Ripple Carry Adder*

The ripple carry adder is constructed by cascading full adders (FA) blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage. A number of full adders may be added to the ripple carry adder or ripple carry adders of different sizes may be cascaded in order to accommodate binary vector strings of larger sizes.

For an n-bit RCA, it requires n computational elements (FA). Figure 1 shows an example of a parallel adder: a 32-bit ripple-carry adder. It is composed of thirty-two full adders. The augends' bits of 'a' are added to the addend bits of 'b' respectfully of their binary position. Each bit addition creates a sum and a carry out. The carry out is then transmitted to the carry in of the next higher-order bit. The final result creates a sum of thirty-two bits plus a carry out (c31). The expressions for the output sum and the carryout are given by:

$$S_i = A_i \oplus B_i \oplus C_i \qquad \text{------ (1)}$$

$$C_{i+1} = A_i B_i + A_i C_i + B_i C_i \qquad \text{------ (2)}$$

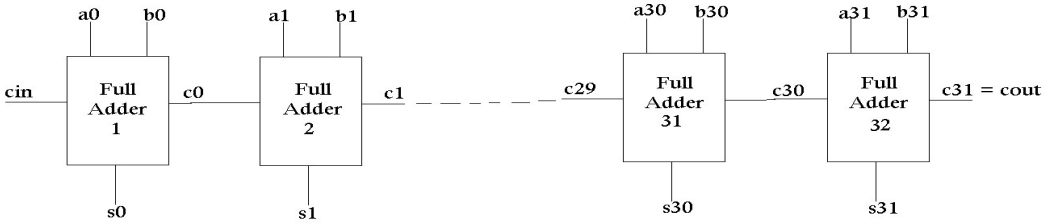

Figure 1: 32-bit RCA

The worst-case delay of the RCA [2] is when a carry signal transition ripples through all stages of adder chain from the least significant bit to the most significant bit, which is approximated by:

$$T = (n - 1)\, tc + ts \qquad \text{------ (3)}$$

Where, tc is the delay through the carry stage of a full adder and ts is the delay to compute the sum of the last stage. The delay of ripple carry adder is linearly proportional to n, the number of bits; therefore the performance of the RCA is limited when n grows bigger. The advantages of the RCA are lower power consumption as well as a compact layout giving smaller chip area.

B. *Carry Look-Ahead Adder*

As seen in the ripple-carry adder, its limiting factor is the time it takes to propagate the carry. The carry look-ahead adder solves this problem by calculating the carry signals in advance, based on the input signals. The result is a reduced carry propagation time.

To be able to understand how the carry look-ahead adder works, we have to manipulate the Boolean expression dealing with the full adder. The Propagate P and generate G in a full-adder, is given as:

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$$Pi = Ai \oplus Bi \quad \text{------ (4)}$$

$$Gi = AiBi \quad \text{------ (5)}$$

Notices that both propagate and generate signals depend only on the input bits and thus will be valid after one gate delay. The new expressions for the output sum and the carryout are given by:

$$Si = Pi \oplus Ci \quad \text{------ (6)}$$

$$Ci+1 = Gi + PiCi \quad \text{------ (7)}$$

The delay of carry Lookahead adder [2] is 4 levels of logic which is given by:

$$T = tp + tg + tc + ts \quad \text{------ (8)}$$

Where, tp is the delay generated during carry propagate level, tg is the delay generated during carry generate level, tc is delay generated during carryout stage and ts is the delay to compute the sum of the last stage.

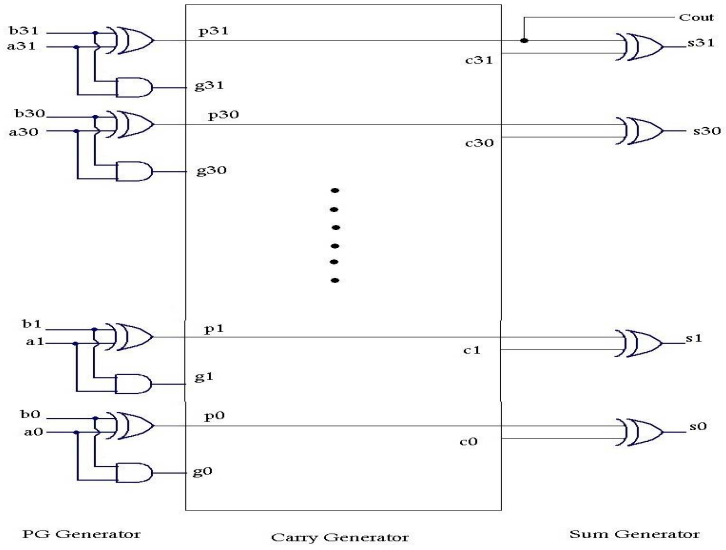

Figure 3: 32-bit CLA

C. Carry-Select Adder

The concept of the carry-select adder is to compute alternative results in parallel and subsequently selecting the correct result with single or multiple stage hierarchical techniques. In order to enhance its speed performance, the carry-select adder increases its area requirements. In carry-select adders both sum and carry bits are calculated for the two alternatives: inputs carry "0" and "1". Once the carry-in is delivered, the correct computation is chosen (using a MUX) to produce the desired output. Therefore instead of waiting for the carry-in to calculate the sum, the sum is correctly output as soon as the carry-in gets there. The time taken to compute the sum is then avoided which results in a good improvement in speed. This concept is illustrated in Figure 4 for Carry select adder with Ripple Carry Adder and also in Figure 6 for Carry select adder with Carry Lookahead Adder.

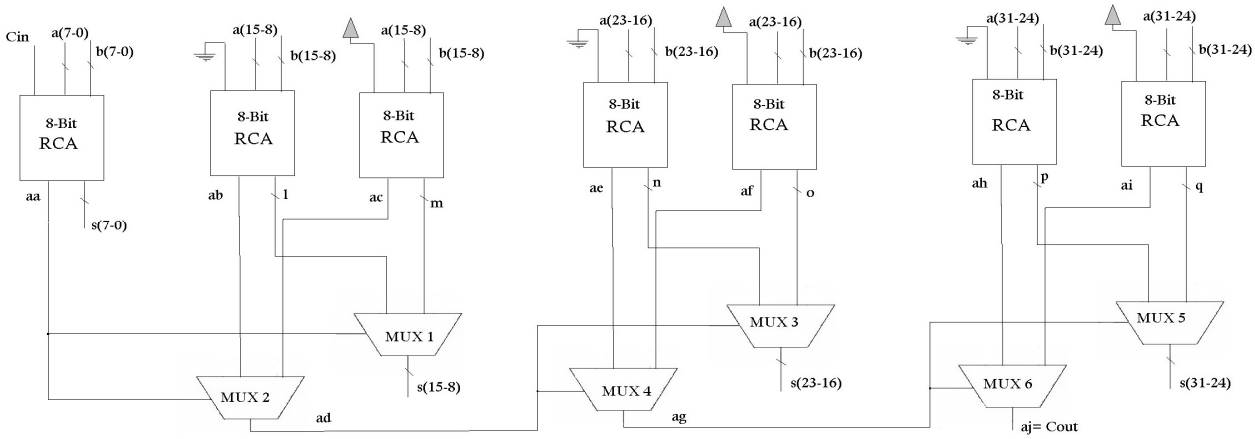

Figure 4: 32-bit CSA_RCA

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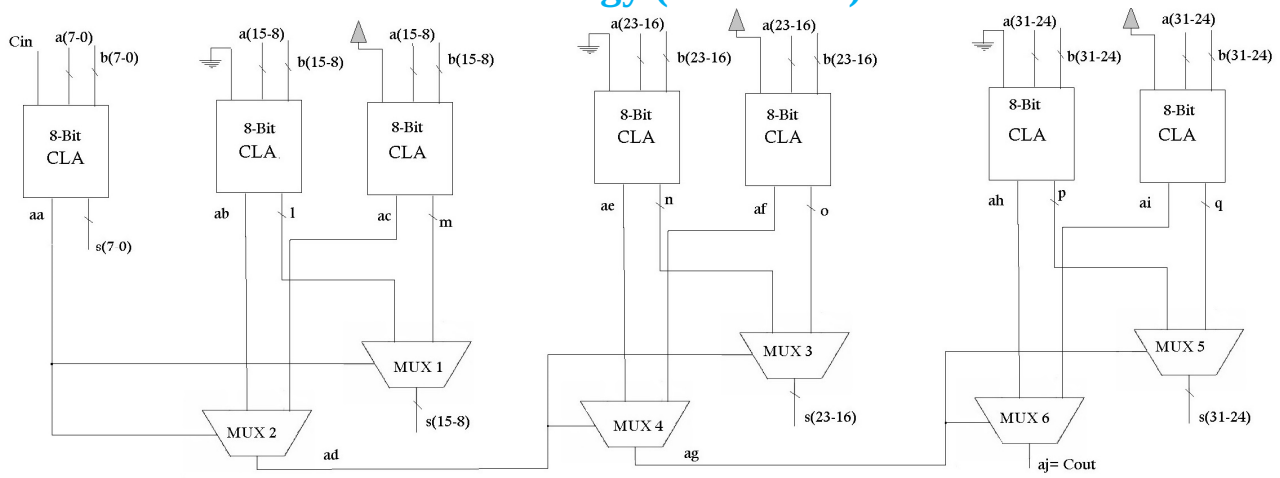

Figure 6: 32-bit CSA_CLA

IV. PARALLEL HYBRID ADDER

Parallel hybrid Adder is combination of Carry-select adders along with ripple carry adder and carry Lookahead adder. To design parallel hybrid adder, we divided 32-bit adder into equal section of 8-bit each. 8-bit section consists of 8-bit Ripple carry adder or 8-bit Carry Lookahead adder. One of these adders is fed with a 0 as carry-in whereas the other is fed a 1. Then using a multiplexer, depending on the real carryout of the previous section, the correct sum is chosen. Similarly, the carryout of the section is computed twice and chosen depending of the carryout of the previous section. The concept can be expanded to any length. This is referred as linear expansion. The figure 8 shows the parallel hybrid adder architecture.

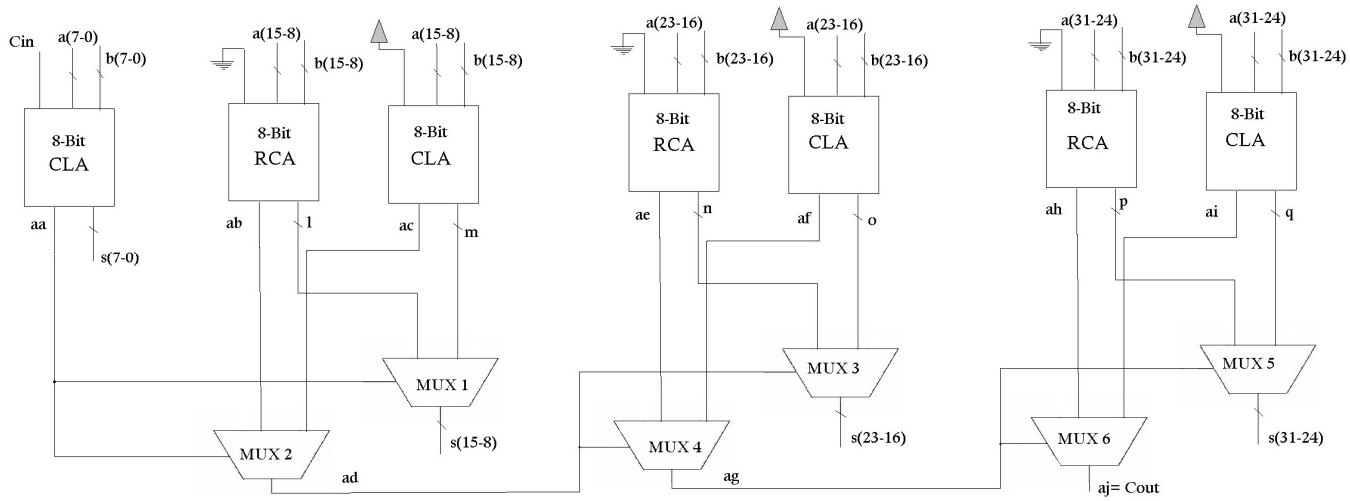

Figure 8: 32-bit CSA_CLA_RCA

The delay of n-bit carry select adder [2] based on an m-bit RCA or CLA blocks can be given by the following equation when using constant carry number blocks

$$T = m\,tc + (n/m)\,tmux + ts \qquad \text{------ (9)}$$

Where, tc is the delay through the carry stage of a full adder, ts is the delay to compute the sum of the last stage, tmux is the delay through the multiplexer stages, m is constant carry number blocks

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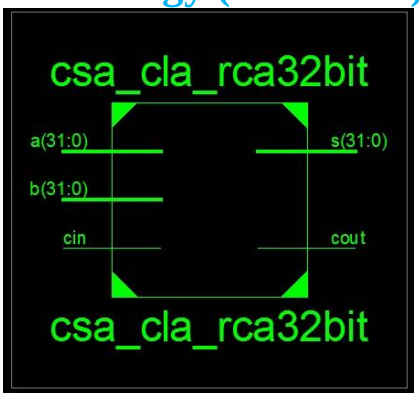

Figure 9: RTL Viewer of 32-bit CSA_CLA_RCA

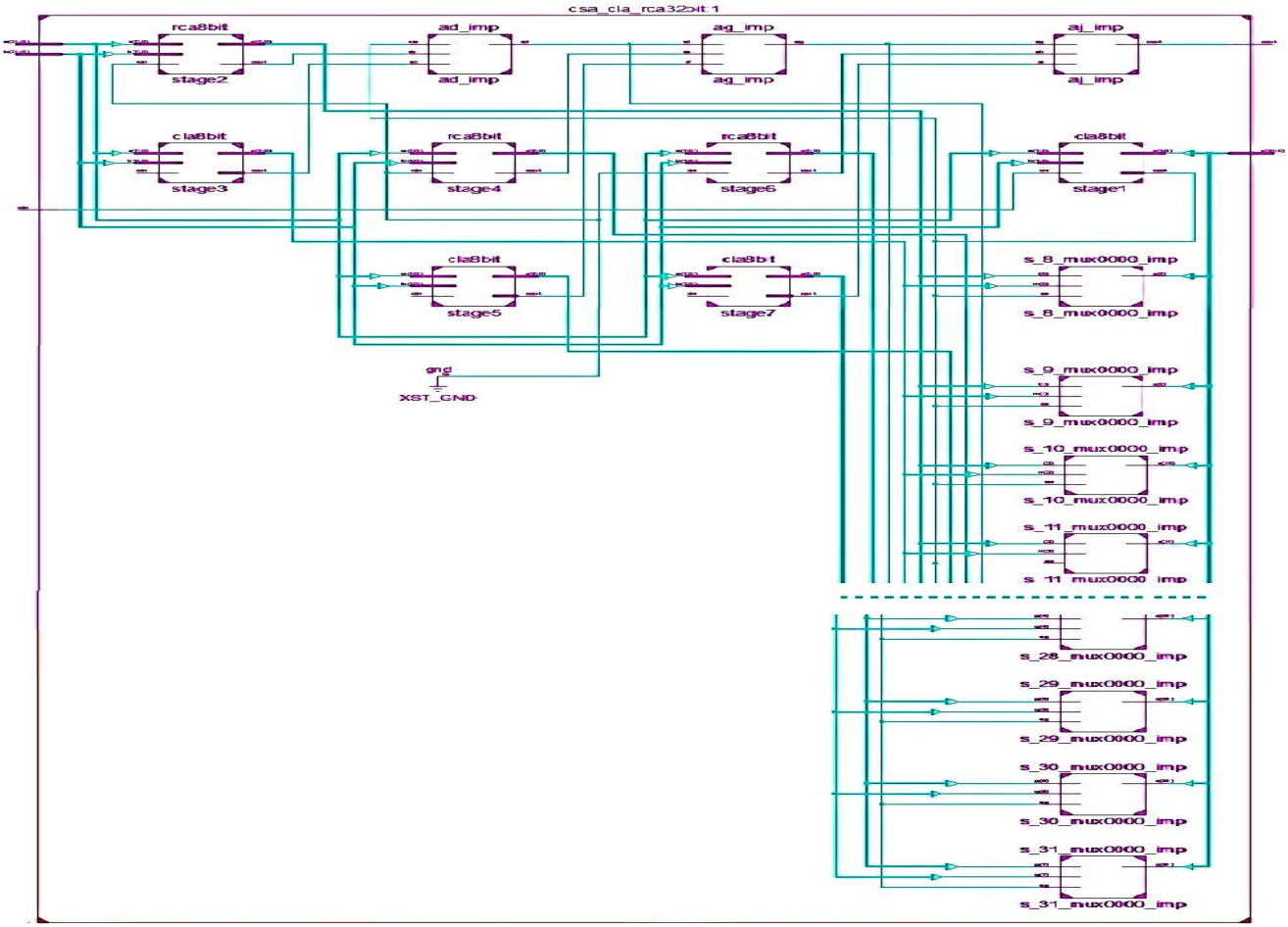

Figure 10: RTL Viewer of 32-bit CSA_CLA_RCA

V. RESULT & SIMULATION

The parallel hybrid adder is designed for 32 bits and this is simulated using Xilinx tool. The figure below shows the simulation result of the proposed 32 bit hybrid adder. The simulation result of 32 bit hybrid adder is given in the Figure 11. The inputs that are given to the adder are a, b and cin. Here both a and b are of 32 bit values each. The signal that is used is 'carry' it is forced with constant values either 0 or 1 and is used for carry generation. With the help of these signals the output sum and cout are produced for the design of 32 bit hybrid adder.

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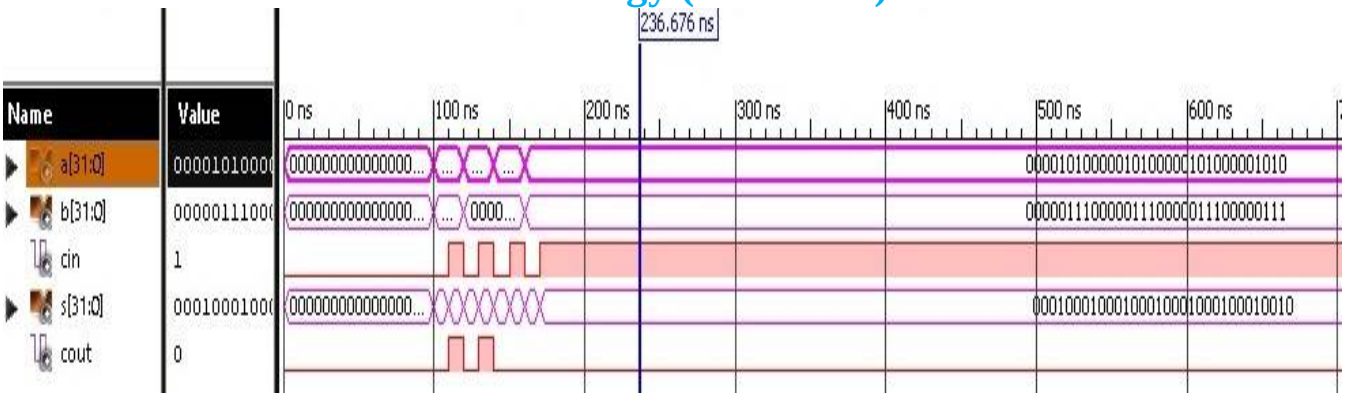

Figure 11: Simulation of 32-bit CSA_CLA_RCA

The maximum combinational path delay is also called, "critical path delay" that encountered by different conventional and heterogeneous CSAs to perform the addition of two 32-bit operands are shown in Tables 1. The optimum delay value is in bold font in the tables. Note that the symbol ∗ signifies the proposed Parallel hybrid adder architecture in the tables. FromTable1, it is evident that the CSA_CLA_RCA hybrid adder based on the 8-8-8-8 input partition features the least propagation delay (20.588ns) amongst all homogeneous and hybrid CSAs, and hence the 8-8-8-8 input partition is deemed to be optimum. The 32-bit RCA has critical path delay of 44.366ns, while the 32-bit CLA adder is found to have the path delay of 44.322ns. Hence it is inferred from Figure 6 and Table1 that for the addition of two input operands having sizes of 32-bits the CSA_CLA_RCA hybrid adder is preferable over all other conventional and heterogeneous CSAs and the favourable input data partition is 8-8-8-8.

Table 1: Maximum propagation delay of 32-bit homogeneous and heterogeneous CSAs corresponding to diverse input partitions

Input Partition	Type of adder Architecture	Propagation delay (ns)
Not Applicable	RCA	44.366
Not Applicable	CLA	44.322
4-4-4-4-4-4-4-4	CSA_RCA	28.507
	CSA_CLA	28.358
	CSA_CLA_CSA*	23.446
8-8-8-8	CSA_RCA	21.311
	CSA_CLA	21.363
	CSA_CLA_CSA*	**20.588**
16-16	CSA_RCA	27.149
	CSA_CLA	26.380
	CSA_CLA_CSA*	26.380

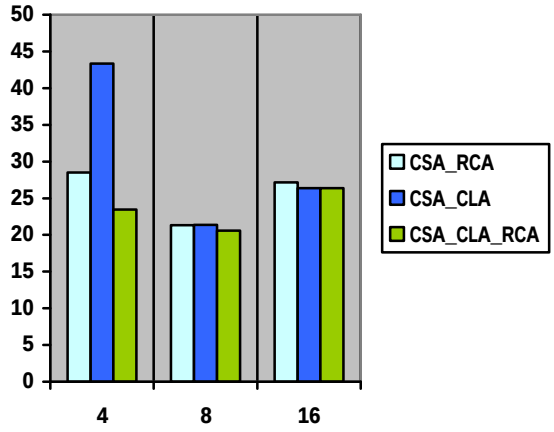

Chart 1: Capturing worst-case delay variations of 32-bit homogeneous and heterogeneous CSAs for different input partitions.
(X-axis: CSA type; Y-axis: Delay in ns.)

32-bit conventional and hybrid CSAs corresponding to various architectures were described topologically in VHDL and were subsequently synthesized by targeting a 90nm FPGA (Spartan-3E: XC3S1600E). The maximum combinational path delay has been estimated after automated place and route and is ascertained from the design summary. The critical path timing and area results (in terms of number of LUTs) of different adder structures are mentioned in Table 2.

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Table 2: Maximum propagation delay and area of 32-bit various designed adders

Parameters	RCA	CLA	CSA_ RCA	CSA_ CLA	CSA_ CLA_ RCA
Propagation Delay (ns)	44.366	44.322	21.311	21.363	**20.588**
No. of 4-inputs LUTs	64	64	103	103	**104**
No. of Bonded IOBs	98	98	98	98	**98**
No. of Slices	37	37	56	56	**57**

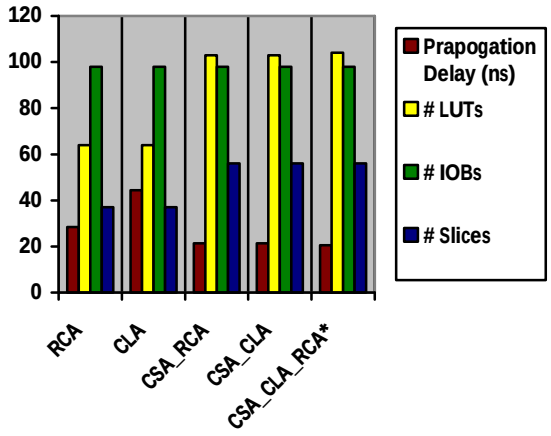


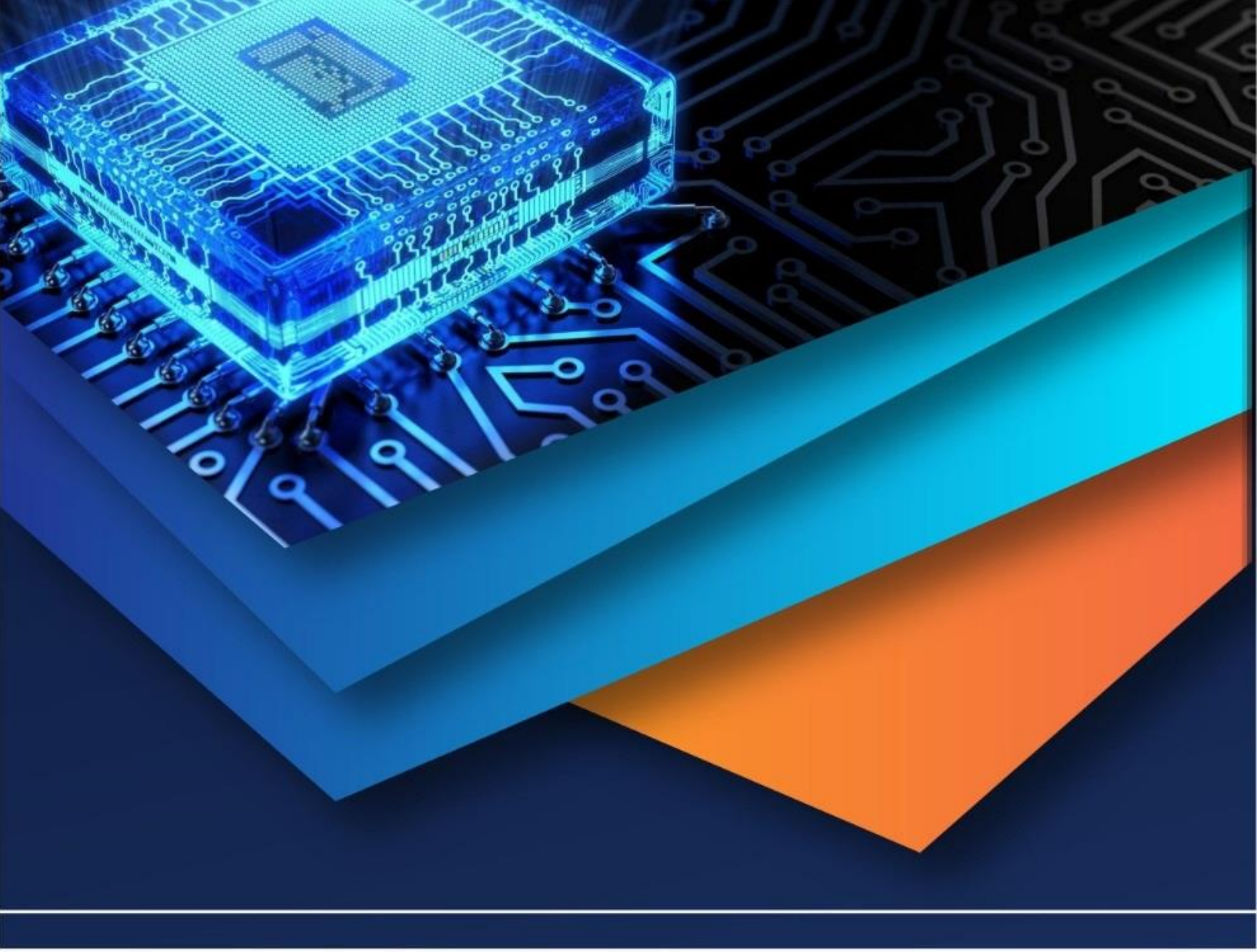
Chart 2: Capturing Maximum propagation delay and area of 32-bit various designed adders (X-axis: Adder type; Y-axis: Various Parameters)

VI. CONCLUSION

It can be concluded that 32-bit Parallel Hybrid Adder is better in all respect like speed, delay, area. Further the work can be extended for optimization of said adder to improve the area. An improvement in addition speed by using new techniques can greatly improve system performance. This project can be extended for the reconfigurable architecture.

REFERENCES

[1] Padma Devi, et. al, "Improved Carry Select Adder with Reduced Area and Low Power Consumption," in International Journal of Computer Applications, Volume 3 – No.4, June 2010.
[2] Shivani Parmar, Kirat Pal Singh, "Design of high speed hybrid carry select adder", in IEEE 3rd International Advance Computing Conference, 2013.
[3] V. Kokilavani, K. Preethi, and P. Balasubramanian, "FPGA-Based Synthesis of High-Speed Hybrid Carry Select Adders", in Hindawi Publishing Corporation, Advances in Electronics, Volume 2015.
[4] K. Preethi, P. Balasubramanian, "FPGA Implementation of Synchronous Section-Carry Based Carry Look-ahead Adders", in IEEE 2nd International Conference on Devices, Circuits and Systems, 2014.
[5] Sajesh Kumar, Mohamed Salih K, "Efficient Carry Select Adder Design for FPGA Implementation", in Elsevier Procedia Engineering, vol. 30, pp. 449–456, 2012.
[6] V. Kokilavani, P. Balasubramanian, and H. R. Arabnia, "FPGA realization of hybrid carry select-cum-section-carry based carry Lookahead adders," in Proceedings of the 12th International Conference on Embedded Systems and Applications(ICESA), pp. 81–85,2014.
[7] Basant Kumar Mohanty, Sujit Kumar Patel, "Area–Delay–Power Efficient Carry-Select Adder", in IEEE Transactions On Circuits And Systems- II: Express Briefs, Vol. 61, No. 6, June 2014.
[8] B. Ramkumar and Harish M Kittur "Low-Power and Area-Efficient Carry Select Adder" IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 20, No. 2, February 2012
[9] P. Vijayalakakshami, N. Kirthika, "Design of hybrid adder using QCA with implementation of Wallace tree multiplier", International journal of advance in engineering & technology, May 2012 vol. 3, issue 2, pp. 202-21
[10] Vaibhav V. Deshmukh, Dr. Nitiket N. Mhala, "Review on: Design of 32-bit Parallel Hybrid Adder," in Proceedings of the International Conference on Quality Up-gradation in Engineering, Science & Technology (ICQUEST-2016).



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