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Design and Analyze a Low Phase Noise LC VCO Using PMOS Varactor for ISM Band

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Abstract— The explosive growth of short range wireless communication systems has lead to highly demand of compact radio frequency (RF) circuit with low power design. As voltage control oscillator (VCO) is the core block of RF systems. Phase Noise performance of LC VCOs is strongly dependent on the Quality Factor of the Inductors. The proposed VCO is designed with the staking switch two series transistors using current reuse topology and inversion-mode of PMOS varactor tank. As known, low cost CMOS technologies, the on-chip inductors have low quality factors compared to external inductors. But, using external inductors connected by traditional bonding technologies limits the integration capacity. In this work we have implemented LC-VCO with PMOS varactor, is demonstrating an improved phase noise performance. The LC-VCO is implemented in 0.13μm CMOS technology operating at 2.4GHz ISM band. The phase noise obtained @ 1MHz offset -113.4dBc/Hz. VCO design techniques and design trade-offs are highlights in this work.

Keywords— CMOS; low power; PMOS; varactor; voltage control oscillator (VCO).

I. INTRODUCTION

In RFIC receivers the LC Voltage Controlled Oscillators (VCOs) are used as local oscillators to down convert signals. Many techniques have been developed to improve the phase noise performance of integrated LC VCOs [1-5]. Despite of these efforts, the quality factor of the inductors (QL) is commonly the main limitation to achieve better results in low cost CMOS technologies.

The short range wireless communications in the area of wireless sensor network, medical implant device and so on are rapidly increasing [6,7]. In this area, the more and more optimized (in terms of low power, low cost, and small size) radio frequency (RF) transceiver system is ever pushing demand. Recently, this demand has been paying much attention in the research work to more optimize the RF transceiver system. Depending on the application, most of the cases the betterment of the power and size is very critical issue in different blocks. Reducing the power of VCO, the key building block of transceiver is here by the main issue. Designing of VCO is trade-offs among the several vital parameters such as power consumption, phase noise, and chip area [8], [10-12]. In the open literature a lot of VCO was reported where the current reuse and other techniques are used. A low power CMOS current reuse VCO is reported in [9] which consume 3.96mW DC power including buffer. Using Flip Chip technology results the better spectral purity in [13] but the power consumption still remain 10.8 mW. On the other hand, in order to reduce the power consumption the staking VCO and Tripler with current reuse technique is used in [14] and reached the power consumption 9 mW as well as the wide frequency tuning range from 7.06 to 8.33 GHz. Therefore, the goal of this work is designing a VCO with optimum power consumption, spectral purity, and increasing the simplicity by reducing the number of circuit components for a low power short range miniaturized RF transceiver system.

Section II presents the basic concepts about NMOS and PMOS complementary cross-coupled LC oscillator topology. In Section III, the VCOs design methodology is shown. The simulation results of the designed circuits and their comparisons are presented in Section IV. Finally, in Section V are drawn some conclusions.

II. BASIC CONCEPT

The cross-coupled transistor topology is used as the design topology for several reasons. For the NMOS and PMOS complementary topology (Fig.1.), power consumption is lower and the oscillation amplitude is a factor of two larger than that of the NMOS only or PMOS only topologies because the bias current is reused. This results in a better phase noise performance for a given bias current. This topology is useable where enough supply voltage range exists for stacking the transistors [15].

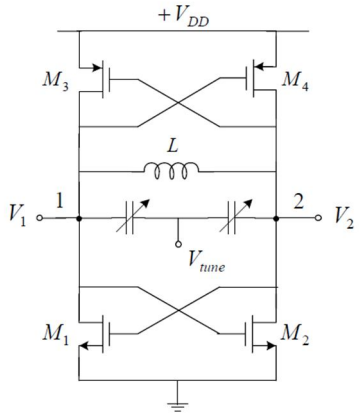

Fig. 1. General LC VCO architecture

Phase noise (PN) is a very important parameter to RFIC's. A linear time invariant model to characterize the phase noise was presented by Lesson [16]. The phase noise predicted by this model is expressed as (1):

$$L(\Delta\omega) = \{\frac{2FKT}{P_S}[1 + \left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2](1 + \frac{\omega_{\frac{1}{f^3}}}{|\Delta\omega|})\} \quad (1)$$

Where F is an empirical device excess noise factor, K is the Boltzmann's constant, T is the absolute temperature, Ps is the average power dissipated in the tank, QL is the loaded quality factor of the tank, Δω is the offset from the carrier frequency ω_0, and ω_{1/f^3} is the corner frequency between $1/f^3$ and $1/f^2$ regions as shown in Fig. 2.

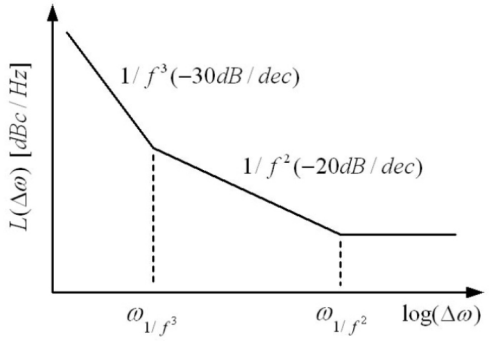

Fig. 2. Phase noise

Analyzing (1), it is possible to observe the influence of the series resistance (Rs) and inductance (Ls) of the inductor inside the $Q_L(Q_L = \omega_0 L_S/R_S)$ and the output amplitude (VA) in PS parameter ($P_S = V_A{}^2/R_P$, where R_P is the parallel resistance of the LC tank approximately $\omega_0{}^2 L_S{}^2/R_P$). VA increases when the bias current increases. So, there is a trade-off between the phase noise performance, power consumption and the quality factor of the inductors.

III. VCO DESIGN METHODOLOGY

The cross-coupled LC VCO in CMOS has attracted considerable interest due to its easy start-up and good phase noise characteristics [5]. The circuit schematic of the proposed CMOS LC-VCO with complementary cross-coupled transistors around an LC-tank is shown in Figure 1. It uses a dual cross-coupled technique and the same bias current flows through both pMOS and nMOS devices. The advantage of using both pMOS and nMOS cross-coupled transistors is mainly three-fold; first, to start up the oscillation easily, second, to well compensate the loss from the LC tank, and active devices with less current consumption saving some power and optimizing the varactors C1, C2 and MOSs size to get enough wide tuning range and keep the phase noise lower around the carrier. The negative resistance -2/gm where gm denotes the transconductance of each transistor generated by cross-coupled pMOS transistors M1 and M2 and nMOS M3 and M4 is designed to compensate for the loss associated with the LC-tank. In order for the oscillation to be sustained, the tail current should be kept to a level for the negative resistance to be smaller in absolute value than the

equivalent loss of the tank and to suppress the flicker noise and thermal noise. Accumulation-mode MOS varactors for tuning the VCO output frequency are realized using high-Q MOS transistors with reverse-biased pn junction parallel to the inductor to form the complementary cross-coupled LC oscillator.

The proposed VCO is shown in figure 3. This topology uses NMOS and PMOS switching transistor in series like stacking opposite side of the tank circuit. The MOS switching transistors are cross connected to each other and generate the sufficient negative resistance which also eliminates one of the cross connected MOS pairs from the conventional topology (fig.3.).

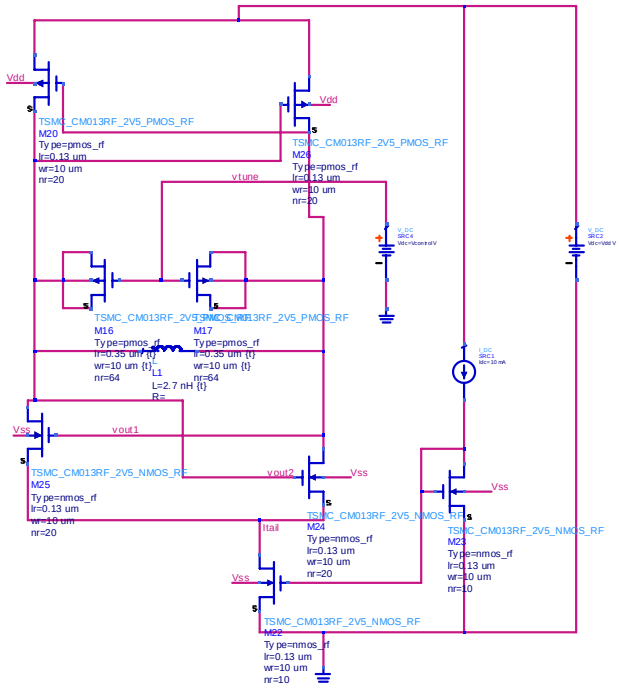

Fig. 3. Designed LC VCO

The proposed current reusing LC VCO is shown in figure 3.This topology uses NMOS and PMOS switching transistor in series like stacking opposite side of the tank circuit. The MOS switching transistors are cross connected to each other and generate the sufficient negative resistance which also eliminates one of the cross connected MOS pairs from the conventional topology figure 1. In regard of phase noise degradation, the PMOS transistor is always preferable due to having the lower 1/f noise than the NMOS transistor [5]. On the other hand, among the different choice of varactor, PMOS varactor is preferred to be implemented in VCO resonator in order to achieve lower phase noise [6]. The tank circuit is optimized with 2.7 nH inductor and the PMOS (PM2 and PM3) varactor with 1.56pf capacitance to make sure the oscillation at the frequency around 2.45 GHz and the best spectral purity. The current in the tank circuit is controlled by the Crossed coupled PMOS and NMOS staking switch which affect the tank performance and amplitude of the output voltage.

The general VCO architecture is shown in figure 1. PMOS M1-M2 and NMOS M3-M4 form VCO core generating negative impedance. The standard passive on chip spiral inductor L and two PMOS as a capacitor varactors form the frequency tuning network. Vctrl is the control voltage of the VCO. The proposed VCO architecture is shown in figure 2. PMOS M1-M2 form VCO core generating negative impedance.

$$\omega_{OSC} = \sqrt{\frac{1}{LC}} \quad (2)$$

Among the several different topologies for the compensation of tank loss in oscillator, the cross couple differential or –Gm LC VCO topology is the common choice for radio frequency integrated circuit (RFIC) in order to get better spectral purity and frequency stability. The spectral purity/phase noise is very important parameter in oscillator performance that mostly depends upon the quality factor (QF) of the tank circuit that used in oscillator. Hence the perfect designing of tank circuit results the better phase noise

performance of VCO. It is vary usual that the C of the LC tank VCO is implemented by the varactor and the part of the C value is varied by the control voltage. The series resistance of varactor has an imperious effect on overall tank quality factor. In this regard, the diode varactor can enable voltage dependent frequency variation but in terms of tank QF, the MOS varactor is better for its lower gate resistance that result superior tank QF.

On the other hand the proper setting of Gm value of switching cross couple NMOS or/and PMOS transistor according to the tank impedance let the circuit oscillate. LC tank has values of total capacitance produced by PMOS Varactor is 1.56pf and inductor L=2.7nH.

IV. SIMULATION RESULTS AND MEASURMENT

LC VCO designed and simulated using Agilent's Advance Design System (ADS). It is the most powerful design tool for RF design. We have performed Transient analysis, DC simulation, AC simulation, Phase noise simulation and HB simulation.

The VCO starts oscillating at$I_D = 4.17mA$. The VCO is tuned by a differential voltage$V_{control}$, applied by two voltage sources$V_{DD} \pm V_{control}/2$.

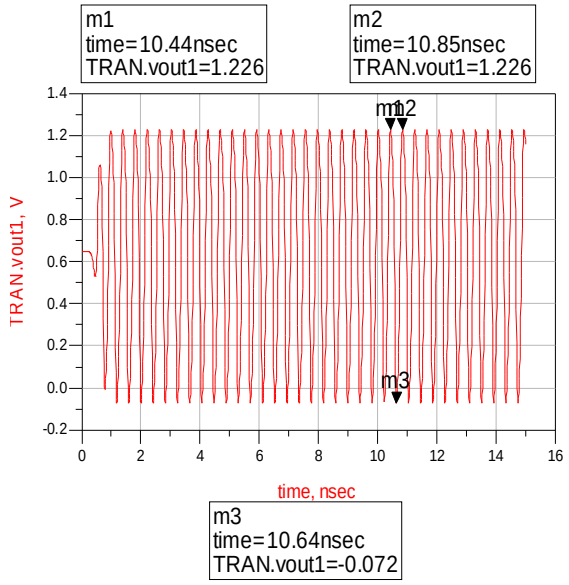

Fig. 4. Single ended transient response of vout1.

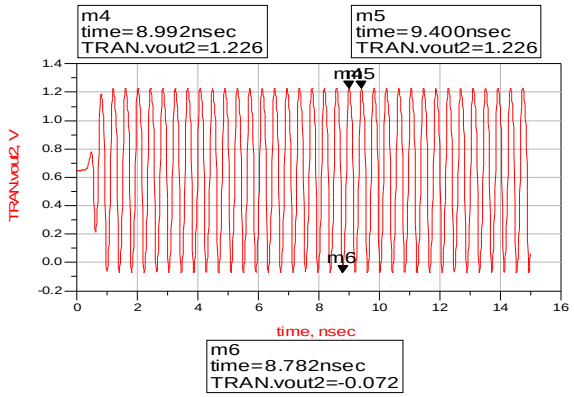

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Fig. 5. Single ended transient response of vout2.

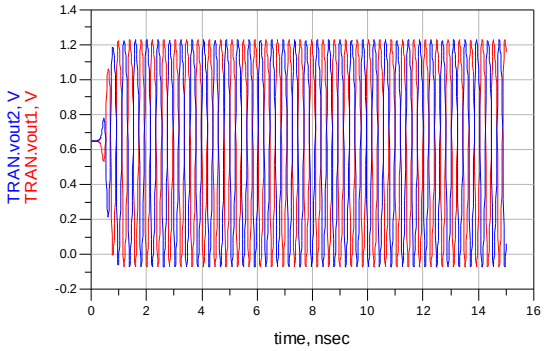

Fig. 6. Differential transient response of LC VCO.

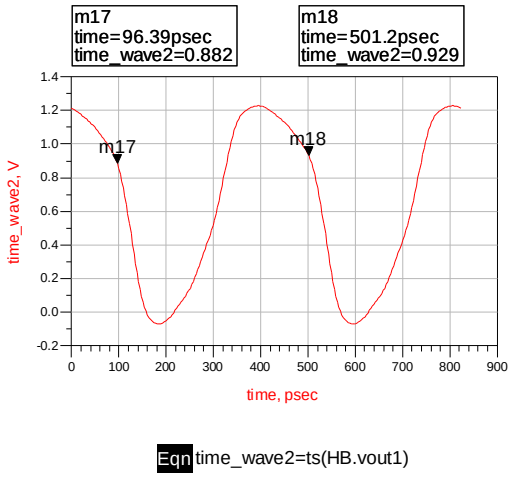

Fig. 7. HB analysis response of LC VCO

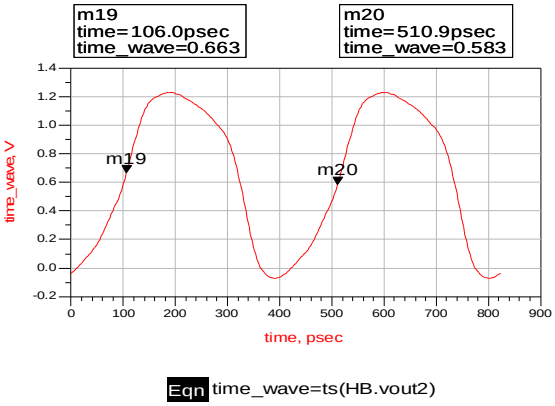

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Fig. 8. HB analysis response of LC VCO

Frequency calculation is as follows,

$$F = \frac{1}{T_2 - T_1} = \frac{1}{510.9psec - 106psec} = 2.45GHz$$

Output Voltage,

$$V_{out} = V_1 - V_2 = 1.226V - (-0.072V) = 1.298V$$

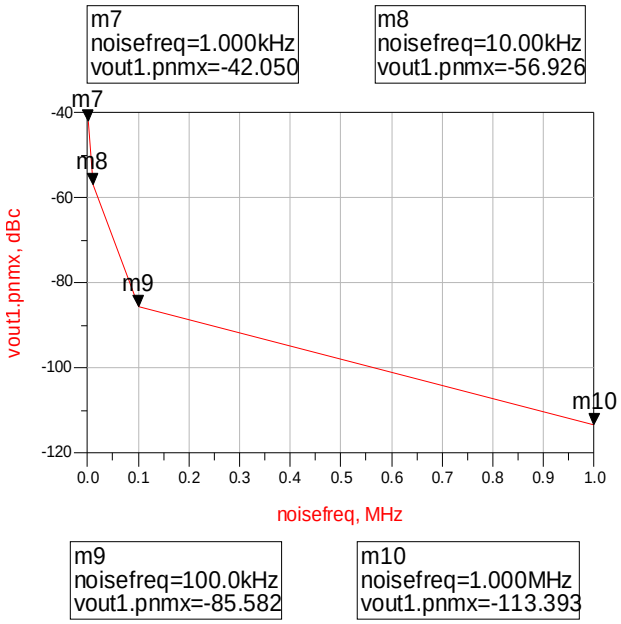

Fig. 9. Phase noise response of LC VCO

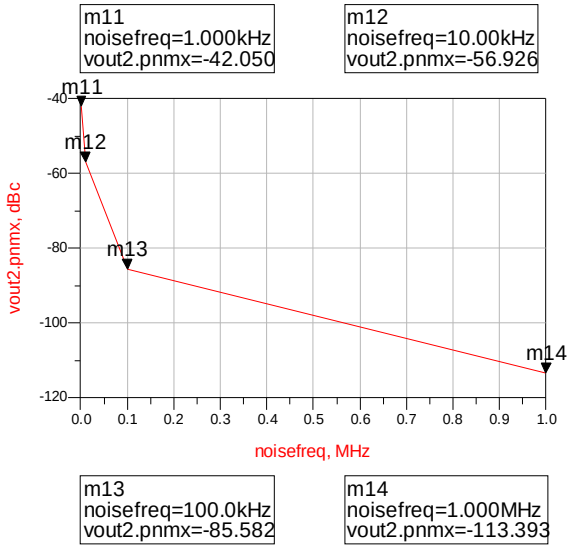

Fig. 10. Phase noise response of LC VCO

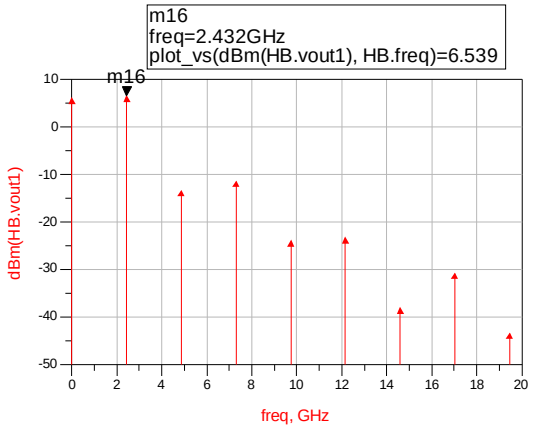

Fig. 11. Frequency Spectrum at Vtune = 0.6V

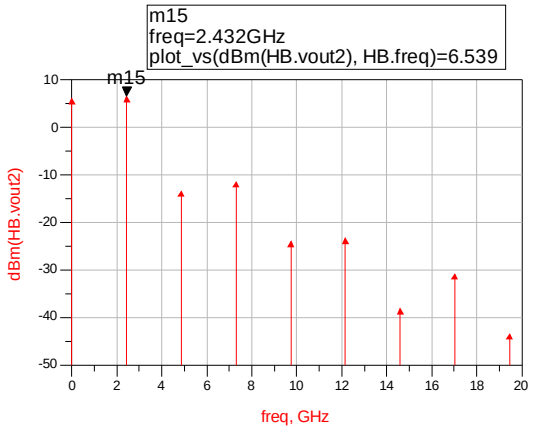

Fig. 12. Frequency Spectrum at Vtune = 0.6V

Fig.7 and fig.8 Shows the measured phase noise spectrum of the VCO for center frequency of 2.45 GHz. Phase noise at the frequency offset of 1MHz away from the carrier is-113.4 dBc/Hz. Fig.4.-fig.7 shows the measured spectrum of the VCO's output with frequency being at 2.45GHz. Summary of the VCO performances is given in Table1.

TABLE I. SPECIFICATION

Sr. No.	Specifications	Parameter Value
1	Technology	130nm
2	Supply Voltage	1.2V
3	Operating Current	4.17mA
4	Frequency	2.45GHz
5	Phase noise @1MHz offset	-113.4dBc/Hz

V. CONCLUSION

A fully integrated CMOS differential 2.45GHz LC VCO used for ISM band in a commercial 0.13µm RF CMOS process has been presented. The whole VCO consumes less than 4.17mA current at 1.2 V supply voltage and with phase noise of -113.4dBc/Hz@ 3MHz offset frequency.

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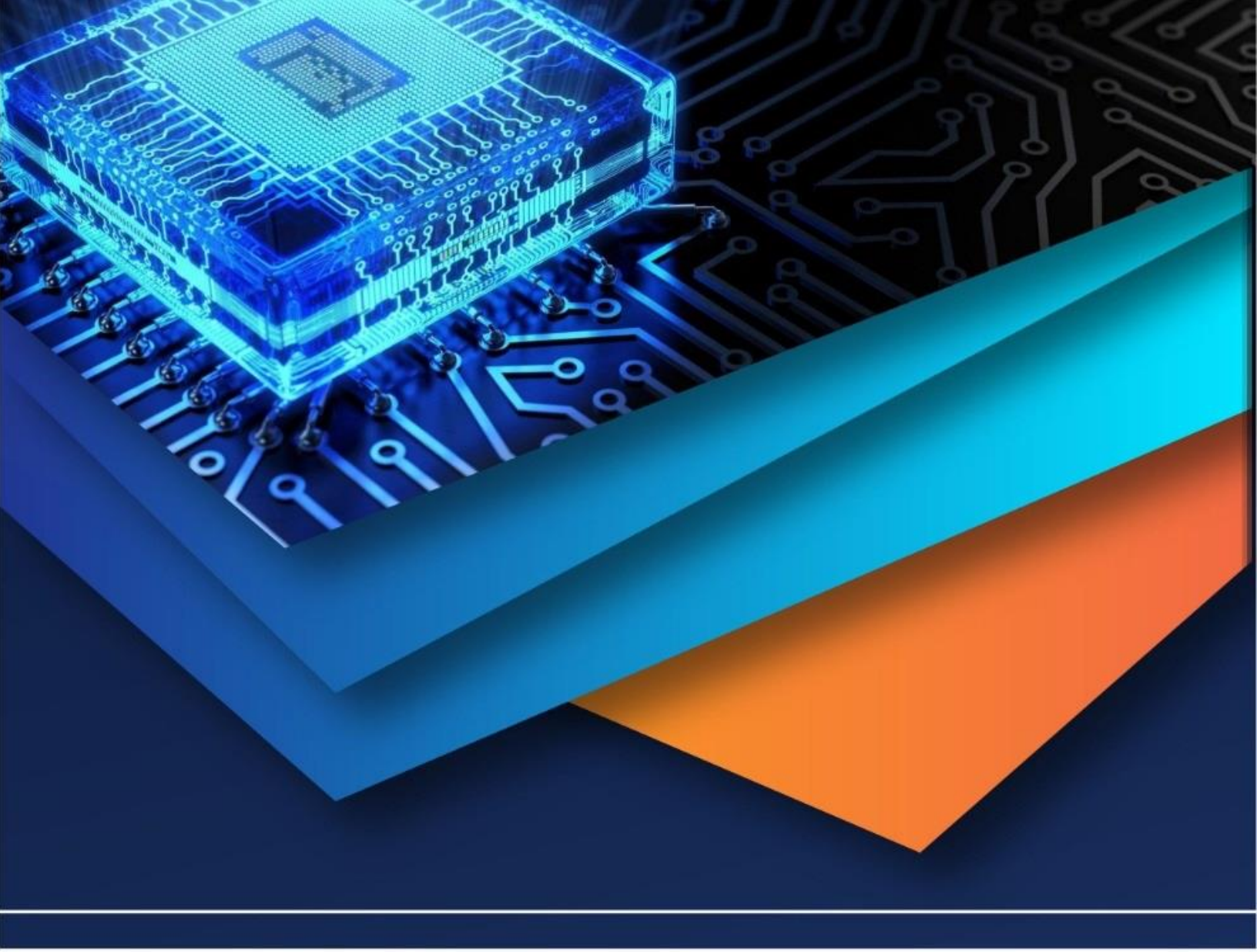

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