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Design & Analysis of 5th Order DC-DC Converter

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Abstract- A new two-input DC-DC converter suitable to draw power from two different dc sources feeding a common dc-bus is presented in this paper. This is a two-switch converter belongs to fifth-order family and performs bucking operation for one dc source while it allows both bucking as well as boosting feature with the second source. The salient feature of the proposed converter is that both the sources either individually or simultaneously supply power to the downstream load at reduced ripple current. This feature is particularly attractive for photovoltaic power processing applications. A digital voltage-mode controller is designed for downstream dc-bus regulation while the current controller regulates the power from the weak input power source. A 24 V, 100 Watt converter performance is analyzed and compared with the simulation observations.

I. INTRODUCTION

Switch-mode power converters application in the dc power distribution is increasing in the recent years. Particularly in the area of automotive systems the main focus is on hybrid vehicles. As the power conversion system is becoming miniaturized, increasing the power density is one of the challenging issues for the power supply designers. One of the main orientations in power electronics in the last decade has been the development of switching-mode converters with higher power density and low electromagnetic interference. Light weight, small size and high power density are also some of the key design parameters [1]-[3]. Several different types of switch-mode dc-dc converters, belongs to buck, boost and buck-boost topologies, have been developed and reported in the literature to meet variety of applications. Major concern in the recent dc distribution systems, such as in automotive and telecom power supply systems, is to meet the increased power demand and reducing the load on the primary energy source, i.e. built-in battery. This is possible by adding additional power sources in parallel to the existing battery source. The additional power sources can be: (i) renewable energy sources such as photovoltaic (PV) or wind, (ii) fuel cell storage power. Power sources supplementing other resources are normally categorized as hybrid power source and the corresponding scheme is called hybrid distributed generation systems.

Integration of renewable energy sources to form a distributed generation system is a viable option for the hybrid vehicles, automotive industries and even in remote stand-alone power supply system. In order to efficiently and economically utilize renewable energy resources it is necessary to tap the energy as and when it is available and then store for subsequent utilization. Nowadays, electric double layer capacitors are coming up in the energy storage systems in addition to the conventional battery systems. However, in all these cases the power conversion efficiency and it's control is major challenge for the power supply designer. The efficiency improvement with higher power density, from the steady-state point of view, of the distributed energy generation is one of the considerations for the designer. The other constraint while designing such system is to evolve simple and reliable power control strategy.

To address some of the above issues, multi-input converters, with different topology combinations, are evolving. Although several power conversion topology configurations can easily be developed, but an integrated converter with bucking, buck-boost feature is desired in most of these schemes. To this affect, there is not enough literature covering the development of converter and control schemes for such applications. Furthermore, literature covering design aspects of digital controllers for such kinds of converters is also limited. In order to bridge this gap, a new two-input dc-dc converter is proposed in this paper and then digital controllers have been designed to ensure dc-bus voltage regulation together with power distribution control of the input dc power sources.

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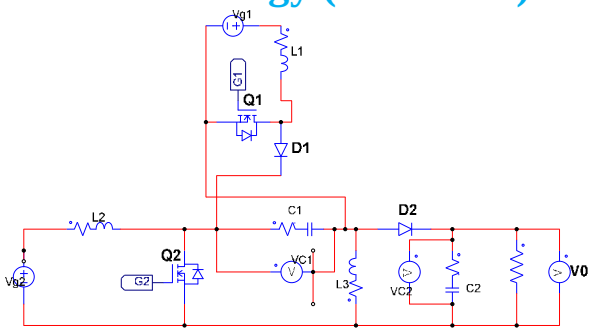

Fig. 1. Two-input dc-dc converter circuit diagram.

Several compensator design approaches have been reported in the literature for Op-Amp or IC based analogue controllers. However, in the case of digital controller design, two main approaches are widely used, that is: (i) digital redesign method (DRM), (ii) direct digital design method (DDDM). In the first case, the compensator is designed in the conventional way by using s-domain transfer functions together with linear system theory and the resulting compensator is transformed into the digital domain using appropriate z-transformations. On the other hand, in DDDM, the compensator design is carried out in the z-domain itself and hence there is no need for s -to- z-domain transformation. In view of these features here DDDM is used for the robust digital controller design.

II. MODELING OF TWO-INPUT DC-DC CONVERTER

The proposed two-input dc-dc converter, shown in Fig. 1, has two switching devices, five energy storage elements and hence it forms a fifth-order system. In the power conversion process it performs bucking operation for one dc source, buck-boost conversion for the second source. It has the following salient features (a) both the dc sources are supplying continuous currents and hence their ripple current is low, (b) lesser filtering requirement on the input side, (c) automatic load transfer on to the first dc source if the second dc source capacity, weak source with limited power supplying capacity, is less than the load demand, and (d) simple control strategy, with or without overlap of duty ratio signals, as there are only two switching devices need to be controlled.

The circuit can operate either in continuous or discontinuous inductor current mode. But, the proposed converter is mainly for higher load power requirement, where one dc source unable to meet the complete load demands and hence the inductor currents are almost all the times are continuous. In view of this the converter is analyzed here for continuous current mode of operation. Here the circuit operation also depends on the type of controlling signal used for switching devices S_1 and S_2, and the two switching devices, (S_1 and S_2), can be synchronized either with trailing-edge or leading edge operation. Each of these schemes has their own advantages and limitations and detailed discussion on the suitability and application requirements will be discussed in the final paper. Furthermore, depending on the load demand and available power with each dc source three different cases will arise, which are: (i) $d_1 > d_2$, (ii) $d_1 < d_2$, (iii) $d_1 = d_2$. In the first two cases the circuit undergoes three different structural changes, while in the last case only two different operating modes in one switching cycle. In this paper the $d_1 > d_2$ case is analyzed for the trailing-edge synchronized switching signals. Applying volt-sec balance to inductors gives the voltage conversion ratio of this converter as $V_o = V_1 d_1 + V_2 d_2 / (1 - d_2)$. From this equation it is clear that the load voltage is controlled by the both the switch duty ratio signals and also depends on both input dc sources. The analysis of the remaining two different cases is quite similar to one presented in this paper. For $d_1 > d_2$ case the switching sequence in one switching cycle is: (i) mode-1: S_1 and S_2 both ON, (ii) mode-2: S_1-ON and S_2-OFF, (iii) mode-3: Diode- ON. In each mode of operation the power stage dynamics can easily be described by a set of state equations given by:

$$\dot{x} = A_K x + B_K u$$
$$v_0 = C_k x \qquad (1)$$

where $[x] = [i_1 \quad i_2 \quad i_3 \quad v_{c1} \quad v_{c2} \quad v_{c3}]^T$, $[u] = [V_{g1} \quad V_{g2}]^T$, and k=1,2,3 for mode-1, mode-2 and 3, respectively. Details of various matrices will be given in the final paper. The small-signal discrete-time model [13] can be written as:

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$$\hat{x}[n]=\phi\hat{x}[n-1]+\gamma\hat{d}[n-1] \quad (2)$$

The output state-space equation can be written as follows:

$$\hat{y}[n]=C_i\hat{x}[n]. \quad (3)$$

In dc-dc converters two different pulse-width-modulations schemes are widely used, which are: trailing-edge and leading edge-modulations. In this paper, trailing-edge OFF-time sampling with a sampling frequency $f_s(=1/T_s)$, as shown in Fig. 2, is implemented and its detailed mathematical analysis is discussed in the following paragraphs. From Fig. 2 over interval-1: $(n\text{-}1)T_s < t < [(n\text{-}1)T_s + t_d - d_2T_s]$, the system state equation can easily be written as

$$\dot{x}=A_3x \quad (4)$$

Assuming the source voltage is almost constant during each mode of operation of the switching cycle, the discrete-time model with state 'x[(n-1)T_s]' at the beginning [5] and duty ratio 'd' can easily be defined by

$$x[(n\text{-}1)T_s+t_d-d_2T_s]=e^{A_3(t_d-d_2T_s)}x[(n-1)T_s] \quad (5)$$

Along similar lines, the discrete-time models for the remaining time intervals are established as

Iinterval-2: $[(n\text{-}1)T_s+t_d-d_2T_s] < t < [(n\text{-}1)T_s+t_d]$,

$$x[(n\text{-}1)T_s+t_d]=e^{A_1[d_2T_s]}e^{A_3(t_d-d_2T_s)}x[(n-1)T_s+t_d-d_2T_s] \quad (6)$$

Interval-3: $[(n\text{-}1)T_s+t_d] < t < [(n\text{-}1)T_s+t_d+(d_1T_s-d_2T_s)]$

$$\begin{aligned}&x[(n\text{-}1)Ts+td+(d_1T_s-d_2T_s)]\\&=e^{A_2[d_1T_s-d_2T_s]}e^{A_1d_2T_s}e^{A_3(t_d-d_2T_s)}x[(n-1)T_s]+K_2T_se^{A_2T_s[d_1-d_2]}\hat{d}_2\end{aligned} \quad (7)$$

Interval 4: $[(n\text{-}1)T_s+t_d+(d_1T_s-d_2T_s)] < t < [nT_s]$

$$\begin{aligned}x[nT_s]&=e^{A_3[T_s-d_1T_s-t_d+d_2T_s]}e^{A_3[t_d-d_2T_s]}e^{A_2T_s(d_1-d_2)}e^{A_1d_2T_s}x[(n-1)T_s]\\&\quad+K_2T_se^{A_3[T_s-d_1T_s-t_d+d_2T_s]}e^{A_2T_s[d_1-d_2]}\hat{d}_2+K_1T_se^{A_3[T_s-d_1T_s-t_d+d_2T_s]}\hat{d}_1\end{aligned} \quad (8)$$

The small-signal discrete-time model in standard form for the converter under discussion can be written as:

$$\hat{x}[nT_s]=\phi\hat{x}[(n-1)T_s]+\gamma_2\hat{d}_2[(n-1)T_s]+\gamma_1\hat{d}_1[(n-1)T_s] \quad (9)$$

Comparing eqns. (8) & (9), it is easy to obtain

$$\phi=e^{AT_s},\ \gamma_1=K_1T_se^{A_3[T_s-d_1T_s-t_d+d_2T_s]},\ \gamma_2=K_2T_se^{A_3[T_s-d_1T_s-t_d+d_2T_s]}e^{A_2T_s[d_1-d_2]},$$

$$K_1=[(A_2-A_3)x+(B_2-B_3)U],\ K_2=[(A_1-A_2)x+(B_1-B_2)U].$$

Taking the z-transform of eqn. (14),

$$x(z)=[zI-\phi]^{-1}[\gamma_1d_1(z)+\gamma_2d_2(z)] \quad (10)$$

Taking the z-transform of equation (8) results in

$$y(z)=E_ix(z) \quad (11)$$

Combining eqns. (9) and (10) results in

$$y(z)=E_i[zI-\phi]^{-1}\gamma_2d_2(z)+E_i[zI-\phi]^{-1}\gamma_1d_1(z). \quad (12)$$

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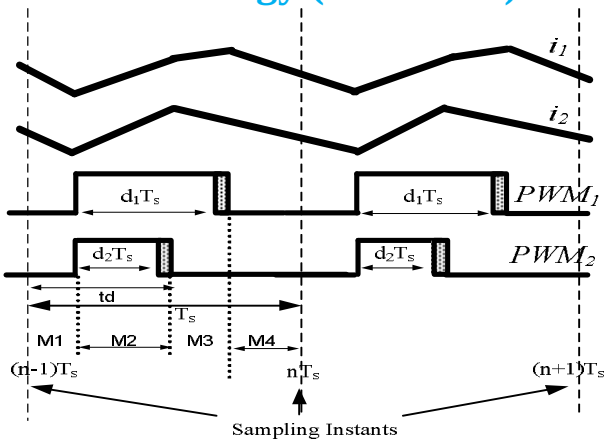

Fig. 2. PWM gating signals and Off-Time sampling process.

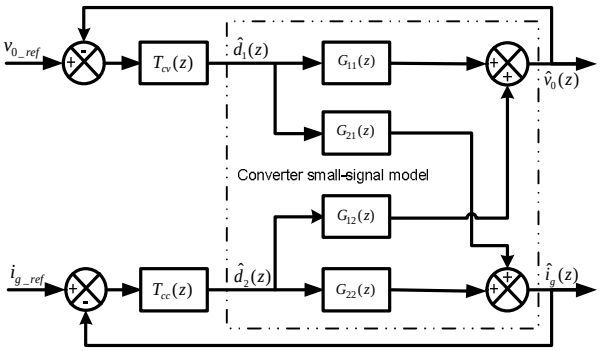

Fig. 3. Block diagram of the closed-loop converter system.

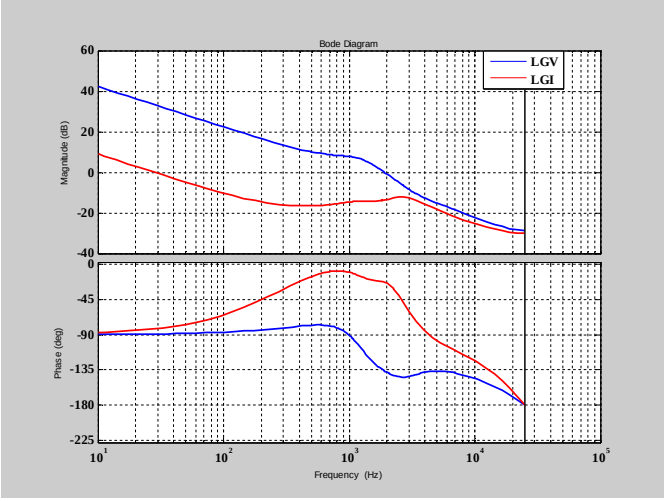

Fig. 4. Bode plots of voltage and current loopgains (LGV: Voltage loop, LGI: Current loop).

A delay greater than T_s, $t_d=(kT_s+t_d')$ can be taken into account by replacing $\hat{d}[n-1]$ with $\hat{d}[n-1-k]$, t_d with t_d', and the corresponding discrete-time model is:

$$x[nT_s]=\phi x[(n-1)T_s]+\gamma_1\hat{d}_2[(n-1-k)T_s] + \gamma_2\hat{d}_1[(n-1-k)T_s] \quad (13)$$

Taking the z-transform of eqn. (13) results in

$$x(z) = z^{-k}\left[zI - \phi\right]^{-1}\gamma_1 d_2(z) + z^{-k}\left[zI - \phi\right]^{-1}\gamma_2 d_1(z) \quad (14)$$

The above equation describes the small-signal dynamics of the proposed converter, with the converter state variables depending on the two control variables, d_1 and d_2. In order to design suitable control strategies based on d_1 and d_2, it is essential to know the degree of interaction between the control loops. Details of control loop interactions using relative gain array theory and loop design aspects will be discussed in the final paper.

III. DIGITAL CONTROLLER DESIGN

Several different types of control strategies are reported in literature, and they are broadly classified into: (i) single-loop voltage-mode, (ii) single-loop current-mode, (iii) two-loop current mode control, and (iv) multi-loop schemes. Although the single-loop strategies are simple to implement, but their dynamic response times are slightly higher side. Although two-loop current-mode schemes are popular in the power supply applications, but their compensator design presents complexity. In this paper two decoupled control scheme are proposed, of which one for dc-bus voltage regulation and the other for load division on second dc source. This structure is capable of maintaining the load voltage regulation while feeding available power from the weak dc source. The control schemes can be interchangeable from one to other depending on the source power supply capacity. However, use of current-control loop for heavier source limits the load supplying capacity and hence it is not recommended. In view of this difficulty it is always recommended to use current-control loop for the weaker source and connected to the circuit portion that gives buck-boost feature. DC-bus voltage regulation loop should be closed together with the heavier source. Detailed mathematical treatment will be presented in the final paper to support above discussion. For decoupled digital controllers design two different loopgains have been defined here, one for current-control loop while the second one for the dc-bus voltage regulation loop. The general block diagram for loop design is shown in Fig. 3 where $G_c(z)$: Compensator, F_m: PWM generator transfer function, 'K' is the load voltage sensing gain, and loopgain $T_L(z)=KF_mG_c(z)G_p(z)$. Here, $G_p(z)$ can be either control –to- inductor current transfer function in case of current controller design, or control –to- output voltage transfer function for the voltage regulator design. In any case the digital compensator is designed using sisotool of the MATLAB in the frequency domain. Pole-zero placement technique is used and then final design is arrived. Fine tuning of the compensator is performed to ensure relative stability margins, i.e. gain margin> 6 dB, 35^0<phase margin<75^0 and reasonable crossover frequency, which normally depends on the order of the converter under consideration.

$$G_{ci}(z) = \frac{0.0506(z-0.97)}{(z-1)} \quad (15)$$

$$G_{cv}(z) = \frac{13.502(z-0.8384)(z-0.8326)}{(z-1)(z-0.272)} \quad (16)$$

IV. SIMULATION STUDIES AND EXPERIMENTAL RESULTS

To extract the salient features of the proposed converter and to verify the load distribution together with dc-bus regulation capability a 24 V, 96 *Watt* two-input dc-dc converter system was considered in this studies and its parameters are listed in Table I. PSIM is used for simulation purpose. In these studies DC source-1 considered as heavier source having sufficient power supplying capacity, more than load demand, while DC source-2 considered as weaker source with its power supplying capacity less than the load demand.

For a load demand 96 W, the load distribution pattern on the two input dc sources is shown in Fig. 5. In this simulation it has been kept current limit of 2 A on the dc source-2 and its maximum power delivering capacity is 24 W. In the load demand of 96 W dc-source-1 supplies 72 W, while source-2 supplies 24 W. When the dc source-2 supplying its full rated power then any additional load coming on to the converter is going reflect on dc source-1. To illustrate this feature the load resistance is changed from 6 to 4 Ω and the corresponding results are shown in Fig. 6. It is clear from the simulation results that load voltage is almost constant and the additional load demand is transferred on the dc source-1.

The load division control strategy effectiveness is also verified when the source voltages are varying between minimum and maximum values. To emulate this aspect, dc source-2voltage kept at its rated value, while the dc source-1 voltage is gradually varied between 36 and 46 V and the corresponding results are plotted in Fig. 6.

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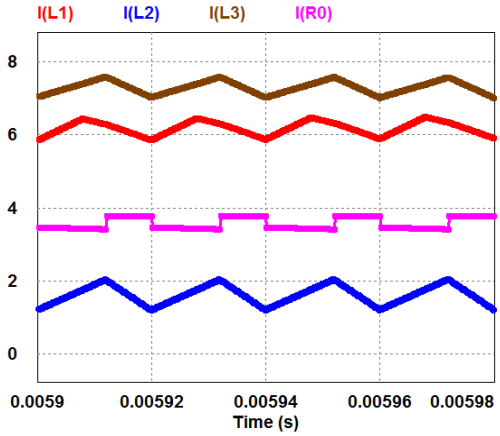

Fig. 5. Steady-state waveforms showing load division on the two input dc sources.

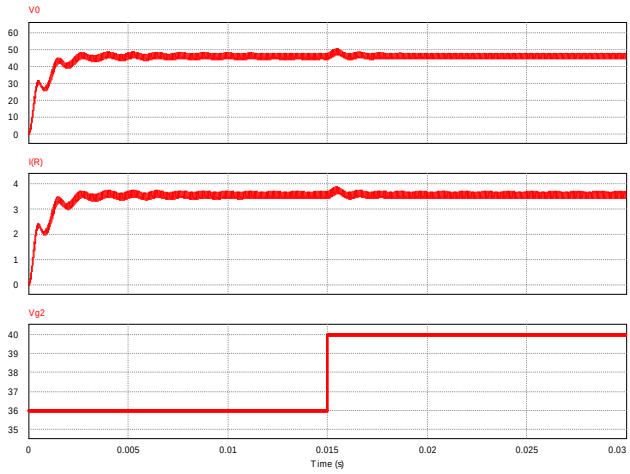

Fig. 6.Dynamic response of load voltage against gradual variation of source voltage (V_1: 36 → 46 V).

V. CONCLUSION

A new two-input DC-DC converter suitable for drawing power from two different dc sources and feeding to common dc bus was proposed in this paper. Modes of operations have been analyzed and then decoupled control-loops were designed to distribute the load demand on both the input sources. Voltage-mode control strategy was used to ensure dc bus voltage regulation, while current-control loop was implemented to restrict the load division on the second source. Simulation and experimental results were in agreement with the theoretical predictions. Detailed comparison of simulation and experimental results for different conditions will be given in the final paper.

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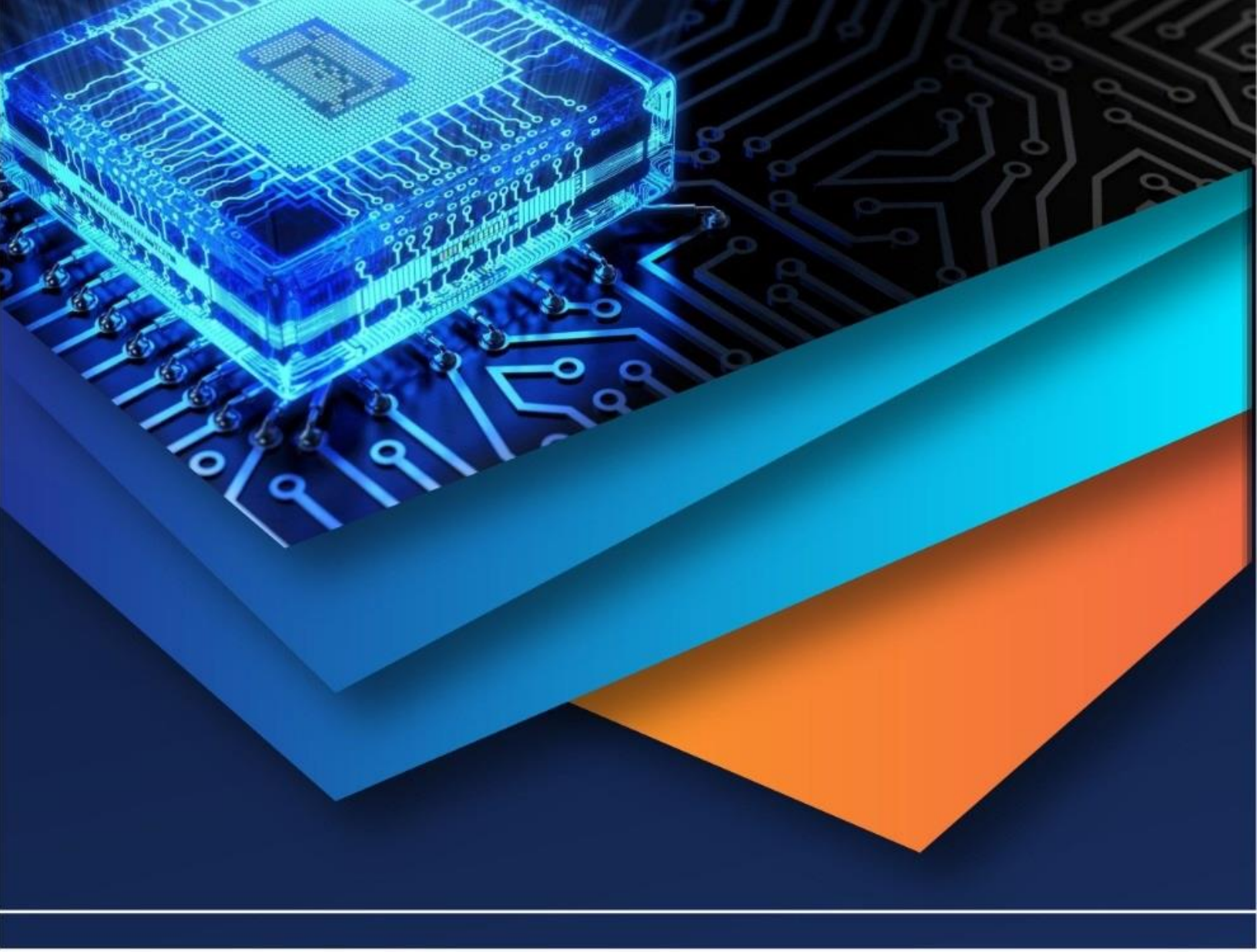

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