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A Novel Full-Bridge PWM Dc–Dc Converter with Energy Recovery Turn-Off Snubber

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Abstract— This paper presents a full bridge pulse-width modulated dc-dc converter with controlled secondary side rectifier using a novel non dissipative energy recovery turn-off snubber, and an innovative control algorithm to achieve soft switching. The circulating current of the converter is eliminated and soft switching for all power switches of the inverter is achieved for full-load range from no-load to short circuit.
Keywords— Controlled output rectifier, dc–dc converter, snubber circuit, soft switching, zero-voltage zero-current switching (ZVZCS).

I. INTRODUCTION

The main and most important part of voltage or current switching power supplies is Dc-Dc converter. For high power, high frequency applications full-bridge pulse-width modulated (PWM) dc–dc converters have been used as they have several advantages and for high output power applications, insulated-gate bipolar transistors (IGBTs) as main switches are predominantly used in the converters. To achieve high efficiency of these converters, it is necessary to reduce switching losses and conduction losses caused by circulating currents. Generally, by choice of converter topology, design of a proper control algorithm, and by using appropriate additional circuits the both mentioned losses can be reduced.

Most of full-bridge dc–dc converters are controlled by phase shifted pulse-width modulation (PS-PWM). However, soft- switching PS-PWM dc–dc converters have some difficulties. Conduction losses of conventional soft switched converter are relatively high during freewheeling period due to the circulating current flowing through the primary and secondary windings of the high-frequency transformer. Moreover, converters need a large commutating current in order to ensure zero-voltage switching (ZVS) operation. Various active or passive, dissipative or nondissipative snubbers, clamps and auxiliary circuits are often added on secondary or primary side of the transformer to ensure soft switching of the main switches and suppression of converter circulating currents [1]–[8].

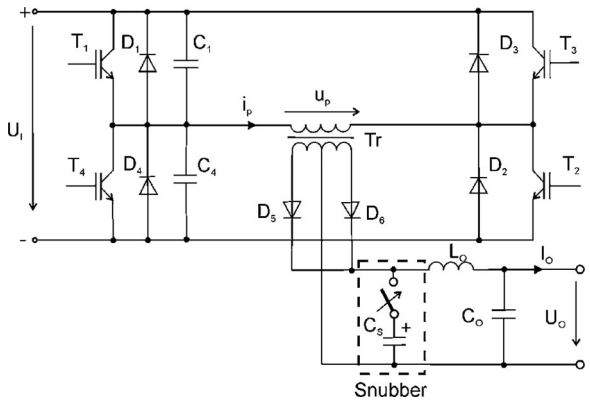


Fig.1: Principle of the ZVZCS PS-PWM converter operation.

In order to rectify high frequency secondary voltage the diode output rectifier is mostly employed on the secondary side of the power transformer. Disconnection of the secondary windings is mostly achieved by application of the reverse bias for the output uncontrolled rectifier (see Fig. 1). Consequently, both primary and secondary currents of the transformer become zero. Afterward, only a low magnetizing current circulates during freewheeling interval. Thus, the RMS current of the transformer and switches are considerably reduced.

The main drawbacks of these PWM and PS-PWM dc–dc converters dwell in the fact that either reduction of the circulating currents

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is insufficient or auxiliary circuits are too complex or control algorithms are overcomplicated. Moreover, soft switching is often achieved only in a relatively narrow range of the load. The other and very effective way, how to decrease circulating currents in the converter and, at the time, to achieve reduction of switching losses, is to utilize a controlled output rectifier [9]–[14].

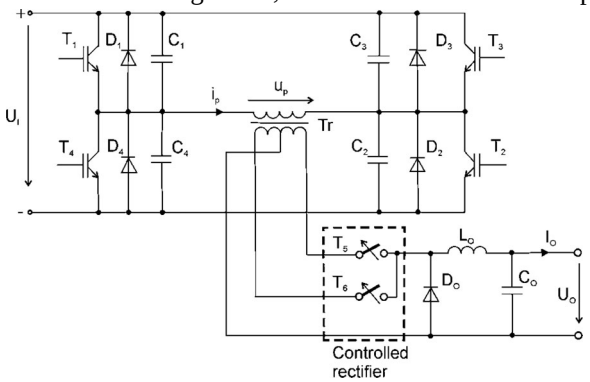


Fig.2: Principle of the ZVS converter with a controlled rectifier.

The principle is shown in Fig.2. Full-bridge inverter T_1-T_4 is controlled with constant switching frequency and 50% duty cycle and thus cannot control the output voltage or current value. Value of the output voltage or current is controlled via the phase shift between the inverter switches T_1-T_4 and switches T5 and T_6 on secondary side of a high-frequency power transformer. The primary switches turn off before the secondary switches do, and thus ZVS of the primary IGBT switches is achieved. Either full-bridge rectifier with two active switches [9]–[10] or centre-tapped full-wave rectifier [11]–[14] is usually used at the secondary side of the transformer. In the all known converters with controlled output rectifier described in [9]–[12], the primary IGBTs operate under ZVS. But at ZVS, switching conditions for IGBTs are not very satisfactory because of tail current problems. Moreover, at turn off of the primary transistors, the snubber capacitors in parallel with switches (or transistor output capacitances only) oscillate with parasitic inductances of the input source and wires in a loop with very low dumping. This increases electromagnetic interference in the converter. In addition, it is complicated to design snubber capacitors for primary transistors for a wide load range. Therefore, ZVS is usually lost at light load and at no-load in these converters, which consequently leads to overcurrent at turn on of the primary switches. To avoid this situation, various auxiliary circuits are added.

In [11], a small saturable inductor is added in series of the secondary switches in order to achieve ZVS easily. To solve this problem, commutation inductors are often connected at primary side of the converters [5], [18] to increase charging and discharging currents of the snubber capacitors and thus to avoid ZVS loss at light load. In order to improve switching conditions of the IGBTs in high-power, high-frequency converters, the zero-voltage and zero-current switching (ZVZCS) PWM dc–dc converter with secondary controlled rectifier, novel turn-off energy recovery snubber, and a new control algorithm is proposed. The proposed converter (see Fig. 3) follows from results in circuits [13], [14], where the primary switches turn OFF under zero current.

II. CONVERTER CIRCUIT DESCRIPTION

The proposed dc–dc converter shown in Fig.3 consists of a high-frequency IGBT full-bridge inverter, a centre-tapped power planar transformer, a controlled output rectifier, an output *LC* filter, and a novel type of secondary snubber. The main part of the converter is a high-frequency full-bridge inverter consisting of four fast IGBTs $T1-T4$ and freewheeling diodes $D1-D4$. The high-frequency centre-tapped step-down power transformer Tr with very low leakage inductance is used to transform high frequency voltage of the inverter.

The secondary winding of the high-frequency step-down power transformer Tr is connected through a controlled rectifier consisting of series connection of MOSFET and diode ($T5$, $D5$; $T6$, $D6$) to the output filter. The output filter consisting of smoothing choke LO and capacitor CO serves for smoothing- out of the rectified voltage.

Control pulses for the full-bridge inverter $T1-T4$ are very simple. They have constant switching frequency and no phase shift between legs of the inverter. So, the inverter operates approximately with 50% constant duty cycle and thus cannot influence the output voltage value.

Value of the output voltage or current is controlled by PWM of output rectifier (see Fig. 4). The control pulses for an output rectifier start simultaneously with the pulses for opposite pair of the primary switches (e.g., pulses for $T5$ start simultaneously with pulses for

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T_3 and T_4). The length of the secondary control pulses is changed from T to T /2 (dead times are neglected). It means that secondary switches are turned OFF prior to corresponding pairs of primary switches (e.g., T_5 prior to T_1 and T_2). As a result, the secondary and also primary current of the transformer drops to zero. Only magnetizing current flowing through the primary winding of the transformer is later turned OFF by primary transistors and thus ZC turn-off is achieved. This magnetizing current is high enough to charge or discharge output capacitances C_{OSS} of the primary transistors at turn off

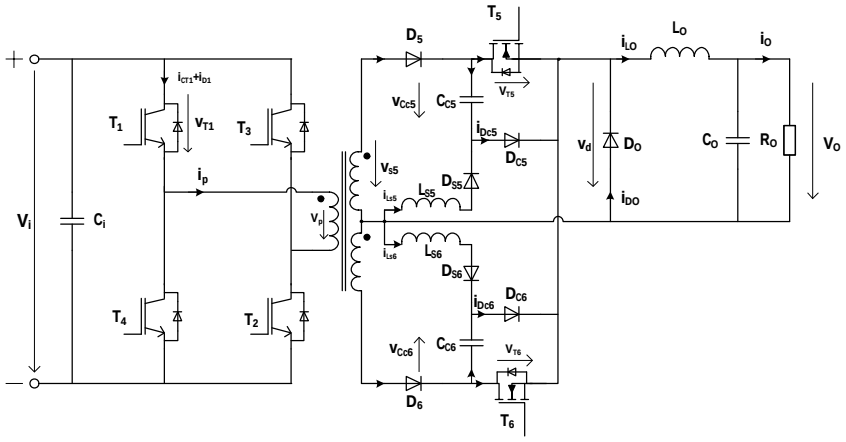


Fig.3(a): Scheme of the proposed converter.

during dead time. So, the ZV turn-on of the primary transistors is reached.

The energy recovery turn-off snubber consists of nondissipative passive components only. By connecting the snubber capacitors C_{C5} and C_{C6} , through snubber diodes D_{C5} and D_{C6} in parallel with secondary transistors T_5 and T_6 , the turn-off losses of the transistors are substantially reduced. Accumulation of the leakage inductance energy of the power transformer at turn off of the secondary transistors is the second function of the snubber capacitors. The leakage inductance energy accumulated in snubber capacitors is consequently transferred through snubber inductors L_{S5} and L_{S6} to the load. This accumulated energy transfer is realized through the secondary switch (e.g., T_5) immediately at its turn on. Simultaneously, the primary transistors (T_3 and T_4) are turned ON and active energy from primary side of the converter is transferred through opened secondary transistor T_6 to the load. It means that in this way of controlling the rms value of the secondary transistor current is considerably reduced and, consequently, conduction losses are decreased.

The new snubber circuit significantly minimizes the turn-off losses of the secondary transistors. The semiconductor switches T_5 and T_6 on the secondary side of the transformer are used to reset secondary and simultaneously also primary circulating current. The energy stored in the leakage inductance of the power transformer is transferred to the load.

III. OPERATION PRINCIPLE AND SNUBBER DESIGN

A. *Operation Principle of the Converter*

In this section, the basic operation of the proposed converter is described. It is assumed that all switching devices and passive components are ideal. The switching diagram and operation waveforms for rated load are shown in Fig.3 and operation analysis of the converter in Fig. 4(a)–(g). The dc–dc converter is controlled by the proposed modified PWM with variable length of the pulses for secondary switches.

Interval (t_0 –t_1): The secondary transistor T_5 is turned ON at t_0 half-period earlier than primary transistors T_1 and T_2 . The capacitor C_{C5} starts discharging through T_5 , L_O , R_O , L_{S5} , and follows:

$$i_{CC5}(t) = \sqrt{\frac{C_{C5}}{L_{S5}}}\left(\frac{V_I}{n} - V_{CC5}\right)\sin\left(\frac{t - t_0}{\sqrt{L_{S5}C_{C5}}}\right) \quad (1)$$

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$$v_{Cc5}(t) = \frac{V_I}{n} + \left(V_{Cc5} - \frac{V_I}{n}\right)\cos\left(\frac{t - t_0}{\sqrt{L_{s5}C_{c5}}}\right) \quad (2)$$

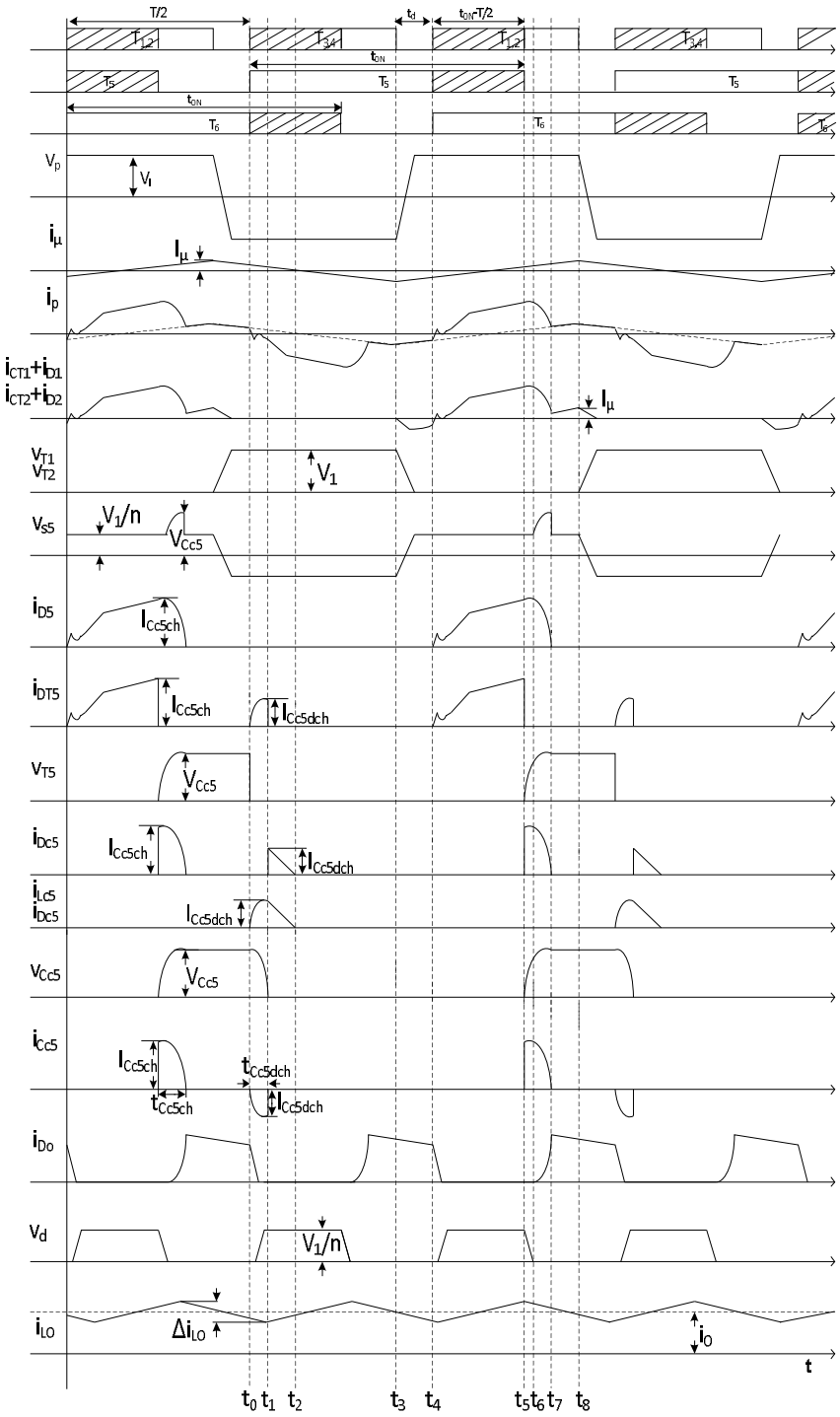


Fig.3(b): Operation waveforms of the converter.

From (2), it follows that total discharging of the capacitor occurs only in the case if its initial voltage V_{Cc5} is higher than double rectified voltage $v_d = V_I/n$

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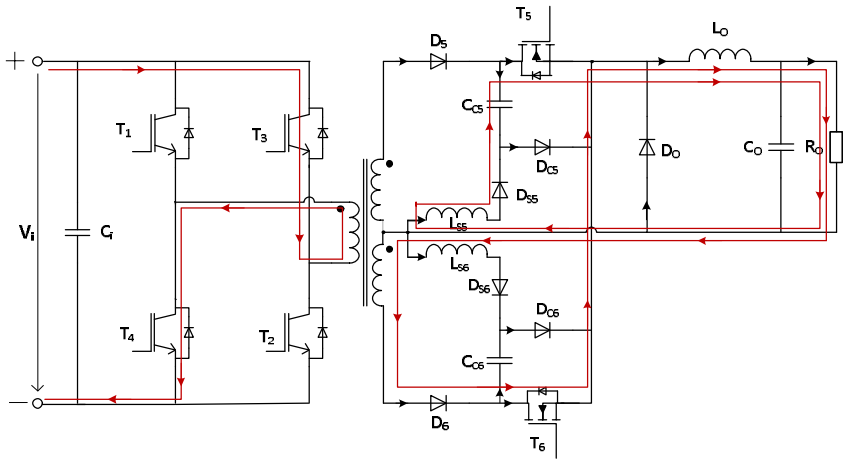


Fig.4(a): Operation in interval t_0-t_1.

The rate of rise of discharging current of the capacitor C_{C5} is limited by the snubber inductance L_{S5}, and thus zero current turn on for the transistor T_5 is achieved. At the same time, transistors T_3 and T_4 are turned ON. Because the transistor T_6 is already in on-state, so the output voltage of the rectifier v_d is equal to V_I/n (where $n = v_p/v_s$ is transformer turn's ratio).

Interval $(t_1 - t_2)$: The energy stored in snubber inductance L_{S5} is now transferred through D_{S5}, D_{C5}, L_O, R_O, and L_{S5}.

The snubber inductor current decays to zero according to equation:

$$i_{Ls5}(t) = \sqrt{V_{Cc5}\left(V_{Cc5} - 2\frac{V_I}{n}\right)}\sqrt{\frac{C_{c5}}{L_{s5}}} - \frac{V_I}{n}\frac{t - t_a}{L_{s5}} \quad (3)$$

From this equation, decay time of the inductor current can be determined

$$t_{Lc5dch} = t_2 - t_1 = \frac{\sqrt{V_{Cc5}\left(V_{Cc5} - 2\frac{V_I}{n}\right)}\sqrt{\frac{C_{c5}}{L_{s5}}}}{\frac{V_I}{n}} L_{s5} \quad (4)$$

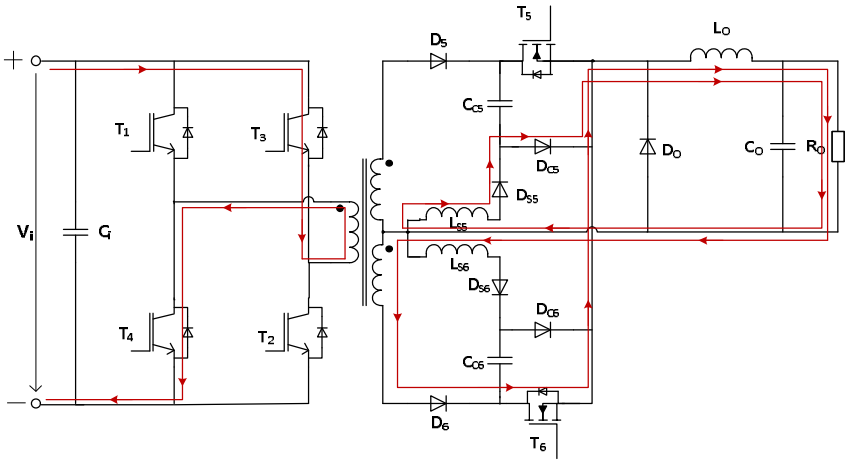


Fig.4(b): Operation in interval t_1-t_2.

The discharging current of capacitor C_{C5} reduces the current of the primary transistors T_3, T_4, and the current of the secondary transistor T_6. At t_2, the whole load current flows through the transistor T_6.

Interval$(t_3 - t_4)$: This interval starts with the turn off of the primary transistors T_3 and T_4. The magnetizing current of the

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transformer T_r discharges the output capacitances of the transistors T_1 and T_2 and charges the output capacitances of the transistors T_3 and T_4. If we assume that magnetizing inductance of the power transformer and the output smoothing inductance are much greater than leakage inductances (L_{1H}, L_O,$L_{1\sigma}$,$L_{2\sigma}$), then simplified equations for collector-emitter voltages of primary transistors T_1, T_2, and T_3, T_4 are obtained

$$v_{T1}(t) = v_{T2}(t)$$

$$\approx \frac{1}{2}V_i\left(1+\cos\left(\sqrt{\frac{1}{C_{OSS}L_\sigma}}(t-t_3)\right)\right)-\frac{1}{2}I_\mu\sqrt{\frac{L_\sigma}{C_{OSS}}}\sin\left(\sqrt{\frac{1}{C_{OSS}L_\sigma}}(t-t_3)\right) \quad (5)$$

$$v_{T3}(t) = v_{T4}(t)$$

$$\approx \frac{1}{2}V_i\left(1+\cos\left(\sqrt{\frac{1}{C_{OSS}L_\sigma}}(t-t_3)\right)\right)+\frac{1}{2}I_\mu\sqrt{\frac{L_\sigma}{C_{OSS}}}\sin\left(\sqrt{\frac{1}{C_{OSS}L_\sigma}}(t-t_3)\right) \quad (6)$$

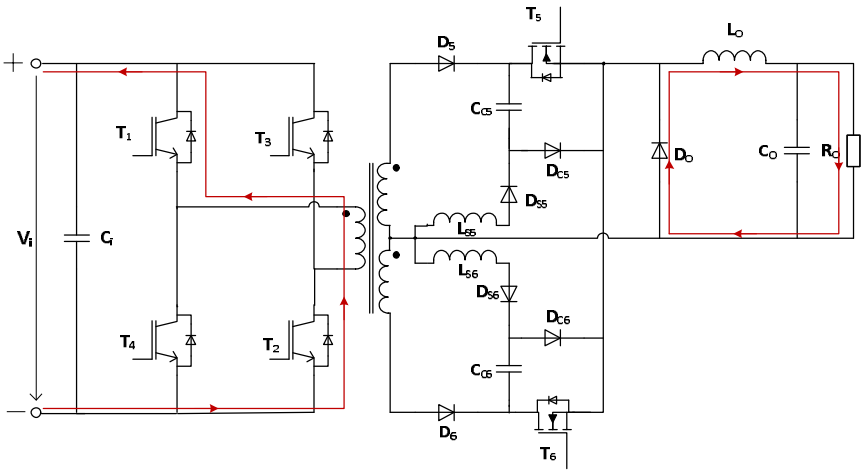


Fig.4(c): Operation in interval t_3-t_4.

$$t_4 - t_3 = t_d \approx \pi\sqrt{C_{OSS}(L_{1\sigma}+L'_{2\sigma})} \quad (7)$$

Interval($t_4 - t_5$): After turn on of the transistors T_1, T_2, and T_6, at t_4, commutation from the freewheeling diode D_O to the transistor T_5 occurs. Collector current of the transistor T_5 is reduced by the discharging current of the capacitor $C_{C\ 6}$ through the opposite transistor T_6 to load and later, after commutation to diode D_{C6}, by the current of the inductance L_{S6}.

The rate of rise of the collector current of the secondary transistor T_5 is limited by the leakage inductance referred to secondary side of the transformer

$$\frac{di_{DT5}}{dt} = \frac{V_i}{n}\cdot\frac{1}{(L'_{1\sigma}+L_{2\sigma})} \quad (8)$$

The rate of rise of the collector current of the primary transistors T_1 and T_2 is primarily limited by the leakage inductance referred to the primary side of the transformer

$$\frac{di_{CT1,CT2}}{dt} = \frac{V_i}{(L_{1H}+L_{1\sigma})}+\frac{V_i}{(L_{1\sigma}+L'_{2\sigma})} \quad (9)$$

The leakage inductance acts for secondary and primary transistors as a turn-on snubber.

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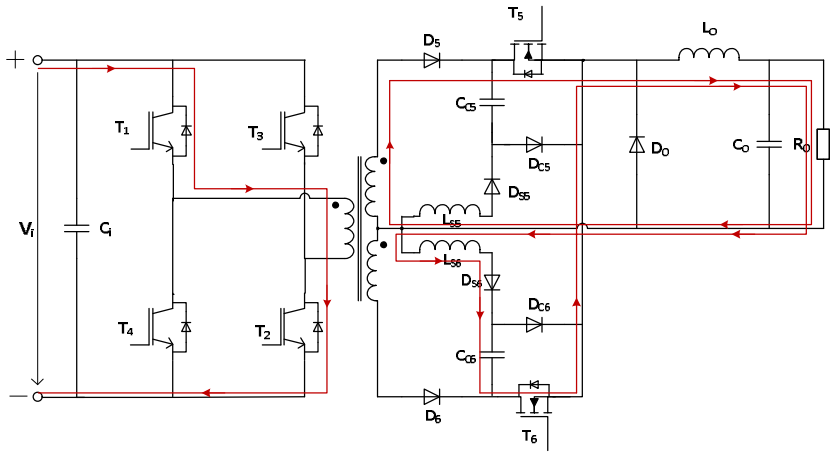


Fig.4(d): Operation in interval t_4-t_5.

Interval($t_5 - t_6$): At t_5 , the secondary transistor T_5 turns off. Its current commutates to the capacitor C_{C5} and the diode D_{C5} and consequently zero voltage turn off of this transistor is ensured. The energy of the leakage inductance of the power transformer is absorbed by the snubber capacitance C_{C5} and by the load. When assuming that $L_{1\sigma}$,$L'_{1\sigma}$, $L_{2\sigma}$, then the rectified secondary voltage drops to zero.

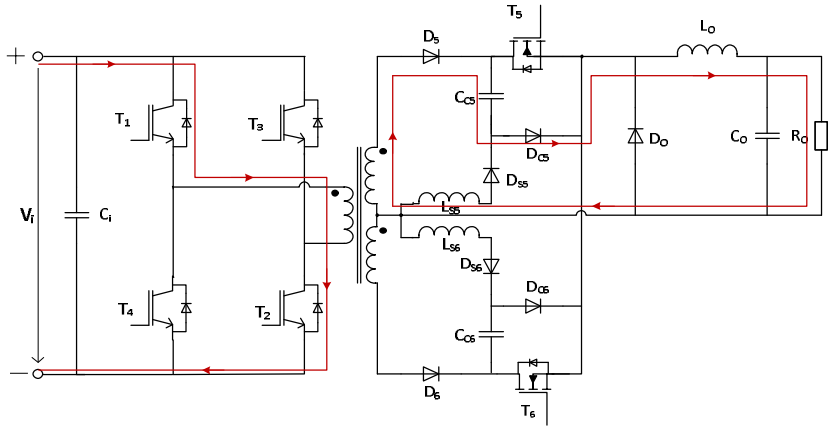


Fig.4(e): Operation in interval t_5-t_6.

Interval($t_6 - t_7$) : At t_6 , the rectified voltage v_d reached zero and afterward the waveform of the charging process of the capacitor C_{C5} are changed. In this interval, the whole energy of the leakage inductance is absorbed by the capacitor C_{C5} only.

Charging current of the capacitor can be expressed as

$$i_{C5}(t) = i_{C5}(t_6)\cos\left(\frac{t-t_6}{\sqrt{C_{C5}L'_\sigma}}\right) + \left(\frac{V_i}{n} - v_{C5}(t_6)\right)\sqrt{\frac{C_{C5}}{L'_\sigma}}\sin\left(\frac{t-t_6}{\sqrt{C_{C5}L'_\sigma}}\right) \quad (10)$$

Where

$L'_\sigma = L'_{1\sigma} + L'_{2\sigma}$ leakage inductance of the transformer reffered to the secondary side;

$L'_{1\sigma}$ leakage inductance of the primary winding reffered to the secondary side;

$L'_{2\sigma}$ leakage inductance of the secondary winding.

The capacitor voltage rises according to equation:

$$v_{C5}(t) = \frac{V_i}{n} + \left(v_{C5} - \frac{V_i}{n}\right)\cos\left(\frac{t-t_6}{\sqrt{C_{C5}L'_\sigma}}\right) + i_{C5}(t_6)\sqrt{\frac{L'_\sigma}{C_{C5}}}\sin\left(\frac{t-t_6}{\sqrt{C_{C5}L'_\sigma}}\right) \quad (11)$$

At t_7 , the current flowing through the rectifying diode D_5 decays to zero and current of the transistors T_1 and T_2 drops to value of magnetizing current of the transformer, because the capacitor absorbed all the leakage inductance energy.

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Charging time of the capacitor C_{C5} is approximately:

$$t_{ccsch} = t_7 - t_6 \approx \frac{\pi}{2}\sqrt{C_{cs}(L'_{1\sigma} + L_{2\sigma})} \quad (12)$$

The value of the capacitor voltage charging is

$$V_{ccs} \approx \frac{V_I}{n} + \left(t_o + \frac{\Delta i_{Lo}}{2}\right)\sqrt{\frac{(L'_{1\sigma} + L_{2\sigma})}{C_{cs}}} \quad (13)$$

The value of the capacitor voltage V_{Cc5} depends on the leakage inductance. The higher the leakage inductance $(L'_{1\sigma} + L_{2\sigma})$, the higher the capacitor voltage. Therefore, leakage inductance of the power transformer should be as low as possible.

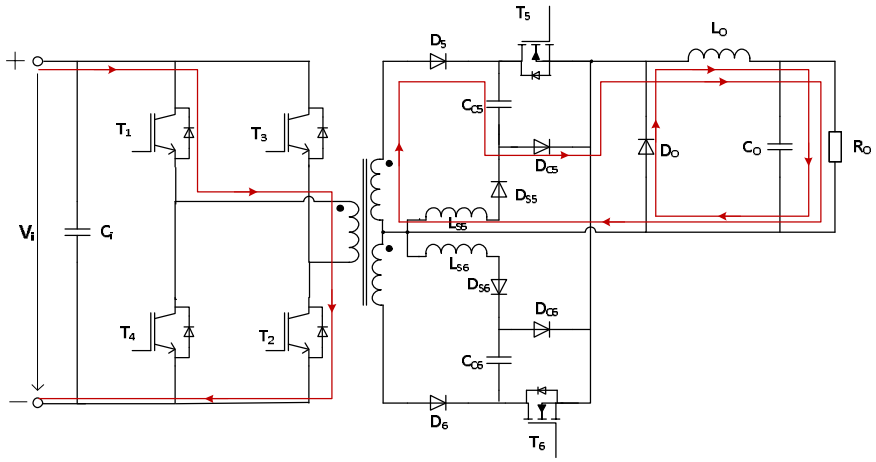


Fig.4(f): Operation in interval t_6-t_7.

Interval($t_7 - t_8$) *:* Only the magnetizing current flows through the primary winding of the power transformer in this interval. This small magnetizing current is turned OFF by primary switches and thus zero current turn off is achieved. The current of the smoothing inductance L_O is flowing through the freewheeling diode D_O now.

At t_8, the primary transistors turn off only magnetizing current, whose magnitude is given by

$$I_\mu = \frac{V_I}{2(L_{1M} + L_{1\sigma})}\frac{T}{2} \approx \frac{V_I}{2L_{1M}}\frac{T}{2} \quad (14)$$

The smoothing inductance current ripple is

$$\Delta i_{Lo} = \frac{V_O}{L_O}\frac{T}{2}(1 - d) \quad (15)$$

where $d = \frac{\left(t_{ON} - \frac{T}{2}\right)}{\frac{T}{2}}$ is duty cycle.

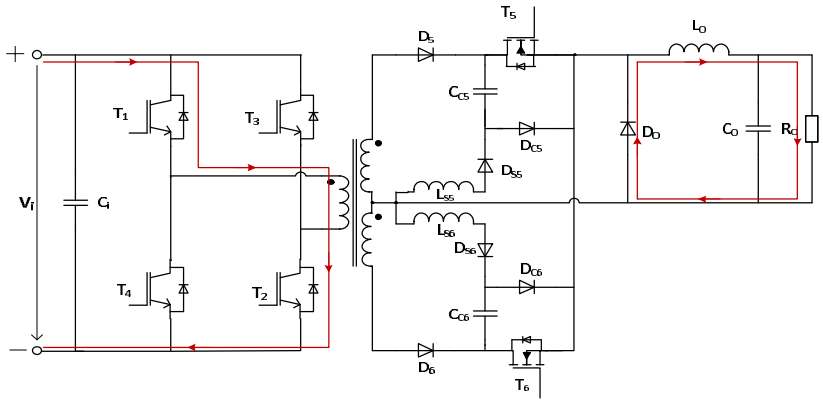


Fig.4(g): Operation in interval t_7-t_8.

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The output voltage can be determined as

$$V_o = \frac{\left(t_{ON} - \frac{T}{2}\right)\frac{V_i}{n}}{\frac{T}{2}} = d\frac{V_i}{n} \quad (16)$$

The smoothing inductance L_O current ripple can be expressed as

$$\Delta i_{Lo} = \frac{T}{2L_o}\left(V_o - \frac{V_o^2}{V_i}n\right) = \frac{V_i T}{2nL_o}(d - d^2) \quad (17)$$

The Output voltage ripple is given by

$$\Delta V_o = \frac{1}{C_o}\int_0^{d\frac{T}{2}} \frac{\Delta i_{Lo}}{d\frac{T}{2}} t dt = \frac{T^2}{8C_oL_o}\left(\frac{V_o^2}{V_i}n - \frac{V_o^3}{V_o^2}n^2\right) = \frac{V_i T^2}{8C_oL_o}(d^2 - d^3) \quad (18)$$

B. Snubber Design

Simplified design of the snubber parameters is given by applying or converting the previously derived equations. Value of the snubber capacitor is derived from (13), where the maximum permissible capacitor voltage V_{Cc5} is chosen

$$C_{cs} \approx \frac{\left(i_o + \frac{\Delta i_{Lo}}{2}\right)^2 (L'_{1\sigma} + L_{2\sigma})}{\left(V_{ccs} - \frac{V_i}{n}\right)^2} \quad (19)$$

Entire energy of the leakage inductance is accumulated in the snubber capacitor at turn off of the secondary switch. The higher leakage inductance of the power transformer referred to the secondary side $L'_\sigma = L'_{1\sigma} + L'_{2\sigma}$, the higher must be snubber capacitance, so that the capacitor voltage V_{Cc5} would not exceed maximum permissible value. Thus , leakage inductance of the transformer should be as small as possible.

Charging time t_{Cc5ch} of the snubber capacitor is calculated from (12). If the maximum discharging current I_{Cc5dch} is chosen, then value of the snubber indicator expressed as follows:

$$L_{ss} = \frac{C_{cs}\left(V_{ccs} - \frac{V_i}{n}\right)^2}{I_{Ccsdch}^2} \quad (20)$$

During discharging and decay times ($t_{Cc5dch} + t_{LS5dch}$), the energy of the leakage inductance stored in the snubber capacitor is transferred to the load.

According to the proposed control algorithm, there is enough time for discharging and decay of the snubber current during leakage inductance energy transfer—at least half of period. Therefore, low value of the discharging current can be chosen, which is one of the advantages of this way of control.

IV. SIMULATION RESULTS

The converter of 4.5kW with 325V dc at switching frequency of 100kHz was designed and simulated in MATLAB/SIMULINK software with the component values obtained from the design procedure and A special planar transformer with very low leakage inductance was designed with parameters presented in Table I.

The primary transistor collector-emitter voltage and collector current including gate signals of primary and secondary transistors are shown in Fig.6. After drop of the secondary MOSFET transistor gate signal V_{GST5} to zero, transformer primary current sinks to the value of magnetizing current. This small magnetizing current is later turned OFF by primary IGBTs and thus only negligible turn-off losses occur. At the turn on of the primary IGBTs, the primary current (transformer magnetizing current) discharges their output capacitances to zero. The rate of rise of the collector current is limited by the leakage induc- tance of transformer and thus zero voltage zero current turn on is ensured for primary IGBTs.

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Switching trajectory of the primary transistor is shown in Fig.7. It is evident that operating point of the primary transistor is moving in the low losses area.

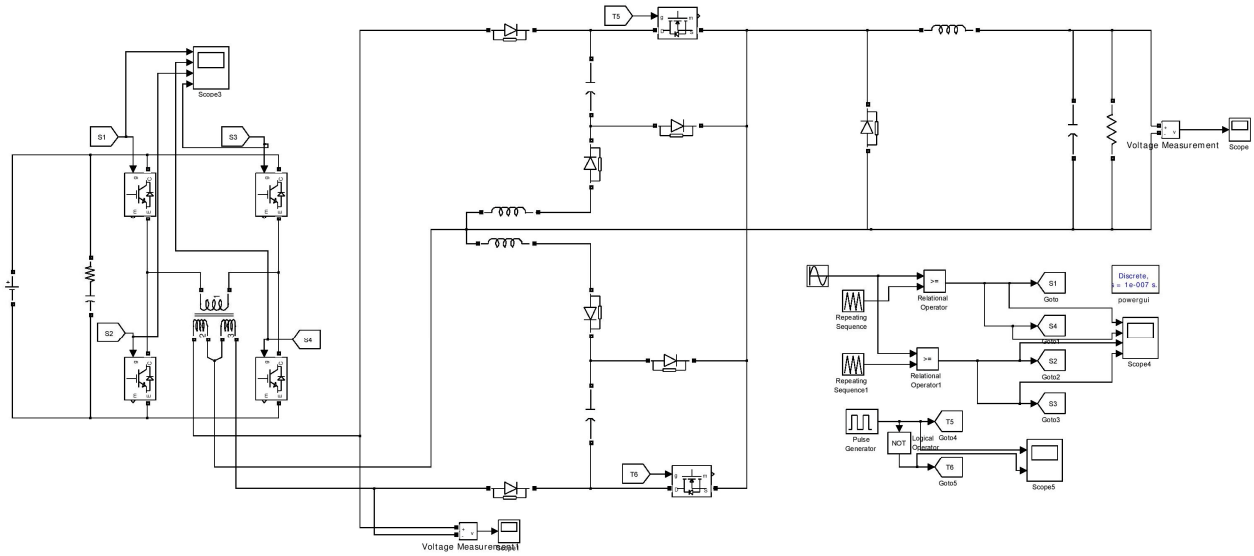


Fig.5: Simulink diagram of proposed converter

Primary voltage and current of power planar transformer are shown in Fig.8. The switches (T_1 , T_2) and (T_3 , T_4) operate very simple as two pairs with duty cycle of 0.5 and therefore the primary voltage is rectangular. It can be seen that circulating current is totally suppressed by using a controlled output rectifier. After elimination of circulating current, only a small magnetizing current of the transformer flows through primary winding.

Primary voltage v_p and primary current i_p of the transformer T_r at no-load are shown in Fig. 9. The minimum current should be set to ensure charging or discharging of output capacitances $C_{OSS1} - C_{OSS4}$ of the transistors $T_1 - t_4$ during dead time t_d.

TABLE-I
PARAMETERS OF THE CONVERTER

Parameters	Value
L_{S5},L_{S6}	0.3µH
C_{S5},C_{S6}	220nF
L_O	5.3µH
C_O	100µH
Turn's ratio n=n_p/n_s	5:1
Primary winding resistance R_1	6.5mΩ
Secondary winding resistance R_2	0.75mΩ
Magnetizing inductance L_{1H}	706µH
Leakage inductance referred to primary side L_σ	625nH

Its value can be approximately calculated from

$$I_{ch,min} \approx \frac{2C_{OSS} \cdot V_I}{t_d} \quad (21)$$

where $C_{OSS} = C_{OSS1} = C_{OSS2} = C_{OSS3} = C_{OSS4}$.

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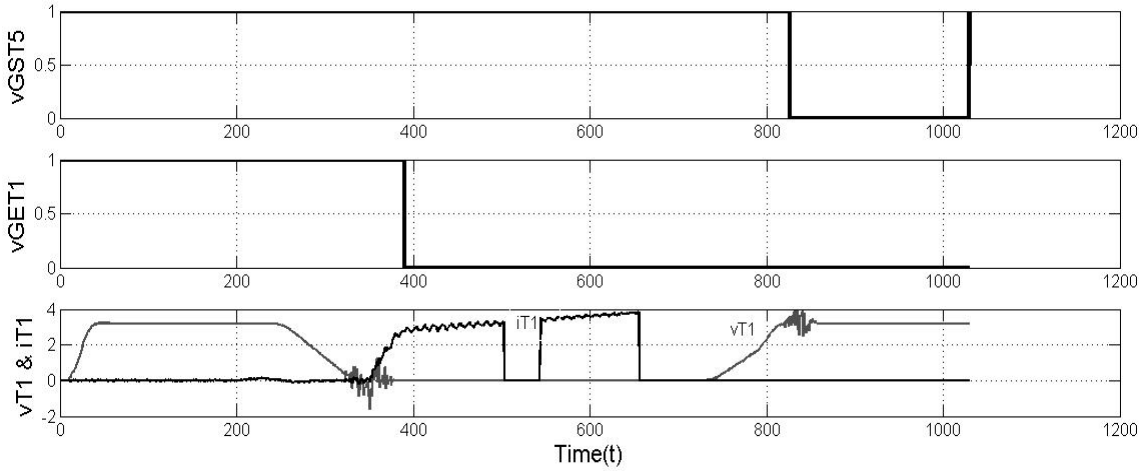


Fig.6: Primary transistor voltage v_{T1} and current i_{T1} at turn on and turn off and gate signals for secondary v_{GST5} and primary v_{GET1} transistors.

Maximum value of the magnetizing current $I_{\mu} \geq I_{ch,min}$ is set by design to approximately 1A, which is high enough for charging or discharging of output capacitances of the primary transistors during dead time in a leg of the converter. The value of the magnetizing current can be adjusted either by air gap or by number of primary turns.

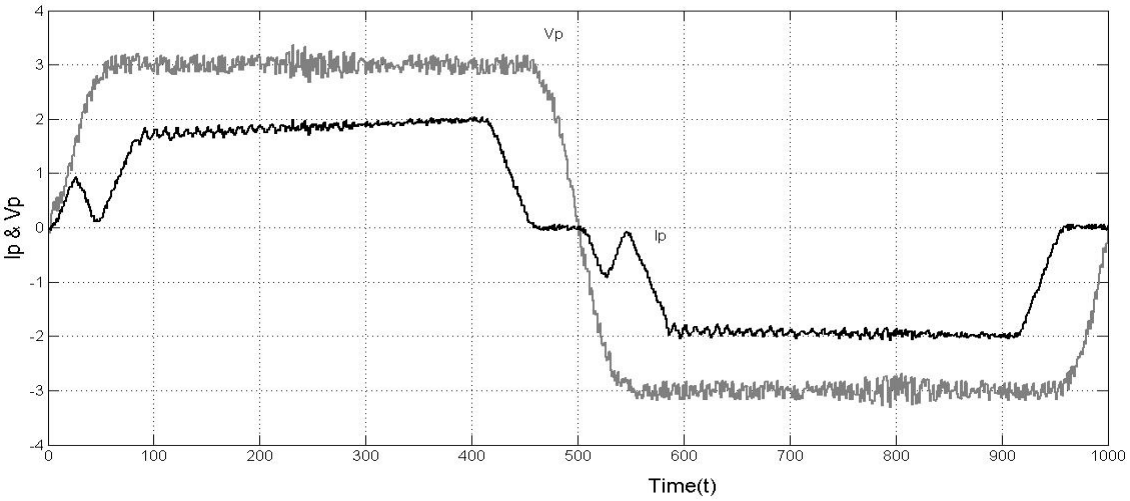


Fig.7: Primary voltage v_P *and* current i_P *of* the transformer.

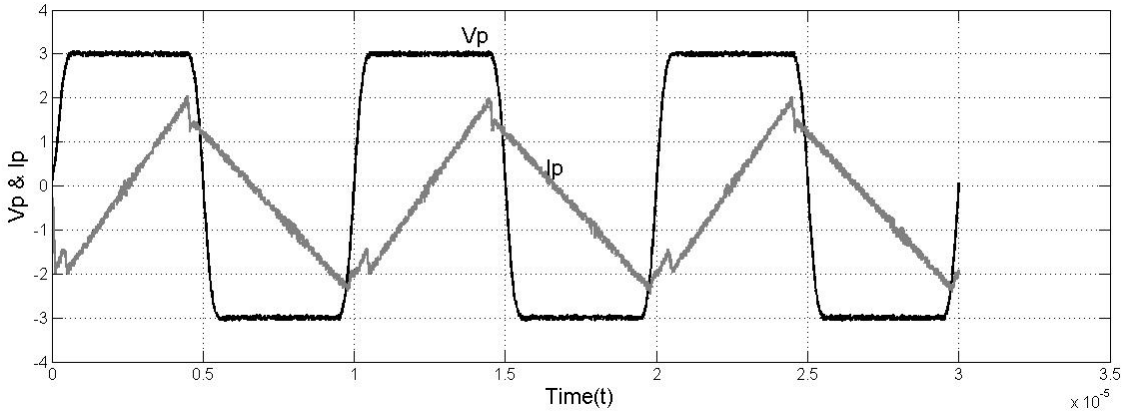


Fig.8: Primary voltage v_P and current i_P of the transformer at no-load.

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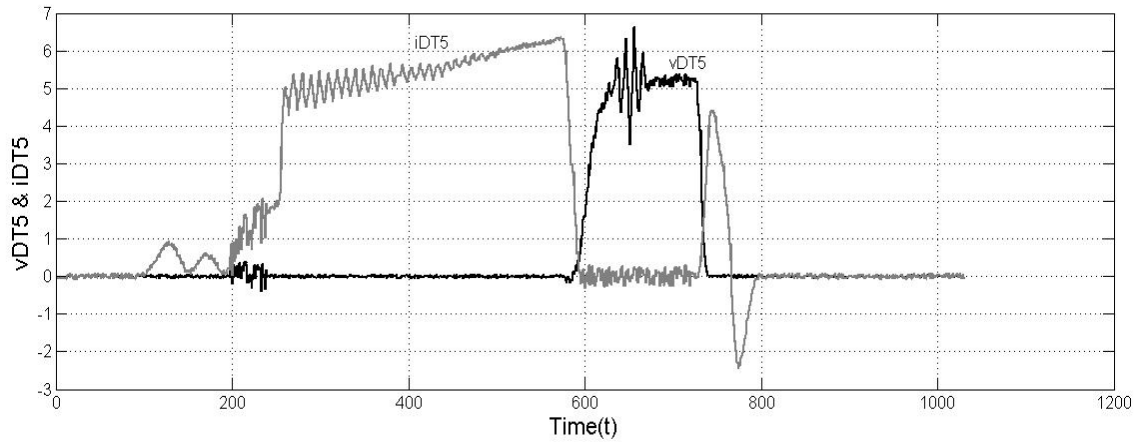


Fig.9: Secondary transistor voltage and current at turn on and turn off.

Drain-source voltage and drain current of the secondary transistor at turn on and turn off are shown in Fig.9. At turn off of the MOSFET transistor T_5 , its drain current commutates to the snubber capacitor $C_{C\,5}$ and thus rate of rise of the drain–source voltage is reduced. At the turn on of the transistor T_5 , the capacitor $C_{C\,5}$ is discharged through transistor and snubber inductance L_{S5} to the load in a resonant way. Therefore, the rate of rise of the discharging current is limited.

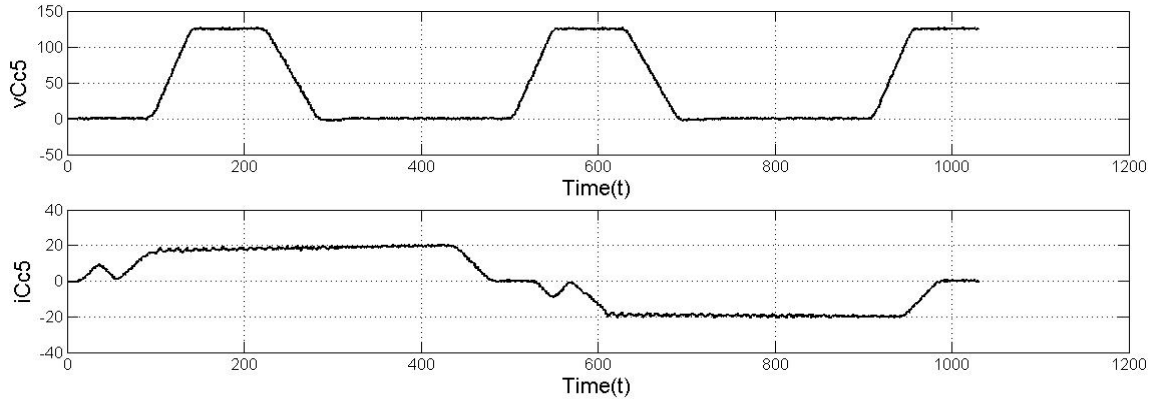


Fig.10: Snubber capacitor voltage v_{Cc5} and snubber capacitor current i_{Cc5} at charging and discharging.

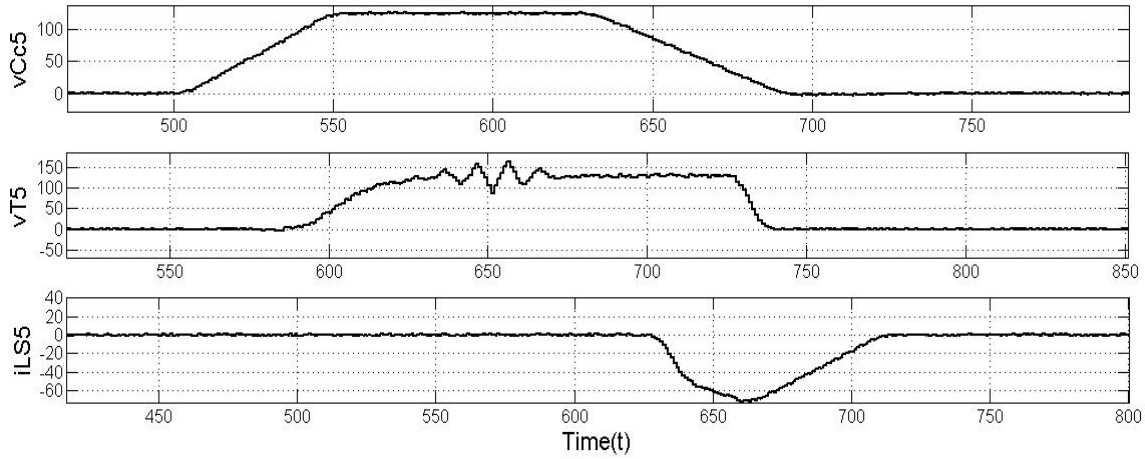


Fig.11: Snubber capacitor voltage v_{Cc5} , secondary transistor voltage v_{DS5} and snubber inductor current $i_{LS\,5}$ at charging and discharging of the capacitor C_{C5}.

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Charging and discharging of the snubber capacitor are shown in Fig. 10. At charging of the capacitor C_{C5}, the rate of rise of the drain–source voltage V_{DS5} of the parallel-connected secondary transistor T_5 is decreased and thus ZV turn off is ensured. At turn on of the secondary transistor T_5, the capacitor is discharged through snubber inductance L_{S5} to the load in a resonant way. At turn off of the secondary transistor T_5, the snubber capacitor discharges through snubber inductance L_{S5} and energy transfers to the load as shown in Fig. 11. The proposed control method enables energy transfer to the load up to half of the period without any problems. As a result, amplitude of the discharging current can be reduced.

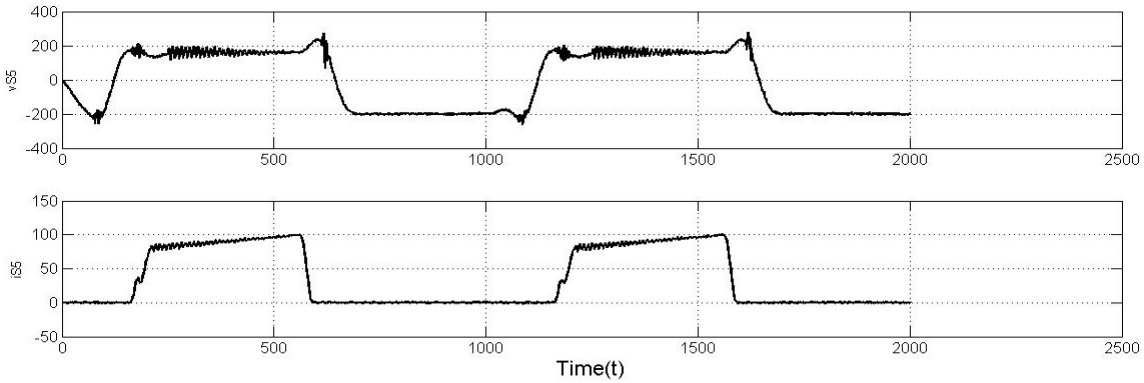


Fig.12: Secondary voltage v_{S5} and secondary current i_{S5} of the transformer.

Secondary voltage v_{S5} and secondary current i_{S5} of the transformer are shown in Fig. 12. After turn off of the secondary transistor T_5, the secondary current i_{S5} continues to flow through snubber capacitor. As a result, the voltage spikes appear on the secondary voltage v_{S5}. The converter was designed as a dc voltage source with rated output voltage of 45 V is shown in Fig.13.

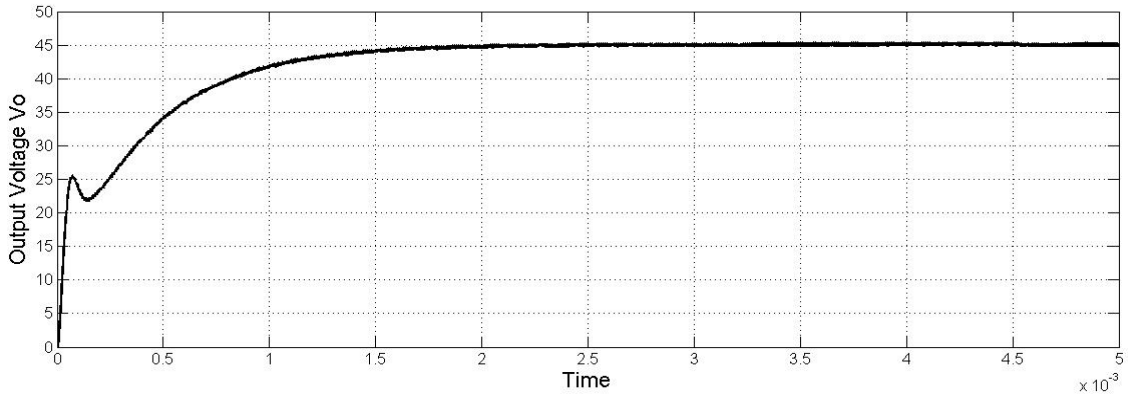


Fig.13: Output Voltage Vo

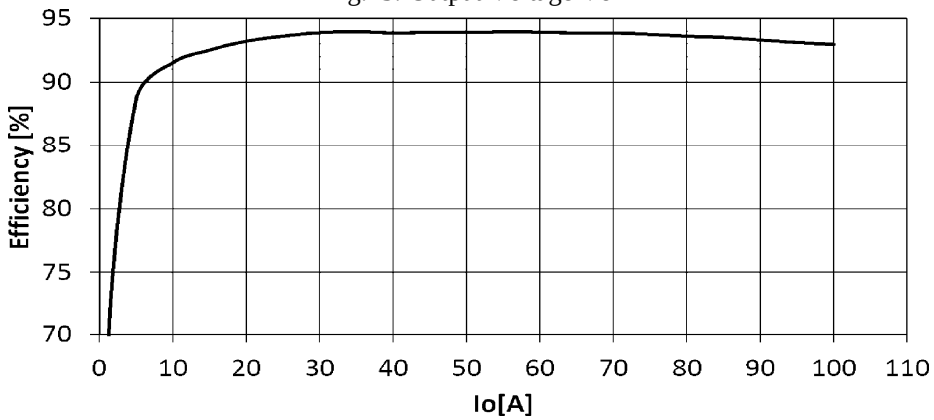


Fig. 14: Efficiency of the converter.

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Efficiency of the converter at rated output voltage of 45 V is shown in Fig. 14. Maximum efficiency of the converter is around 94%. The decrease in efficiency for currents of 30 up to 100 A is caused by conduction losses, especially when two secondary devices are in series with the load current. The impact of conduction losses is highly significant in converters with low output voltage and high output current, like in our case. Despite these facts, the efficiency is quite high. Of course, it would be higher for high output voltage and low output current.

V. CONCLUSION

The topology of PWM dc–dc converter that permits all switching devices to operate under soft switching by using a controlled rectifier and the turn-off snubber is described in this paper.

Soft switching and reduction of circulating currents in the proposed converter are achieved for full-load range using a secondary-side turn-off snubber in combination with a con- trolled output rectifier and an appropriate control algorithm.

By proper design, it is possible to utilize magnetizing current of the power transformer for charging or discharging output capacitances of the IGBT switches and thus to achieve zero voltage turn on of the IGBTs.

The IGBTs are turned OFF almost under zero current. Only small magnetizing current of the power transformer is turned OFF by IGBTs.

The important task of the proposed secondary turn-off snub- ber is accumulation of the leakage inductance energy, and fol- lowing transfer of this energy to the load. Moreover, the snubber ensures zero current turn on and zero voltage turn off of the sec- ondary switches.

IGBTs in the full-bridge inverter operate at almost ideal switching conditions—zero voltage turn on and zero current turn off, which is the main advantage of the proposed converter.

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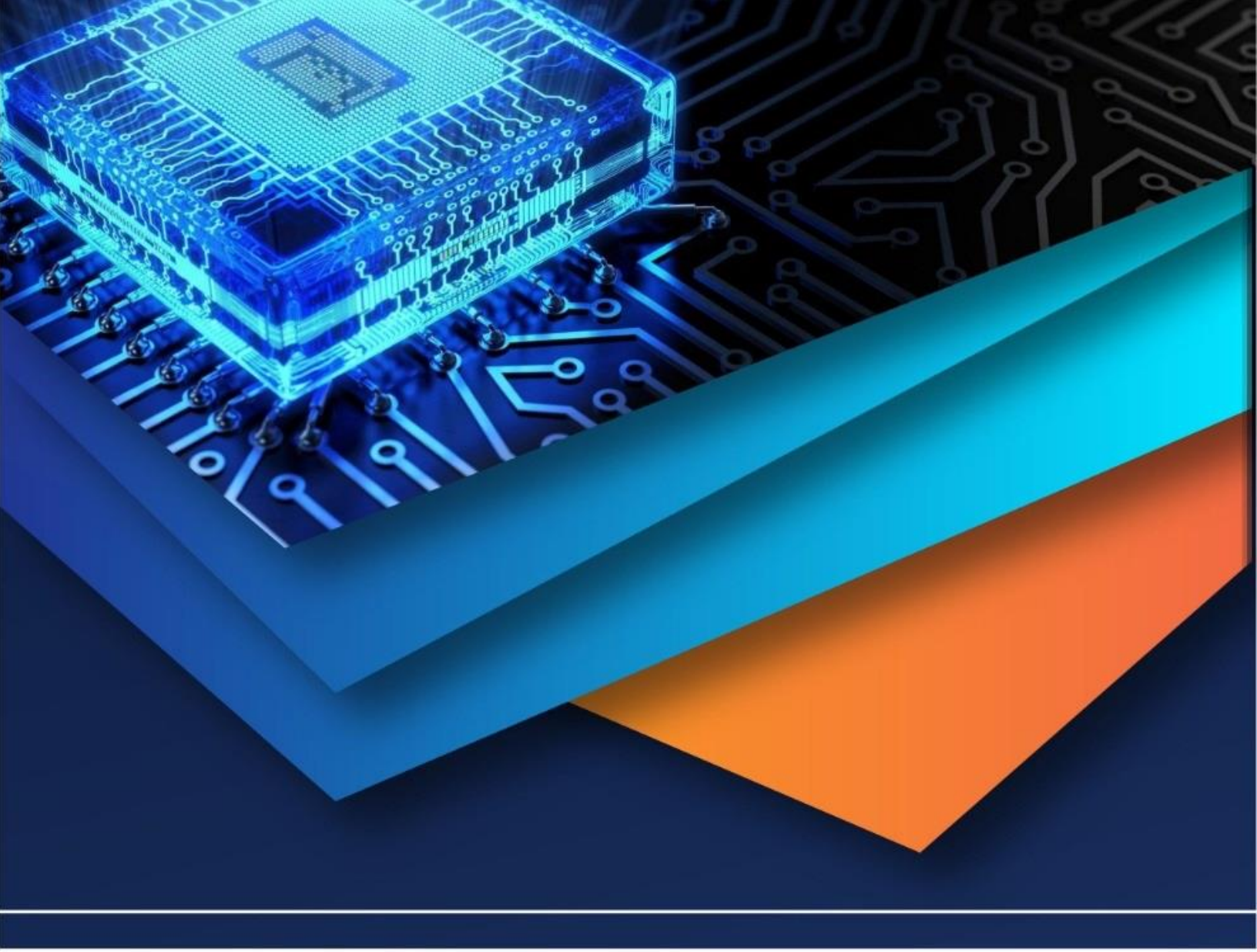
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