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FPGA Implementation OF Iterative Log Multiplier Using Operand Decomposition For Image Processing Application

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Abstract—Faster multiplier is the vital procedure mainly for DSP and image processing application. Log multiplier converts the multiplication into addition, hence speed up the multiplication. Mitchell's approximation based log multiplier does this but with errors. OD-Mitchell reduces the AEP (Average Error Percent) while the iterative Mitchell reduces the MPE (Maximum Possible Error).This project focuses on combining both the method to improve AEP and MPE. Further this multiplier is used in case of Gaussian filter to improve PSNR (Peak Signal To Noise Ratio).Hence the accuracy is improved here. The hardware implementation is done by using the FPGA board. The simulation is done using XILINX 14.5 and Modelsim.

Keywords—AEP, MPE, Gaussian filter, PSNR,FPGA

I. INTRODUCTION

The binary multipliers operate on the binary operands and calculate products by using partial product additions. Logarithmic multiplier converts the binary operands into their corresponding logarithmic form. In LNS (Logarithmic Number System) multiplication is achieved by means of addition. Hence the Multiplication is obtained by first calculating logarithms of binary numbers and then adding individual log values, finally calculating antilog value of the added sum.

The multiplication using logarithm function is used in a large number of applications such as digital signal processing and image processing, biomedical systems, telecommunication systems and so on. Calculation of logarithm function using software is not fast enough, and hence a dedicated hardware should be used. Also the dedicated hardware has become much attractive to design the arithmetic blocks in 3-D graphics systems for mobile applications and for Cartesian-to-polar coordinate translation systems. Logarithmic number system of base two is used to optimize the arithmetic block like multiplication, division and square root. It maintains high performance without incurring excessive area and power increment.

Basically in a large number of DSP applications, speed is the significant criteria compared to accuracy. In these cases, the most suitable multiplier is the truncated and Logarithmic multipliers. In case of truncated multipliers, the less important partial products are left out and recompense is provided. So it partly compensates for left out terms. In the Logarithmic multipliers rounding of products can be done. It is alternatively used for fixed point number and floating point number. This translates multiplication into addition and division into subtraction. The main goal of Log Multiplier is to lessen errors with power utilization. One of the methods to calculate log and antilog is to use LUT method, but it requires more area to store the log and antilog values. The Mitchell log multiplier uses only some shift operations for log and antilog calculations .So it require fewer hardware overhead and results high speed with less power utilization.

II.LITERATURE SURVEY

Till now papers are published based on OD-Mitchell and Iterative Mitchell separately. A paper for the process of binary logarithm has been also published. How the multipliers are used in filters to improve the accuracy also has been done. The filter has removed the salt pepper noise, Gaussian noise and high frequency noise.

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II. PROPOSED SYSTEM

The proposed system aims at solving the accuracy problem. It reduces the maximum possible error by using iterative method and also reduces the average error rate by using the operand decomposition method. Operand decomposition is done prior to the Mitchell logarithm. After skipping the leading one from both the number, again these are given as input to one more basic block. Finally both the output is added to give the final output.

The key component in the Gaussian filter is the convolution between the Gaussian mask and the 255*255 pixel values. Hence according to the accuracy of the multiplier, the PSNR of an image having Gaussian noise and salt pepper noise has been improved.

III. WORK METHODOLOGY

The basic block includes logarithm block, adder, and antilogarithm block along with zero detector. The error involved here is more. So the proposed architecture has been implemented. The below figure is the basic Mitchell block.

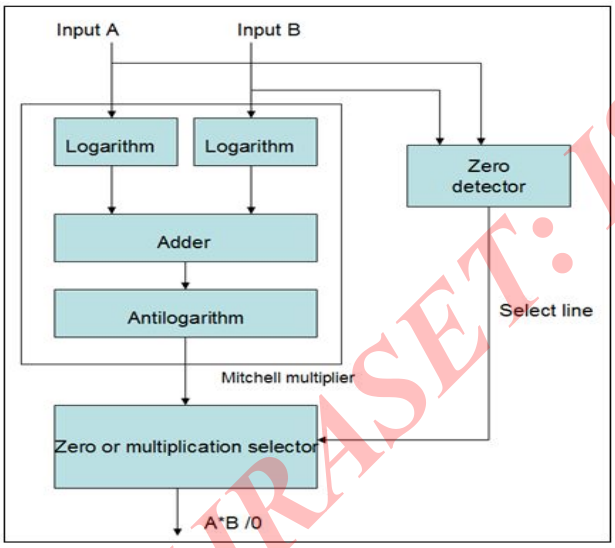

Fig 1: Basic Mitchell Block

As shown in the figure Operand decomposition reduces the error caused by the carry over generated from the mantissa part to the characteristic part. Hence when we apply this through the Mitchell block the error will be reduced compared to the only Mitchell block. The iteration of the Mitchell again reduces the maximum possible error.

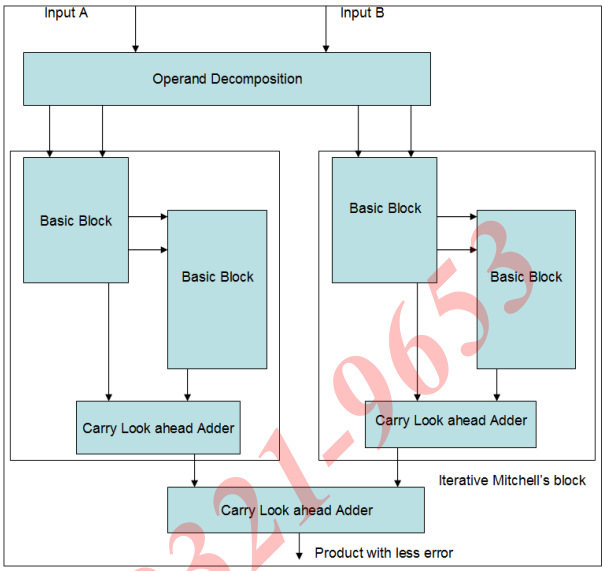

Fig 2: Proposed Mitchell Block

The Gaussian filter is implemented using FIFO memory, hence reduces the area utilization. The image with Gaussian noise and the salt pepper noise are made noise free with the help of Gaussian filter that uses the proposed multiplier.

V.RESULT

Simulations of the proposed design will be conducted in the Xilinx 14.5 and modelsim . The verified Verilog code will be then dumped into FPGA board.

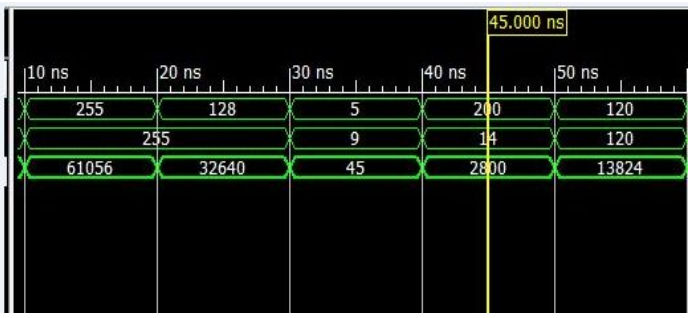

Fig 3: Simulation result of the proposed multiplier using XILINX

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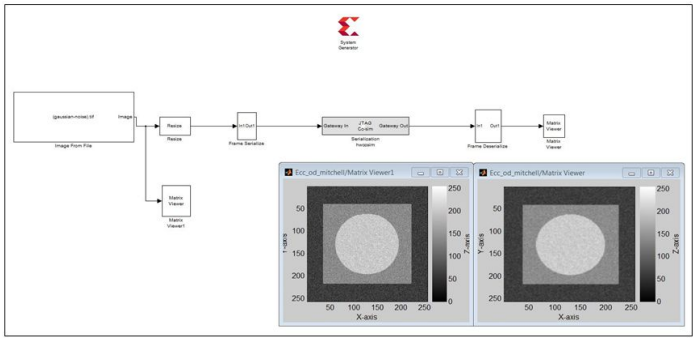

Fig 4: Verilog simulation result in Spartan-6 FPGA board using system generator

Standard Deviation with mean=0	Filter using Basic-Mitchell	Filter using OD-Mitchell	Filter using Ecc-basic-block	Filter using Ecc-OD-Mitchell
1	31.2288	31.2288	35.896	36.0896
1.2	28.1308	29.0459	32.567	34.15140
1.4	28.1308	29.049	32.567	34.1514
1.6	29.0459	31.22884	33.15	34.15

TABLE I: PSNR comparison of an image

We have shown a proposed method of multiplier in order to get more speed with less error. Also we have shown the application of multiplier in Gaussian filter to increase the PSNR.. This proposed architecture can be applied to the MAC unit, where we require large number of convolution, FFT filter, FIR filter if pipeline can be achieved.

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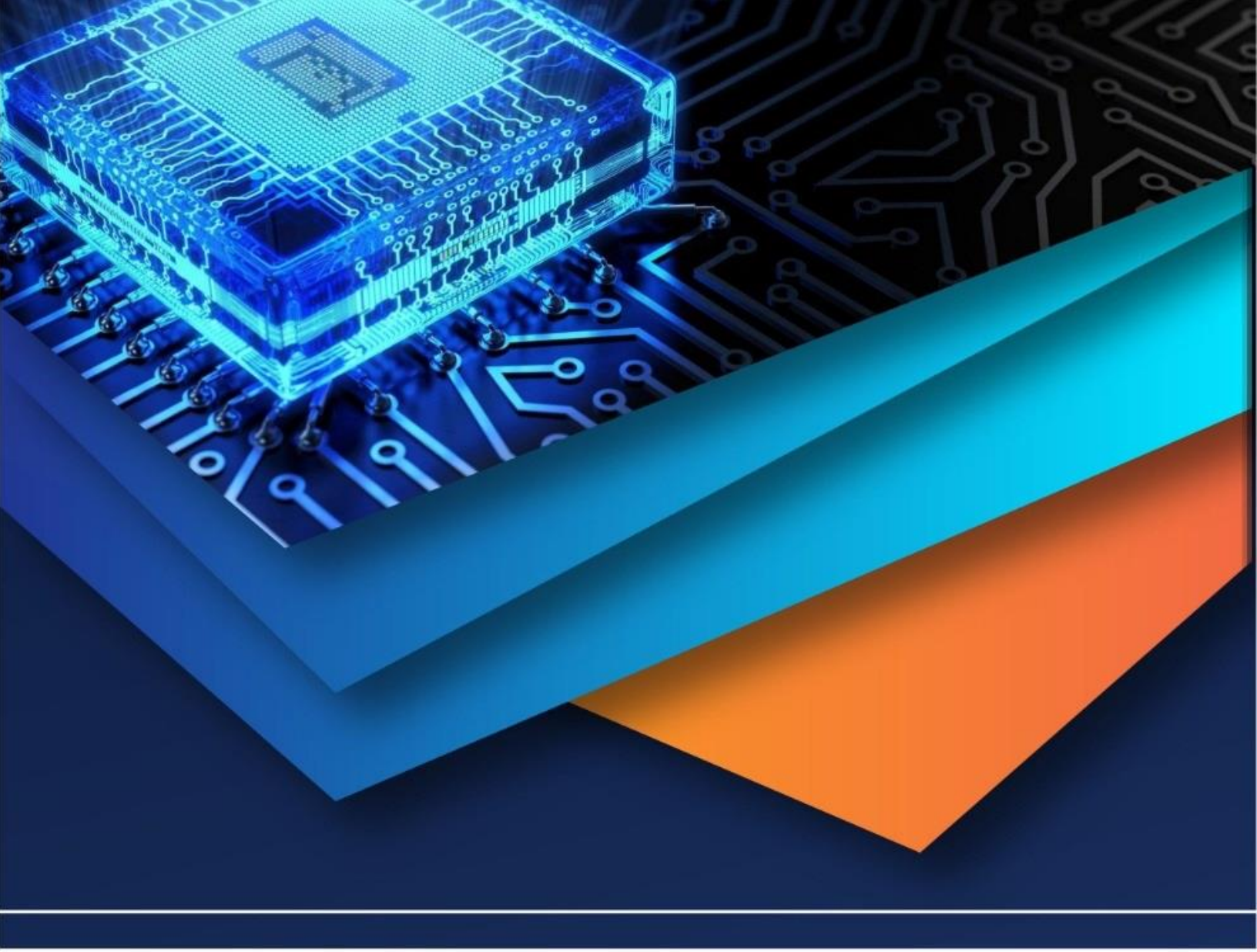

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