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Improved Interline Unified Power-Quality Conditioner with Multi Level Converter

N. Bharath Kumar[1], B. R. Narendra[2]
[1]*M. Tech in Power Electronics from MIC College of Science and Technology, Kanchikacharla*
[2]*Associate Professor, MIC College of Science and Technology, Kanchikacharla*

Abstract- This paper proposes a new connection for a unified power quality conditioner (UPQC) to improve the power quality of two feeders in a distribution system. A UPQC consists of a series voltage-source converter and a shunt VSC both joined together by a common dc bus. It is demonstrated how this device is connected between two independent feeders to regulate the bus voltage of one of the feeders while regulating the voltage across a sensitive load in the other feeder. Thus Interline connected Unified Power Quality conditioner made to improve the power quality and efficiency of the system. The performance of the IUPQC is illustrated by simulation. The results obtained in MATLAB on a two-bus/two-feeder system with 7 level converter show the effectiveness of the proposed configuration
Index Terms: Power Quality, Interline Unified Power Quality Conditioner, Feeders, Voltage Source Converter, Matlab.

I. INTRODUCTION

As the power quality problems are originated from utility and customer side, the solutions should come from both and are named as utility based solutions and customer based solutions respectively. The best examples for those two types of solutions are FACTS devices (Flexible AC Transmission Systems) and Custom power devices. FACTS devices are those controlled by the utility, whereas the Custom power devices are operated, maintained and controlled by the customer itself and installed at the customer premises.

Voltage-source converter (VSC)-based custom power devices are increasingly being used in custom power applications for improving the power quality (PQ) of power distribution systems. Devices such as distribution static compensator (DSTATCOM) and dynamic voltage restorer (DVR) are the facts devices. A DSTATCOM can compensate for distortion and unbalance in a load such that a balanced sinusoidal current flows through the feeder. It can also regulate the voltage of a distribution bus. A DVR can compensate for voltage sag/swell and distortion in the supply side voltage such that the voltage across a sensitive/critical load terminal is perfectly regulated .A unified power-quality conditioner (UPQC) can perform the functions of both DSTATCOM and DVR. The UPQC consists of two voltage-source converters (VSCs) that are connected to a common dc bus. One of the VSCs is connected in series with a distribution feeder, while the other one is connected in shunt with the same feeder. The dc links of both VSCs are supplied through a common dc capacitor. It is also possible to connect two VSCs to two different feeders in a distribution system. In, a configuration called IDVR has been discussed in which two DVRs are connected in series with two separate adjacent feeders. The dc buses of the DVRs are connected together. The IDVR absorbs real power from one feeder and maintains the dc link voltage to mitigate 40% (about 0.6 p.u.) Voltage sag in the other feeder with balanced loads connected in the distribution system. It is also possible to connect two shunt VSCs to different feeders through a common dc link. This can also perform the functions of the two DVRs mentioned above, albeit with higher device rating. This paper presents a new connection for a UPQC called interline UPQC (IUPQC). The single-line diagram of an IUPQC connected distribution system is shown in Fig. 1.

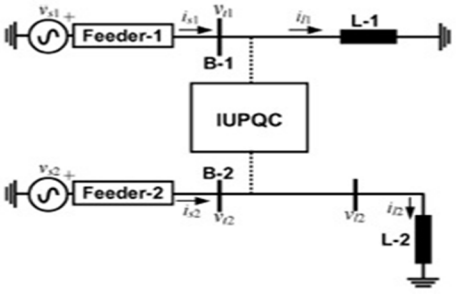

Fig 1. Single-line diagram of an IUPQC connected distribution system

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Two feeders, Feeder-1 and Feeder-2, which are connected to two different substations, supply the system loads L-1 and L-2. The supply voltages are denoted byV_{s1} and V_{s2} It is assumed that the IUPQC is connected to two buses B-1 and B-2, the voltages of which are denoted by V_{t1} and V_{t2} respectively. Further two feeder currents are denoted by i_{s1} and i_{s2} while the load currents are denoted by i_{l1} and i_{l2}. The load L-2 voltage is denoted it1 and i_{t2} by v_{t2}. The purpose of the IUPQC is to hold the voltages V_{t1} and V_{t2} constant against voltage sag/swell, temporary interruption in either of the two feeders. It has been demonstrated that the IUPQC can absorb power from one feeder (say Feeder-1) to Hold V_{t2}. constant in case of a sag in the voltage V_{s2}This can be accomplished as the two VSCs are supplied by a common dc capacitor. The dc capacitor voltage control has been discussed here along with voltage reference generation strategy. Also, the limits of achievable performance have been computed.

II. PROPOSED CONCEPT

A. *Circuit Configuration*

The single-line diagram of a distribution system with an IUPQC is shown in Fig. 1.

As shown in this figure, two feeders connected to two different substations supply the loads L11, L12 and L2. The IUPQC is connected to two buses BUS1 and BUS2 with voltages of Vs1 and Vs2, respectively. The shunt part of the IUPQC is connected to loads L11 and L12 with a current of il11 and il12. Supply voltages are denoted by Vs1 and Vs2 while load voltages are Vl1 and Vl2. Finally, feeder currents are denoted by is1 and is2.

Load currents are Il11; Il12 and Il2 Bus voltages Vt1 and Vt2 are distorted and may be subjected to sag/swell. The load L11 is a sensitive load and load L12 is nonlinear load which needs a pure sinusoidal voltage for proper operation while its current is non sinusoidal and contains harmonics. The load L2 is a sensitive/critical load which needs a purely sinusoidal voltage and must be fully protected against distortion, sag/swell, and interruption. These types of loads primarily include production industries and critical service providers, such as medical centres, airports, or broadcasting centres where voltage interruption can result in severe economical losses or human damages.

B. *IUPQC Structure*

The internal structure of the IUPQC is shown in Fig. 2. It consists of two Voltage Source Converters (VSC1, and VSC2) which are connected back to back through a common dc-link capacitor. In the proposed configuration, VSC1 is connected in shunt with BUS1 with load L11 and Load L12 at the end of Feeder1 and VSC2 is connected in series with Bus 2 with load L2 at the end of Feeder2. Each of the two Voltage Source Converters in Fig. 2 is realized by a three-phase converter with a commutation reactor and output filter as shown in Fig. 3. The commutation reactor is connected at the output filter to prevent the flow of switching harmonics into the power supply. As shown in Fig. 2, all converters are supplied from a common dc-link capacitor and connected to the distribution system through a transformer. Secondary

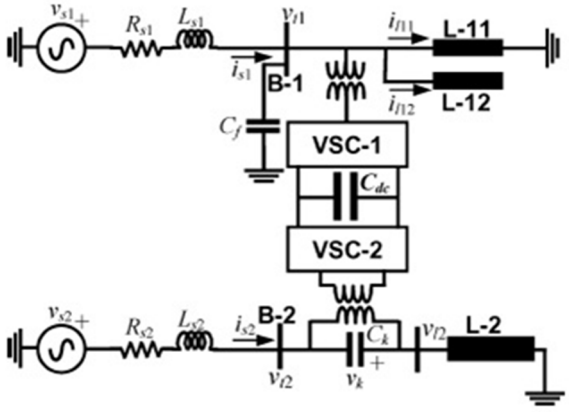

Fig2. Typical IUPQC connected Distribution System

(Distribution) sides of the series-connected transformers are directly connected in series with BUS1 and BUS2, and the secondary (distribution) side of the shunt-connected transformer is connected in parallel with load L1. The aims of the MC-UPQC shown in Fig. 2 are to regulate the load voltage against sag/swell and disturbances in the system to protect the

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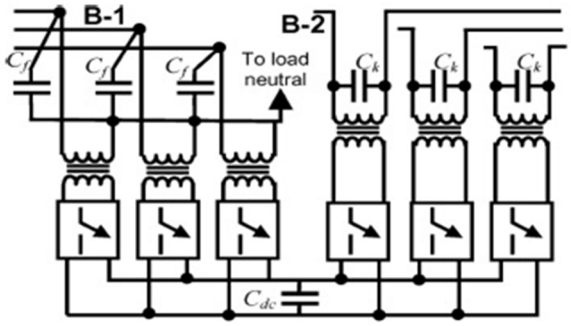

Fig3. Schematic Structure of VSC

Nonlinear/sensitive load L1 and the load voltage against sag/swell, interruption, and disturbances in the system to protect the sensitive/critical load L2 and to compensate for the reactive and harmonic components of nonlinear load current.

TABLE I
SYSTEM PARAMETERS

System Quantities	Values
System Fundamental Frequency	50Hz
Voltage source Vs1	11Kv(L-L, rms), Phase angle 0^0
Voltage source Vs2	11Kv(L-L, rms), Phase angle 0^0
Feeder-1 (rs1+2πfLs1)	Impedance: 6.05+j36.28Ω
Feeder-2 (rs2+2πfLs2)	Impedance: 3.05+j18.14Ω
Load L-1 1 Unbalanced RV Component	Phase a: 24.2+j60.50Ω Phase b: 36.2+j78.54Ω Phase c: 48.2+j94.25Ω
Load L-1 2 Non Linear Component	A Three phase diode rectifier that supplies a load of 3.05+j18.14Ω
Balanced Load L-2 Impedance	72.6+j54.44Ω

In order to achieve these goals, series Voltage Source Converter (VSC1) operate as voltage controllers while the shunt VSC (VSC2) operates as a current controller.

C. Control Strategy

As shown in Fig. 2, the MC-UPQC consists of two series VSCs and one shunt VSC which are controlled independently. The switching control strategy for series VSCs and the shunt VSC are selected to be sinusoidal pulse width-modulation (SPWM) voltage control and hysteresis current control, respectively. Details of the control algorithm, which are based on the method [12], will be discussed later. Functions of the shunt-VSC are to compensate for the reactive component of load L11 and L12 currents

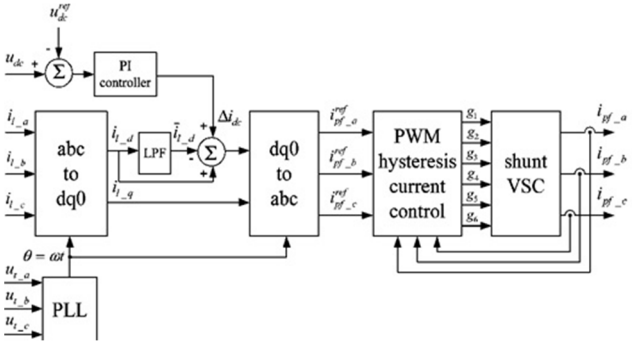

Fig.4. Control block diagram of the shunt VSC.

And to compensate for the harmonic components of load L12 current and to regulate the voltage of the common dc-link capacitor. Fig. 4 shows the control block diagram for the shunt VSC.

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The measured load current is transformed into the synchronous reference frame by using

$$il_{dq0} = T_{abc}^{dq0} \cdot i_{l-abc} \qquad (1)$$

Where the transformation matrix is

$$T_{abc}^{dq0} = \frac{2}{3}\begin{bmatrix} \cos(wt) & \cos(et - 120^0) & \cos(wt + 120^0) \\ -\sin(wt) & -\sin(wt - 120^0) & -\sin(wt + 120^0) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} (2)$$

By this transformation, the fundamental positive-sequence component, which is transformed into dc quantities in the *d* and *q* axes, can be easily extracted by LC filters. Also, all harmonic components are transformed into ac quantities with a fundamental frequency shift.

$$i_{l-d} = \bar{\imath}_{l-d} + \hat{\imath}_{l-d} \qquad (3)$$

$$i_{l-q} = \bar{\imath}_{l-q} + \hat{\imath}_{l-q} \qquad (4)$$

If i_l is the feeder current and i_{pf} is the shunt VSC current and knowing as $i_s = i_l - i_{pf}$, then d-q components of shunt VSC reference current are defined as follows

$$i_{pf-d}^{ref} = i_{l-d} \qquad (5)$$

$$\hat{\imath}_{pf-q}^{ref} = i_{l-q} \qquad (6)$$

Consequently, the *d-q* components of the feeder current are

$$i_{s-d} = \check{\imath}_{l-d} \qquad (7)$$

$$i_{s-q} = 0 \qquad (8)$$

This means that there are no harmonic and reactive Components in the feeder current. Switching losses cause the dc-link capacitor voltage to decrease.

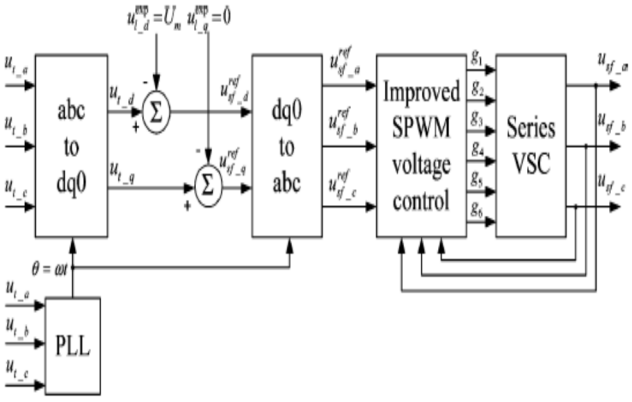

Fig.5.Control block diagram of the series VSC

Disturbances, such as the sudden variation of the load, can also affect the dc link. In order to regulate the dc-link capacitor voltage, a proportional-integral (PI) controller is used as shown in Fig. 4. The input of the PI controller is the error between the actual capacitor voltage (u_{dc}) and its reference value(u_{dc}^{ref}). The output of the PI controller (i.e.,Δi_{dc}) is added to the *d* component of the shunt-VSC reference current to form a new reference current as follows:

$$\begin{Bmatrix} i_{pf-d}^{ref} = \check{\imath}_{l-d} + \Delta i_{dc} \\ i_{pf-q}^{ref} = i_{l-q} \end{Bmatrix} \qquad (9)$$

As shown in Fig. 4, the reference current in(9) is then transformed back into the *abc* reference frame. By using PWM hysteresis

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current control, the output-compensating currents in each phase are obtained

$$i_{pf-abc}^{ref} = T_{dq0}^{abc}\, i_{pf-dq0}^{ref}, \left(T_{dq0}^{abc} = T_{abc}^{dq0-1}\right) \qquad (10)$$

Series-VSC: Functions of the series VSCs in each feeder are to mitigate voltage sag and swell and to compensate the voltage distortion, such as harmonics and small interruption in Feeder (In Feeder2 Only).

The control block diagram of each series VSC is shown in Fig5. The bus voltage is detected and then transformed into the synchronous *dq0* reference frame using

$$u_{t-dq0} = T_{abc}^{dq0}\, u_{t-abc} = u_{t1p} + u_{t1n} + u_{t10} + u_{th} \quad (11)$$

Where

$$u_{t1p} = [u_{t1pd} \quad u_{t1pq} \quad 0]^T$$

$$u_{t1n} = [u_{t1n-d} \quad u_{t1n-q} \quad 0]^T$$

$$u_{t10} = [0 \quad 0 \quad U_{00}]^T$$

$$u_{t1h} = [u_{th-d} \quad u_{th-q} \quad u_{th-0}]^T \qquad (12)$$

u_{t1p}, u_{t1n} and u_{t1n} are fundamental frequency positive-, negative-, and zero-sequence components, respectively, and is the harmonic component of the bus voltage.

According to control objectives of the MC-UPQC, the load voltage should be kept sinusoidal with constant amplitude even if the bus voltage is disturbed. Therefore, the expected load voltage in the synchronous *dq0* reference frame u_{t-dq0}^{exp} only has one value

$$u_{t-dq0}^{exp} = T_{abc}^{dq0}\, u_{i-abc}^{exp} = \begin{bmatrix} u_m \\ 0 \\ 0 \end{bmatrix} \qquad (13)$$

Where the load voltage in the *abc* reference frame is

$$u_{i-abc}^{exp} = \begin{bmatrix} u_m \cos(wt) \\ u_m \cos(wt - 120^0) \\ u_m \cos(wt + 120^0) \end{bmatrix} \qquad (14)$$

The compensating reference voltage in the synchronous *dq*0 reference frame is defined as

$$u_{sf-dqo}^{ref} = u_{t-dq0} - u_{i-dqo}^{exp} \qquad (15)$$

This means u_{t1p} in equation (12) should be maintained at while all other unwanted components must be eliminated. The compensating reference voltages in (15) are then transformed back into the *abc* reference frame.

By using an improved SPWM voltage control technique (since PWM control with minor loop feedback) [8], the output compensation voltage of the series VSC can be obtained.

D. Multi-Level Converter

Using the Multi level converter in the Interline Unified Power Quality Conditioner we can attain better power quality free of ripples and DC in AC content. Multi level converters use components of low rating to serve medium rated applications to reduce the overall cost. The performance of a converter with any switching strategies can be related to the harmonics contents of its output voltage. Based on converter topology they are divided into three types:

1) Diode clamped multilevel converter.
2) Flying capacitor multilevel converter.
3) Cascaded multilevel converter.

Cascaded multilevel converters are based on a series connection of several single phase converters. This structure is capable of reaching medium output voltage levels using only standard low voltage components. A basic structure of a cascaded MLI is shown in fig. 5.

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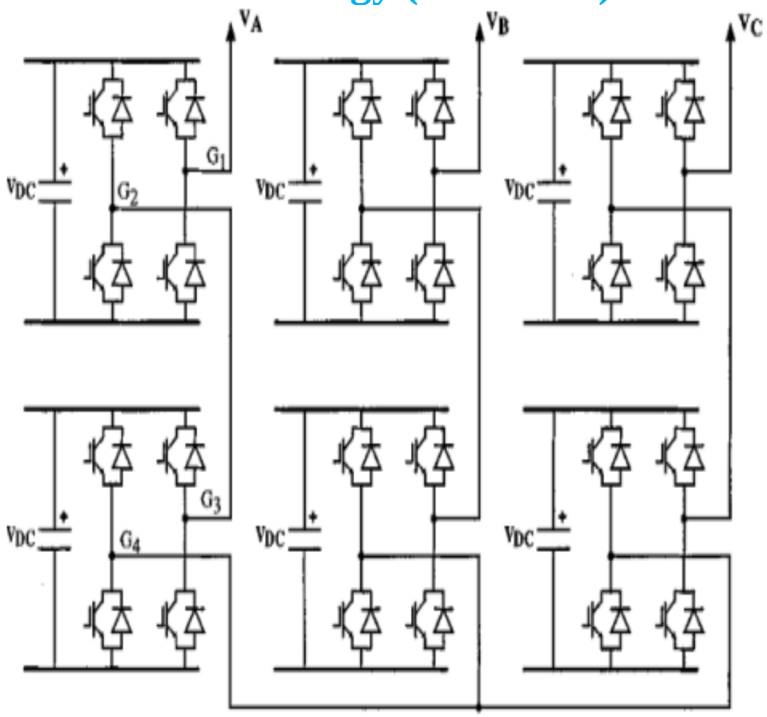

Fig5. Three Phase H-Bridge Cascaded Multi Level Converter

Each inverter used a dc-link voltage to generate a modulated voltage at the output terminals. The total output voltage is obtained by the sum of each individual output voltage is obtained by the sum of each individual output voltage. Three phase voltage output from a Multi-Level Converter is shown in Fig. 5.

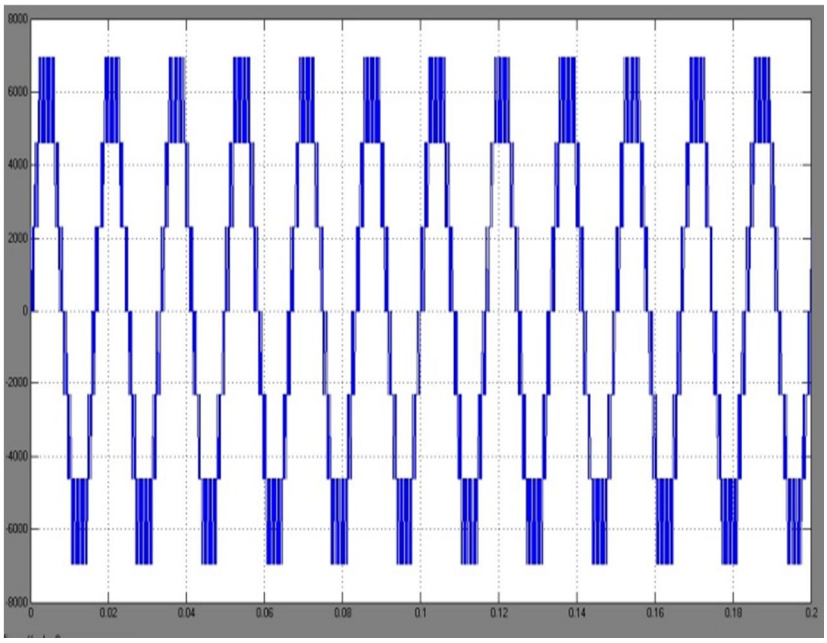

Fig 6. Multi-level Converter Seven level Pulse Signals

A phase shift sinusoidal pulse width modulation (PS-SPWM) switching is proposed for MOSFETs in the Multi level Converters. Optimal harmonic cancellation is achieved by phase shifting each carrier by (k-1) π/n, where k is the k_{th} inverter. Where n = (L-1)/2 is the number of series connected single phase inverters. L is the number of switched DC levels that can be achieved in each phase leg.

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III. ANALYSIS OF IUPQC AND SIMULATION RESULTS

The simulation Circuit of the Interline Unified Power Quality Conditioner is shown as the

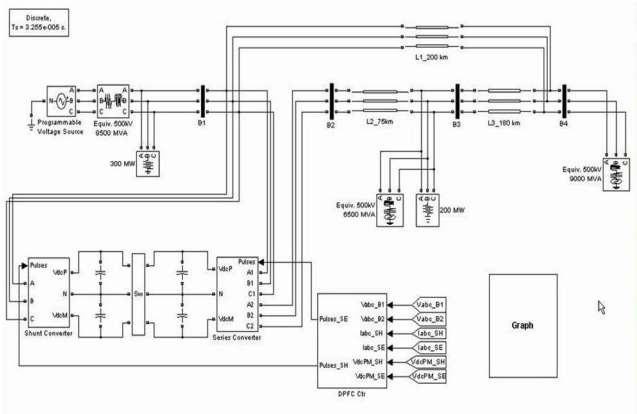

Fig 7. Simulation Circuit of the IUPQC with multi level converter

This circuit is taken with the Unified Power Quality Conditioner system with the two feeder basis and by we take the two lines as such a way we can take specific problem rectification in the specified areas rather than focus on the whole systems problems at the same time. We can increase the efficiency of the UPQC through interline connection process and by we can achieve the wonderful controlling over power in the distribution system.

The Interline Unified Power Quality Conditioner is processed with the Multi level Converter as to reduce the ripple content and reactive power in the feeder systems and to reduce the DC in AC contents with this circuit construction.

A. Simulation Results

This paper describes the power quality issues majorly on the distribution system and problem solving using the power electronics devices. As such a way we take the problematic situation in the distribution systems is shown as the below

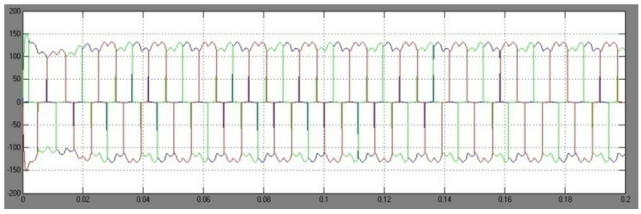

Fig 8(a). Linear loads effective currents in the feeder

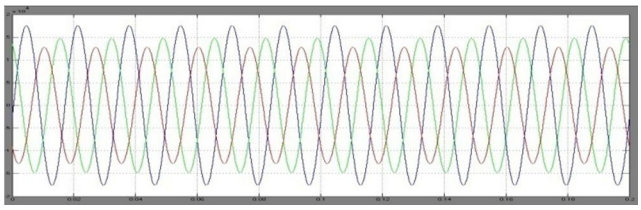

Fig 8(b). Unbalanced loads effective voltages in the feeder

Here we have the source side effective ness of the voltage and current values with the deviated and effective voltages and currents in the source side with this fascinating deal. And thus we have bus 1 and bus 2 voltage and currents respectively

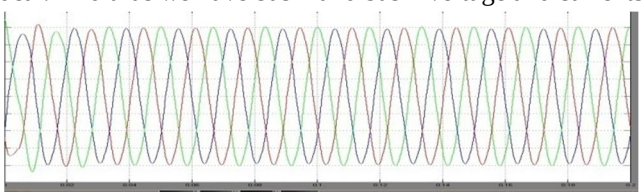

Fig 9(a). Bus 1 Source Voltage

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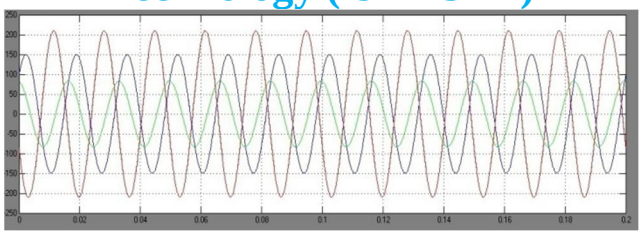

Fig 9(b). Bus 1 Source Current

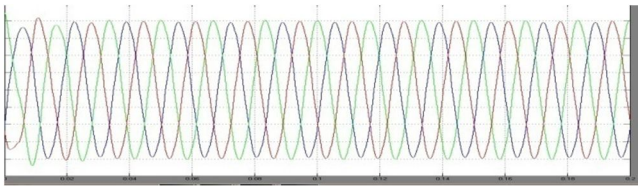

Fig 9(c). Bus 2 Source Voltage

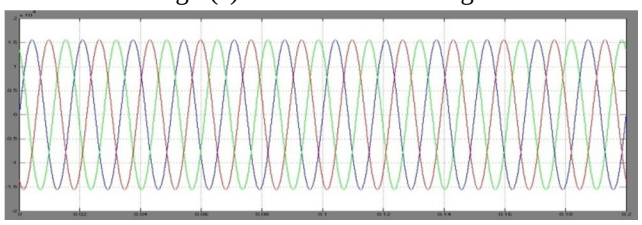

Fig 9(d). Bus 2 Source Current

1) *Linear Unbalanced load:* Linear Unbalanced are most frequently used loads ion the power system we have the linear R-L-C load with unbalanced condition on the systems with the unbalanced currents and voltages on the feeder. The respective plots are given as below

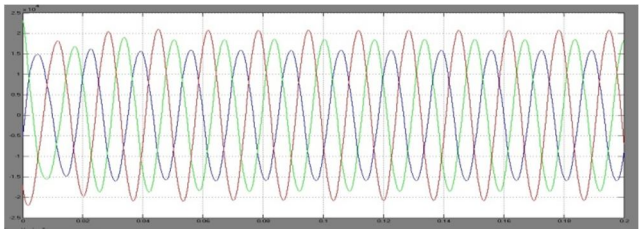

Fig 10(a). Bus 1 linear Unbalanced load voltage

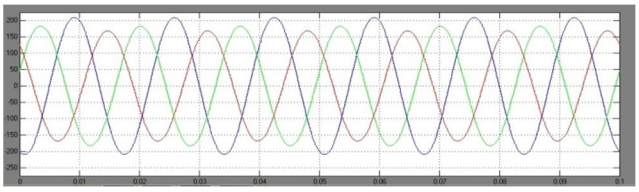

Fig 10(b). Bus 1 linear Unbalanced load currents

2) *Non Linear Loads:* Here we have the major fluctuating loads majorly used in the consumer localities and cause major power quality issues such as harmonic distortion and reactive power generation and also voltage fluctuations as such a way resulting waveform are give as below

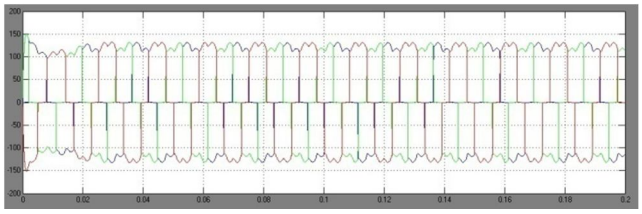

Fig 10(c). Bus 1 Non Linear load currents(before application of IUPQC)

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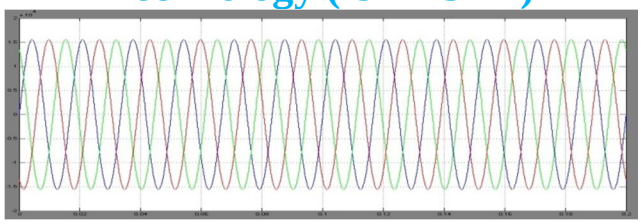

Fig 10(d). Source side corrected bus 1 current

3) *Sensitive Loads:* This part of the paper discuss about the sensitive loads which are the most fluctuating loads in the distribution system which are easily effected by the power deviations and harmonic distortions and to are to maintained in a good power regulation to keep the devices in a good conditions

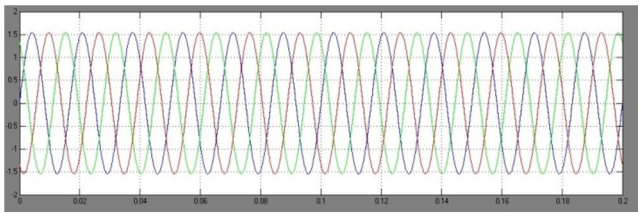

Fig 10(e). Bus 2 Sensitive Load currents

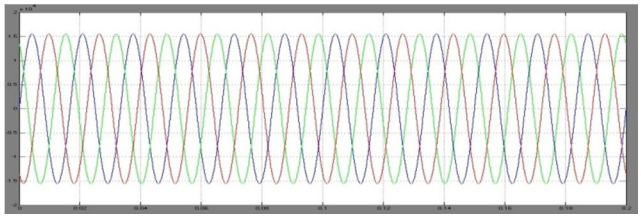

Fig 10(f). Bus 2 Sensitive load voltages

The DC link Voltage of Interline Unified Power Quality Conditioner is give as below,

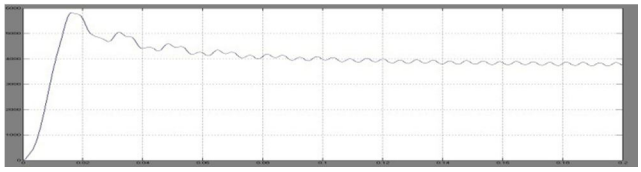

Fig 10(g). DC Link Voltage

Thus we take the problems in the distribution system and reduce the effect and causing good power quality in the system with our Interline Unified Power Quality Conditioner as to make our distribution system provides the good quality of power to our consumers and to get the system to the stability. As in the systems we control the total harmonic distortion factor from percentage from the 16% to 5% of THD values in the simulation using IUPQC

The simulation results for the Interline Unified Power Quality Conditioner BUS1 voltage with series compensation voltage, and load voltage in feeder 1 are shown in Figure 9. The simulation results show that the voltage sag, swell, fluctuations and distortions of BUS1 voltage are compensated for by injecting the proper series voltage. In this figure, the load voltage is a three-phase sinusoidal balance voltage with regulated amplitude. In the same way BUS2 current with shunt compensation current, and load current in feeder 2 are shown in Figure 9. The simulation results show that the harmonic components and current harmonic distortions of BUS1 current are compensated for by injecting the proper shunt current. In this figure, the load current is a three-phase sinusoidal balance voltage with regulated amplitude

IV. CONCLUSION

This paper describes a new connection for a Interline unified power quality conditioner (UPQC) to improve the power quality of two feeders in a distribution system. It is demonstrated how this device is connected between two independent feeders to regulate

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the bus voltage of one of the feeders while regulating the current across a load in the other feeder. And as by using multi level converter in the IUPQC we are able to control the ripple content and DC in the AC content in the IUPQC system and as by increasing the efficiency of the device such that improving the power quality in the feeders. From the result, it can be concluded that, whenever there is a voltage swell in either of the feeders, one feeder readily compensates for the other. Total harmonic compensation of the feeder also can be controlled from 5.2%. The structure, control and capability of the IUPQC have been discussed in this paper. The efficiency of the proposed configuration has been verified through simulation studies using Mat lab.

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BIOGRAPHIES

N. Bharath Kumar received his B. Tech degree in Electrical & Electronics Engineering from Dhanekula Institute of Engg & Tech (Ganguru) in 2014 and (M. Tech) in Power Electronics From MIC college of Science and Tech, Kanchikacharla.

B.R. Narendra M.tech is currently working as Associate professor in MIC College of Science and Tech, Kanchikacharla.

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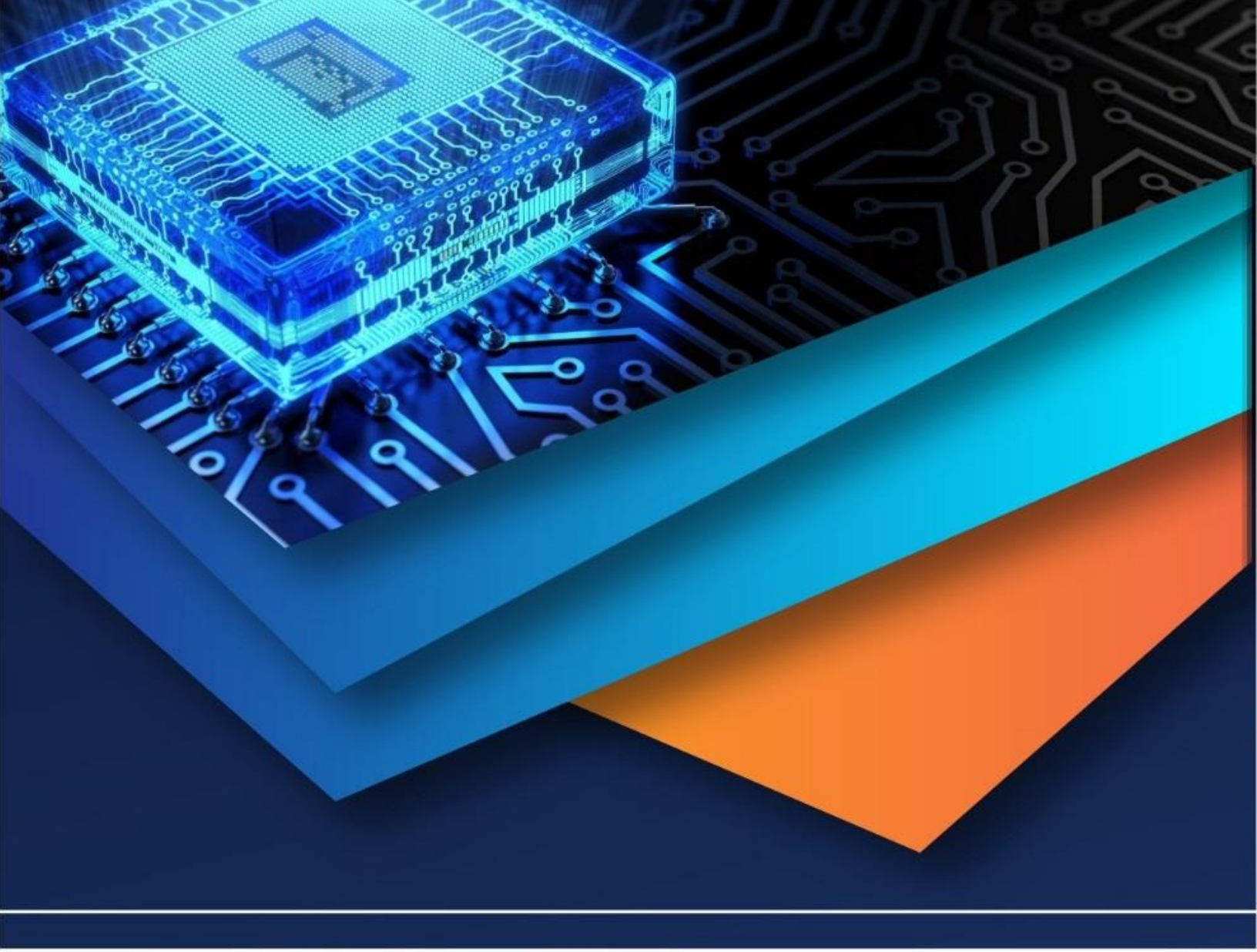

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