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Analysis of Different Types of Domino Logic: A Review

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Abstract—Power and area will remain the main constraints in the designing of VLSI circuits. Dynamic CMOS logic circuits are broadly designed for high performance circuits due to their high speed. Conversely, the demerit of dynamic logic style is its high noise sensitivity. The main cause of this is the sub-threshold leakage current flowing through the pull down network and with continuous technology scaling, this problem is getting more and more severe. Compared to static CMOS circuits which have larger capacitance and offers more delay , Dynamic circuits are used to reduce those parameters of design. In that area lot of work has been done to improve the noise immunity and to make more power efficient without sacrificing the speed of the dynamic circuits. Domino with keeper, Domino with footer and keeper, High speed domino logic, Conditional keeper domino logic and several other techniques have been employed to improve the performance of the domino logic. Simulations were done in cadence earlier in order to visualize the different types of domino logic at different technology nodes and power supply for comparison purpose.

Keywords—domino logic, leakage power, noise immune, wide fan in.

I. INTRODUCTION

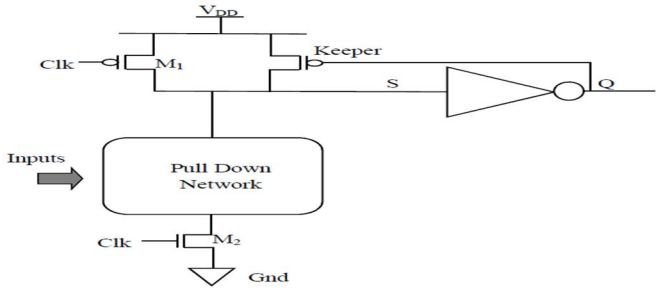
In comparison with static CMOS circuits, dynamic CMOS circuits have various advantages such as less number of transistors, low-power, higher speed, no short-circuit power and glitch-free operation Because of the above properties, high performance systems are realized using dynamic CMOS circuits. With the need of low power and higher speed processors and the use of portable devices have resulted in very fast growth in VLSI circuit designs [1]. In modern VLSI circuits dynamic domino logic is widely used due to its high performance compared to static logic. But the major drawbacks of dynamic logic are high power dissipation and less immunity to noise. As the technology is scaling down continuously, it results in the increase of leakage current which is dependent on parameters like gate oxide thickness, doping profile, channel dimension, sub-threshold conduction, gate oxide tunneling, and reverse bias junction. And as a result of this, the lower noise margin and higher static power dissipation becomes the dominant factors in the design of VLSI circuits and for the high fan-in dynamic OR gates. Wide fan-in OR gates play an important role in microprocessors so to achieve higher performance operation.

II. TYPES OF DOMINO LOGIC

In recent years, different logic styles have been proposed to implement domino logic which can be further used to implement several circuits including the memory designs, wide-fan in OR gates .In this paper brief discussion of various domino logic styles having least efficient designs to high efficient designs have been discussed.

A. Conventional domino logic

In conventional domino logic, a keeper transistor is utilized so as to provide feedback for retaining the state of the dynamic node [2]. But the contention that results between the keeper and pull down network reduces the power and speed characteristics of the circuit. This has been shown in fig.(a):-



Fig(a) Conventional domino logic

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B. Footless domino logic(FLD)

Conventional domino logic achieves better immunity to noise due to the stacking effect when compared to footless domino style . To achieve the improvement in robustness of the Conventional domino circuits, keeper upsizing can be done[1][2]. But upsizing of keeper transistor results in contention between dynamic node and pull down network(PDN) which increases power consumption and delays during evaluation period.

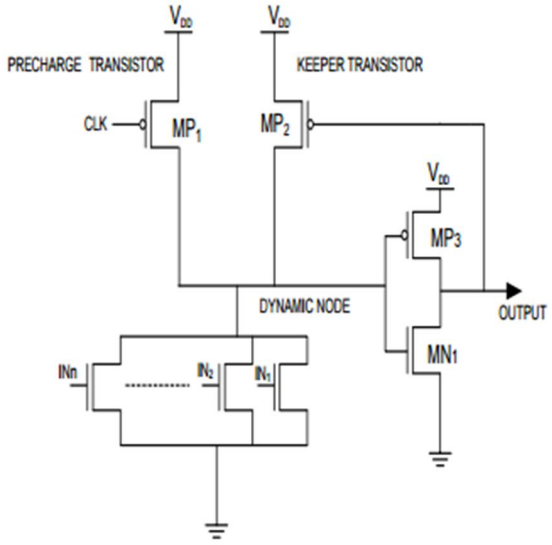
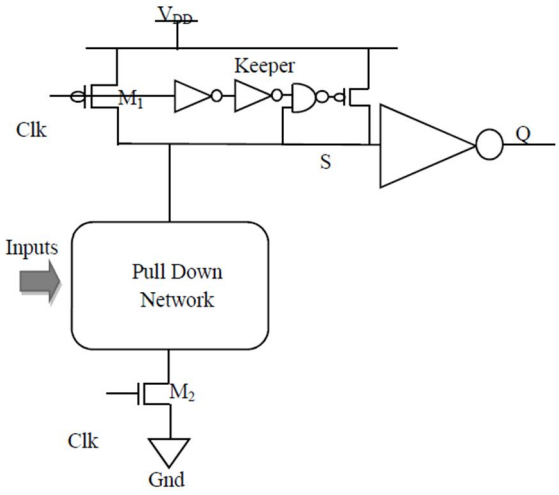


Fig (b) Footless Domino Logic

C. Conditional keeper domino logic(CKD)

When we design a high fan-in gates In deep sub-micron technology the Leakage current associated with that Design is quite significant therefore there is a need of strong keeper that will compensate for the loss of charge[2], although these types of strong Keepers have contention problem but are quite good for the circuits in noisy in environments when gate inputs are not protected[5].



Fig(c) Conditional keeper domino logic

D. High speed domino logic(HSD)

This logic further minimizes the contention between the pull-down network and keeper by having only strong keeper operating that increases the speed but at the cost of increased power consumption and lesser noise immunity compared to conventional keeper domino[4][5].

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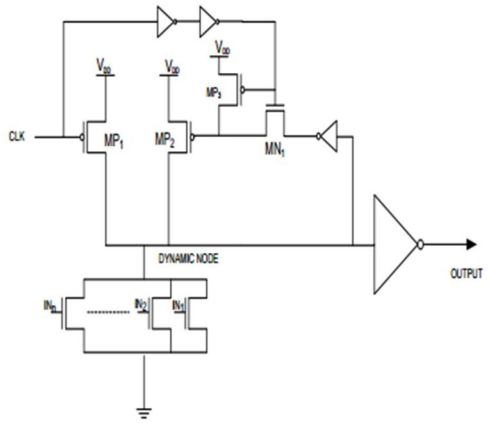


Fig (d) High speed domino logic

E. Diode footed domino logic

The diode footer (M1) results in lowering the sub threshold leakage by the use of stacking effect[14] . But there is performance degradation due to presence of diode footer that's why the mirror transistor [M2] is used that increases the performance characteristics[7].

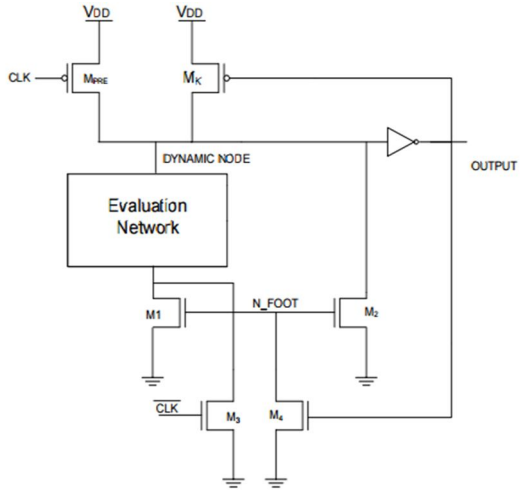
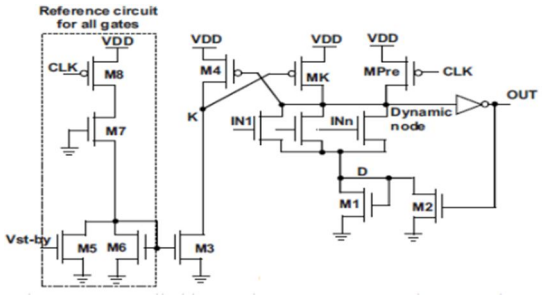


Fig (e). Diode footed domino logic

F. Controlled keeper by current comparison domino(CKCCD)

The above proposed technique makes domino circuits more robust and with less leakage and without significant performance degradation in terms of power consumption. This technique compares reference current with pull down network current[10] and when there is no conducting path from dynamic node to ground and only current in the PDN is the leakage current.



Fig(f) Controlled Keeper by current comparison based domino

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G. Current comparison domino(CCD)

In the CCD circuit, the current of the Pull up network is mirrored by transistor M2 and compared with the reference current, which replicates leakage current of Pull up network. The topology of the keeper transistors and the reference circuit, which is shared for all gates, which successfully tracked the process, voltage and temperature variations[11]. The CCD circuit employs pMOS transistors to implement logical function, as shown in figure (h). This circuit is similar to Replica Leakage Circuit, in which a series diode-connected transistor M6 similar to M1 has been added. Using the N-well , source and body terminals of the pMOS transistors are tied together such that the body effect is eliminated.

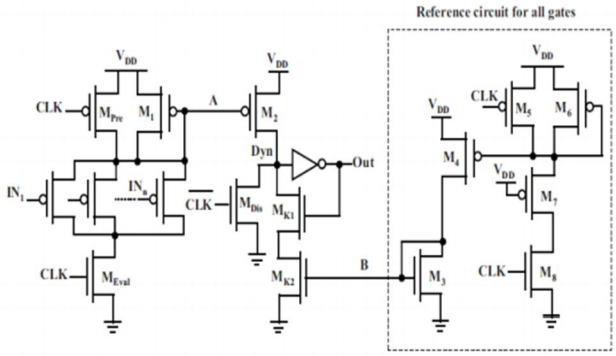

Fig (g) Current comparison domino

H. Dynamic logic using leakage current replica keeper(LCR)

In the case of wide fan-in gates, the capacitance of the dynamic node is large therefore the speed is decreased dramatically. In addition, noise immunity of gates is reduced due to many parallel leakage paths in wide input gates. Although keeper transistor can improve the noise robustness but at the cost of power consumption and delay which gets increased due to large contention[9] . A domino logic that is implemented by Leakage current replica(LCR) keeper uses an analog current mirror to replicate the leaking current of a dynamic pull-down stack and tracks process, voltage, and temperature variations. The proposed keeper has one field-effect transistor per gate plus a portion of a shared current mirror fig(h).

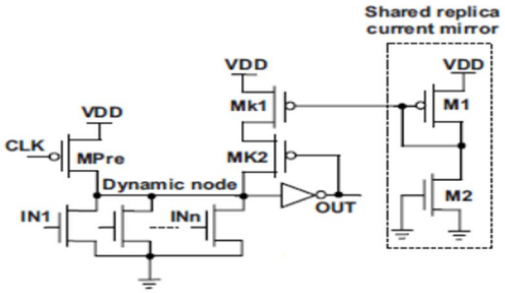

Fig (h) LCR keeper based domino logic

I. High speed domino logic circuit for improved performance

Creating Stacking effect[14] using current mirror circuits is one of the most recently found remedy which helps in a following way that in the below mentioned circuit that if any noise signal occurs at M1 it will be leak to ground via M4 and M5. Transistors M3 and M4 again forms current mirror[12], by using the current mirrors the gate to source voltage decreases to even greater extent. This effect is Known as stacking effect. Therefore the purpose of M4 and M5 in the circuit is to create a stacking effect, which then results in reduction of voltage drop across M2.

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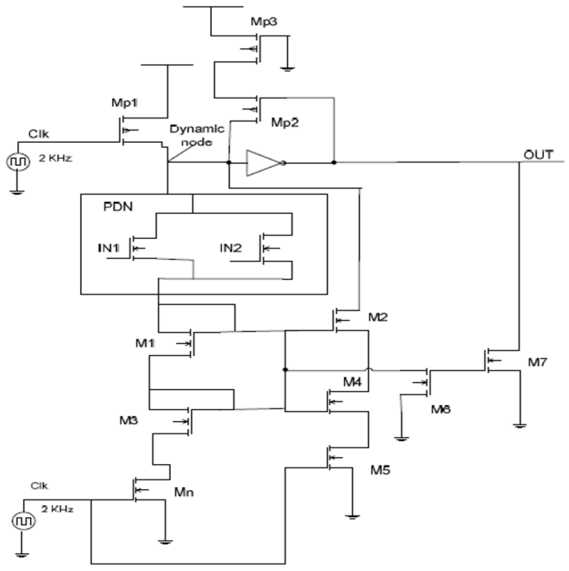

Fig(I) High Speed Domino Logic Circuit for Improved Performance

III. RESULTS

The Table 1 [13] shows the comparison of different domino logics. The Table 2 shows the simulations performed on cadence tool with 90nm technology node for High speed domino logic circuit of fig(I)

TABLE 1. comparison of different domino logics

Parameters	FLD	FD	HSD	CKD	DFD	LCR	CCD
Power(µW)	2.203	2.964	375.49	205.52	3.320	2.259	1.98
Delay(ps)	16.55	29.615	16.152	19.05	27.88	16.91	18.13
Power-delay product(aJ)	36.45	87.64	6064.1	3915.1	92.56	38.19	35.89

TABLE 2(a) Simulations with varying supply voltage

Supply Voltage	1v	0.9v	0.8v	0.7v	0.6v
Power (nW)	333.74	121.66	179.05	73.592	72.895
Delay (ps)	172.88	245.60	441.41	867.73	2046.9
PDP (10^-18)	57.695	29.879	79.036	63.858	149.21

TABLE2(b) Simulations with varying width of transistor

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W of NMOS	PDP (10^-19)
180n	576.95
240n	407.62
300n	322.22
360n	276.03
420n	249.85
480n	234.29

IV. CONCLUSION

New designs were necessary to obtain desired noise robustness because in dynamic logic circuits the evaluation network consumes a lot power in the earlier designs and also there was a problem of leakage power dissipation and these problems became more and more severe as we moved into the nanometer regime and as with the development of wide fan in gates as well . Moreover, increasing the fan-in resulted not only in reducing worst case delay but also increased the contention between the keeper transistor and the evaluation network. The main purpose of above mentioned techniques was to make domino circuits more noise immune and with reduced leakage power dissipation. The recent techniques developed are doing it by comparing the evaluation current of the gate with the leakage current in the current comparison domino circuit technique recently developed and by the use of current mirror circuits to produce stacking effect[14] .

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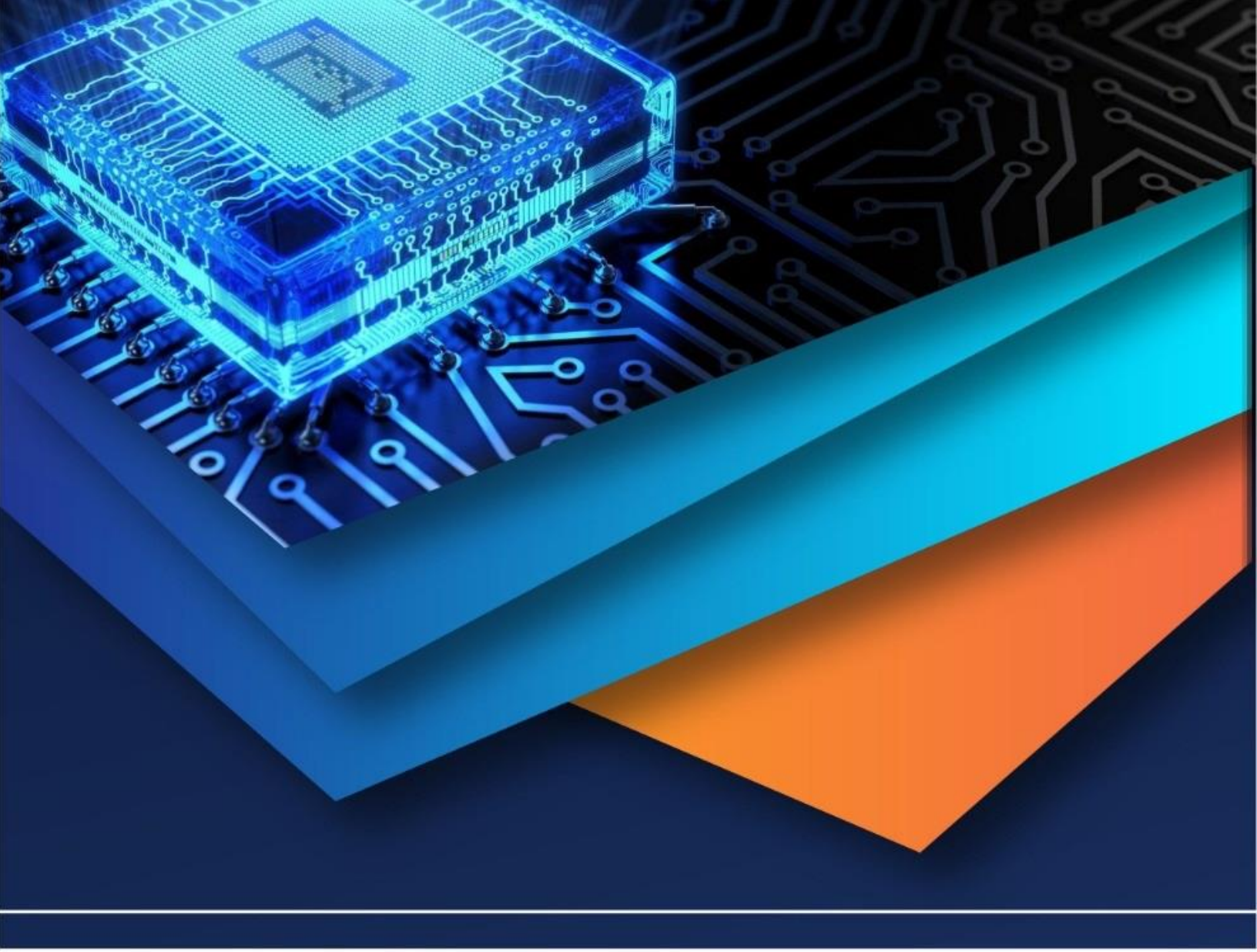

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