



iJRASET

International Journal For Research in
Applied Science and Engineering Technology



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 5 Issue: II Month of publication: February 2017

DOI: <http://doi.org/10.22214/ijraset.2017.2006>

www.ijraset.com

Call: ☎ 08813907089

E-mail ID: ijraset@gmail.com

Design of Five Level Inverter Configuration With Boost Converter in a Photovoltaic System

Prof. B. Anjanee Kumar¹, Neelam Chandra²

Electronics and Telecommunication, RITEE(Raipur Institute of Technology)Raipur,India

Abstract: This paper displays an investigation and an outline of a basic single stage five level inverter for PV applications. The framework is made out of a dc-dc multilevel lift converter which is utilized for producing two voltages at its yield terminal. Furthermore a multilevel inverter reasonable for the created dc transport voltages. The inverter produces five levels at its yield terminal. The proposed topology has the upsides of utilizing less number of segments, less sounds, and high productivity. This is confirmed through reproduction utilizing MATLAB/SIMULINK. The equipment is actualized with multilevel lift converter and multilevel inverter. The outcomes got through reenactment are confirmed with equipment comes about acquired.

Keywords: PV(Photovoltaic), MLI(Multilevel Inverter), MPPT(Maximum Power Point Tracking), P&O(Perturb and Observe), PWM(Pulse width modulation)

I. INTRODUCTION

The interest for renewable vitality has expanded essentially throughout the years in view of lack of fossil fills and nursery impact. Among different sorts of renewable vitality sources, sun powered vitality and wind vitality have turned out to be extremely well known and requesting because of headway in power hardware strategies [1]. Multilevel inverter innovation has risen as of late as a vital option in PV frameworks. Scientists are going ahead to enhance their capacities encourage through upgraded control strategies, and to minimize both segment check and assembling cost [2]. Multilevel inverters began with the impartial point clasped inverter topology [3] [4], and these days a few multilevel topologies have been produced [5] [6] [7], yet as the yield voltage levels builds, it additionally expands the quantity of switches, number of free dc sources, exchanging stresses, misfortunes, voltage unbalancing crosswise over capacitors. This paper proposes a basic structure for changing over DC vitality to AC vitality for PV applications with less number of switches. The proposed topology is appeared in Fig 1.

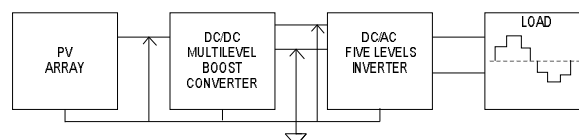


Fig1. Proposed Topology.

Block diagram is composed of the DC source (PV array), the multilevel DC–DC boost converter, the DC–AC (five levels) inverter, and the load. The function of the multilevel DC–DC boost converter is to transfer multilevel DC energy to the inverter from single DC source, whereas that of the inverter is to convert the input levels DC energy into an output AC form.

II. PHOTOVOLTAIC CELL

A PV cell is the fundamental basic unit of the PV module that produces current bearers when daylight falls on it[8]. The power produced by these PV cell is little. To increment the yield control the PV cells are associated in arrangement on the other hand parallel to frame PV module. The equal circuit of the PV cell is appeared in fig: 2. The primary attributes of the PV cell are given by:

$$I = I_{pv} - I_o \left[\exp \left(\frac{q(V + IR_s)}{\alpha KT} \right) - 1 \right] - \frac{V + IR_s}{R_{sh}}$$

$$I_o = I_{o,n} \left(\frac{T_n}{T} \right) \exp \left[\frac{qE_g}{\alpha K} \right] \left(\frac{1}{T_n} - \frac{1}{T} \right)$$

$$I_{pv} = [I_{sc} + K_i(T - T_n)] \frac{G}{G_n}$$

Where,

International Journal for Research in Applied Science & Engineering Technology (IJRASET)

I and V- Cell output current and voltage;

I_0 -Cell reverse saturation current;

T- Cell temperature in Celsius;

K- Boltzmann's constant;

q- Electronic charge;

Ki- short circuit current/temperature coefficient;

G- Solar radiation in W/m²;

G_n-nominal solar radiation in W/m²;

E_g-energy gap of silicon;

I_{0,n}-nominal saturation current;

T_n-nominal temperature in Celsius;

R_s-series resistance;

R_{sh}-shunt resistance;

α-ideality factor between 1.0 to 1.5;

I_{pv}-light generated current.

The I-V normal for a PV module is exceedingly non-straight

in nature. This qualities definitely changes with regard to changes in the sunlight based radiation and temperature. While the sun based radiation for the most part influences the yield current, the temperature influences the terminal voltage. The information of the PV framework utilized as a part of this are taken from msx60i kind of boards.

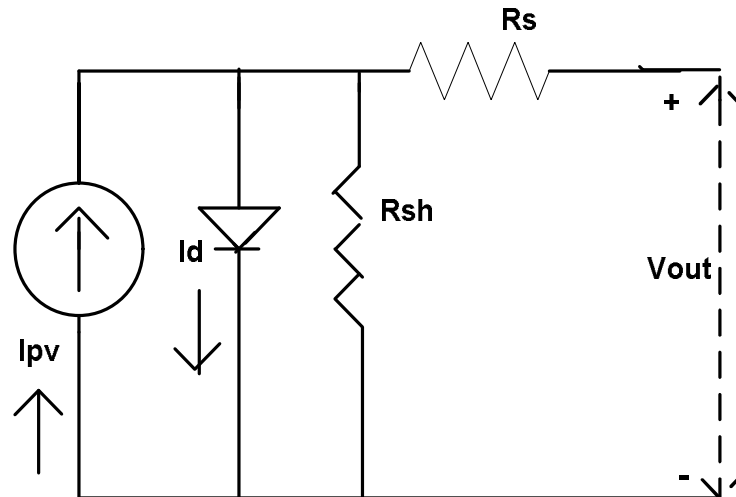


Fig 2. Equivalent circuit of the PV cell.

III. MULTILEVEL BOOST CONVERTER

Fig. 3 indicates two levels boost converter, which depends on one inductor, one switch, 3 diodes and 3 capacitors. It is a boost converter PWM controlled and can keep up a similar voltage in the two yield levels and control the input current. The output voltage can be figured as follows after [8][9]:

$$V_{out} = \frac{N \times V_{in}}{(1-D)}$$

Where,

N- the no. of level

D-the duty cycle

V_{in}-the input voltage

V_{out}-the output voltage

International Journal for Research in Applied Science & Engineering Technology (IJRASET)

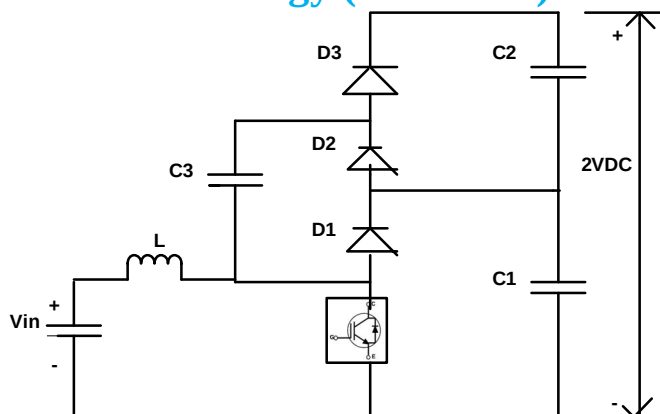


Fig.3 Configuration of 2-Level DC-DC boost converter.

Because of the self adjusted voltage levels, this topology is reasonable to be coordinated with the multilevel inverter. When switch S is conducting, inductor L is charged by input voltage V_{in} . Capacitor C3 is charged by capacitor C1 through D2. Fig 4

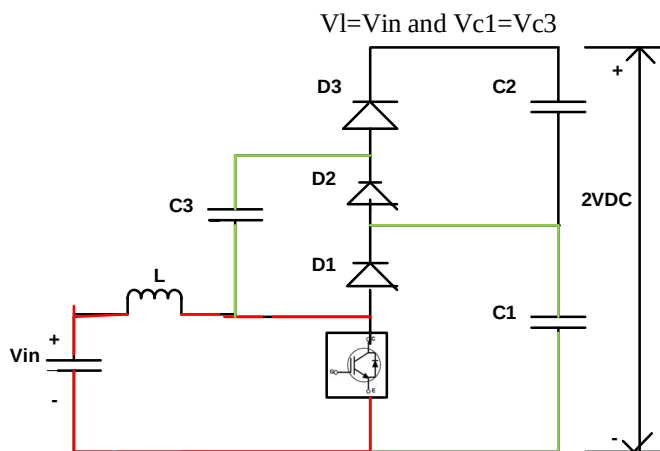


Fig4. Switch-on states.

When S is not conducting, capacitor C1 is charged by input voltage V_{in} and voltage across inductor L through D1. When D3 is forward biased, capacitors C1 and C2 are charged by V_{in} , inductor voltage and voltage across C3 through D3. Fig5

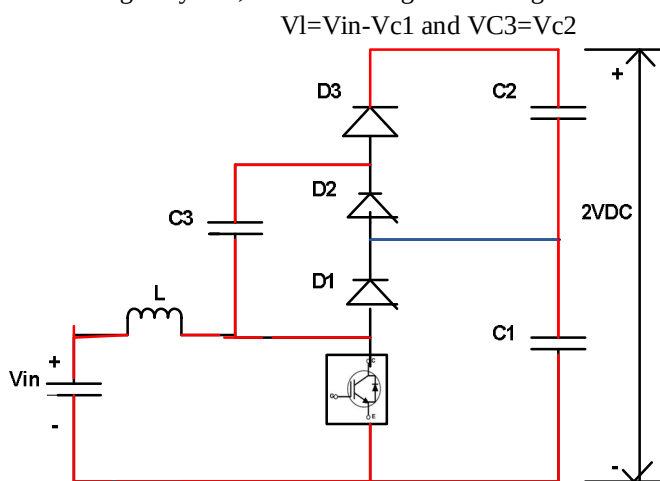


Fig.5 Switch-off states.

International Journal for Research in Applied Science & Engineering Technology (IJRASET)

For a D duty cycle: $V_L \cdot D + V_L \cdot (1-D) = 0$.

From (5) and (6): $V_{in} \cdot D + (V_{in} - V_{c1}) \cdot (1-D) = 0$

$$V_{c1} = V_{dc} = \frac{V_{in}}{(1-D)} \text{ and } 2 \cdot V_{dc} = V_{c1} + V_{c2} = \frac{2 \cdot V_{in}}{(1-D)}$$

IV. MAXIMUM POWER POINT TRACKING

Maximum power point tracking (MPPT) control is compulsory to create greatest power from the PV board and to get great execution when the atmosphere changes (especially light also, temperature) or the Standard Test Condition values digresses. By utilizing this MPPT controller, the obligation cycle is created and is utilized for setting off the lift converter switch. The P&O calculation for MPPT is the most prominent calculation because of its effortlessness and simplicity of execution progressively. The working standard of a P&O MPPT is appeared in Fig. 6 with a flowchart. In P&O, the working point is annoyed occasionally by changing the voltage in PV framework [10]. After every annoyance, the P&O calculation thinks about the estimation of force encouraged from the PV source prior and then afterward the annoyance [11]. In the event that the power has expanded after the bother, the working point moves towards the MPP. After a voltage annoyance, the power drawn from PV diminishes, the working point has been moved far from MPP subsequently the turn around annoyance course is required in the following irritation cycle [11]. The procedure is rehased persistently and the obligation cycle is produced and bolstered to the lift converter. The scientific representation of P&O calculation [12] is given as takes after

$$\frac{dP}{dV_{pv}}(k) = \frac{P(k) - P(k-1)}{V_{pv}(k) - V_{pv}(k-1)}$$

Whenever $\frac{dP}{dV_{pv}} \delta k > 0$ the course moves towards MPP and the voltage must be expanded and $\frac{dP}{dV_{pv}} \delta k < 0$, the voltage must be diminished. Here, $P(k)$ and $P(k-1)$ speak to present power and past figured control, $V_{pv}(k)$ and $V_{pv}(k-1)$ speaks to present and past PV voltage.

Amid the typical operation, the working point consistently differs around the MPP point. Along these lines, the PV framework yield voltage ceaselessly wavers, in this manner, size of bother is vital to keep up the MPP condition as more annoyance size prompts to more swaying [13,14]. Therefore, annoyance voltage step estimate must be picked deliberately. A hypothetical and trial execution of P&O calculation with the framework conduct and reaction are plainly portrayed in [13].

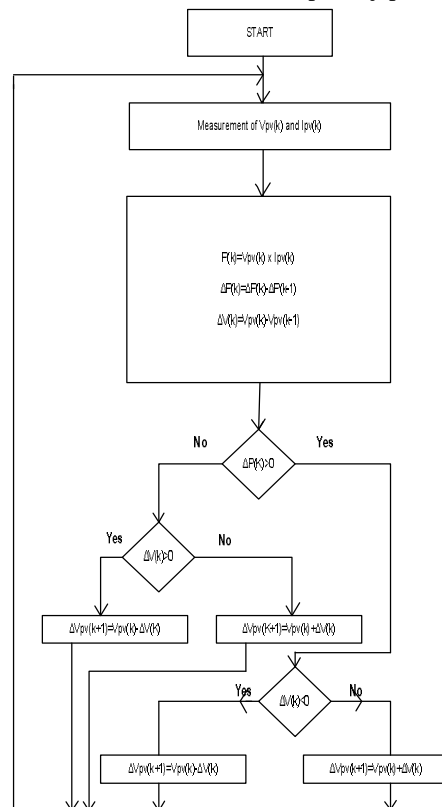


Fig6. Flowchart for perturb and observe maximum power point tracking method.

International Journal for Research in Applied Science & Engineering Technology (IJRASET)

V. PROPOSED SINGLE PHASE FIVE LEVEL INVERTER

The proposed single stage five level inverter appeared in fig 7 altered from [10] [11], comprise of a full-connect (Q1, Q2; Q3, Q4) arrangement with two voltage source (V_{dc} , $2V_{dc}$), and two switches (S1, S2).

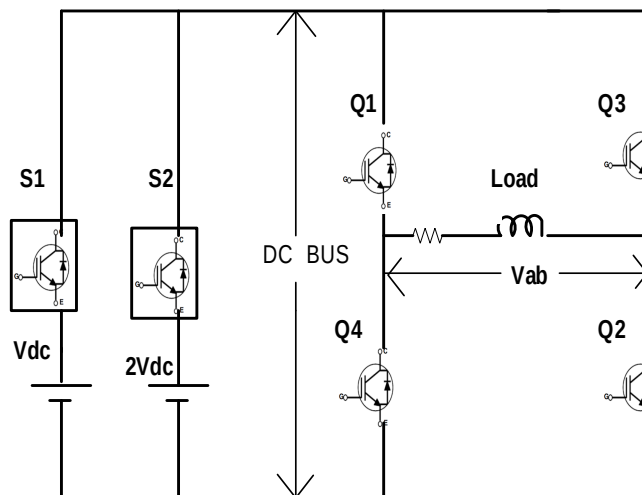


Fig7. Proposed single –phase five- level inverter.

The DC Bus has two states by controlling S1 and S2 with an integral heartbeats. The H-connect inverter is utilized to change over the dc Bus voltage to an air conditioner voltage utilizing customary PWM.

Two strategies have been proposed for getting the exchanging signals for the proposed inverter.

Method1.

In this technique the beat with regulation (PWM) control calculation comprise of two triangular bearer signals indistinguishable to each other with a counterbalance identical to the sufficiency of the triangular transporter flag and having a similar recurrence and are in-stage which contrast and reference flag (which is redressed sinusoidal) as appeared in Fig 8.

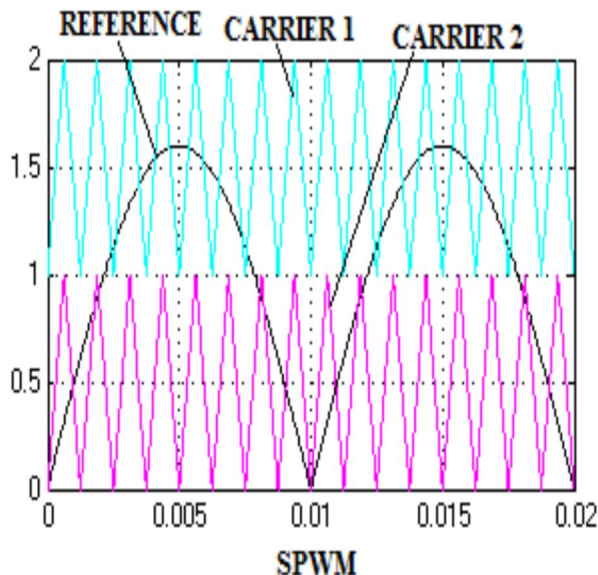


Fig8.First PWM strategy(Method 1)

The second proposed technique can be executed by contrasting four triangular transporter signals indistinguishable with each other with a balance equal to the sufficiency of the triangular transporter flag and having a similar recurrence with reference sinusoidal flag as appeared in Fig 9.

International Journal for Research in Applied Science & Engineering Technology (IJRASET)

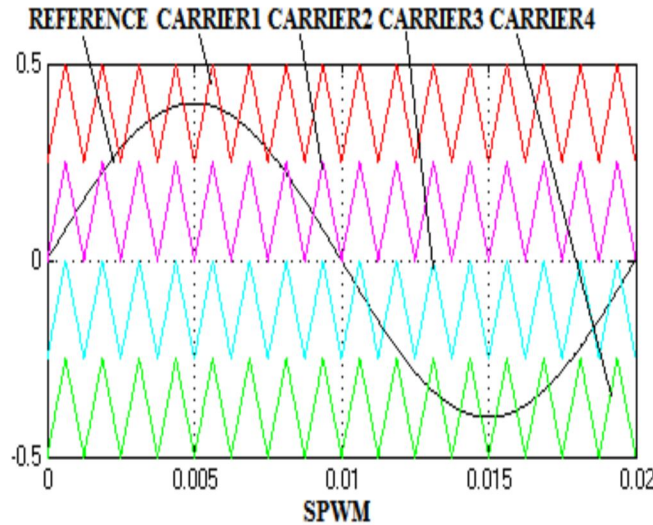


Fig9.Second PWM strategy (Method2)

The main technique brings more effortlessness into the framework. The tweak file for this technique is: $MI = (AM \div 2AC)$. Where AM is the amplitude of reference signal and AC is the amplitude of triangular carrier signal. Table 1 demonstrates the exchanging conditions of switches with comparing voltage level.

SWITCHES STATES						Vab
Q1	Q2	Q3	Q4	S1	S2	
ON	ON	OFF	OFF	OFF	ON	+2Vdc
ON	ON	OFF	OFF	ON	OFF	+Vdc
ON	OFF	ON	OFF	OFF	OFF	0
OFF	ON	OFF	ON	OFF	OFF	
OFF	OFF	ON	ON	ON	OFF	-Vdc
OFF	OFF	ON	ON	OFF	ON	-2Vdc

Table1.Switching patterns of proposed inverter.

VI. SIMULATION RESULTS

The proposed system has been simulated by using MATLAB/SIMULINK with resistance (0.001ohm), snubber resistance R_s (500 ohm), voltage at maximum power point $V_{mp}(V)$ -54.7, duty cycle 0.6. Frequency of output voltage is set to 50Hz. Fig 10 shows the SIMULINK model for the proposed topology. Fig 11 shows the output voltage of Multilevel Inverter. Fig 12 shows the FFT analysis for harmonic component of the output voltage of the inverter. The fig shows THD value of 38.52 of five level output voltage from the sample topology of a single phase five-level inverter with less number of power elements for PV applications.

International Journal for Research in Applied Science & Engineering Technology (IJRASET)

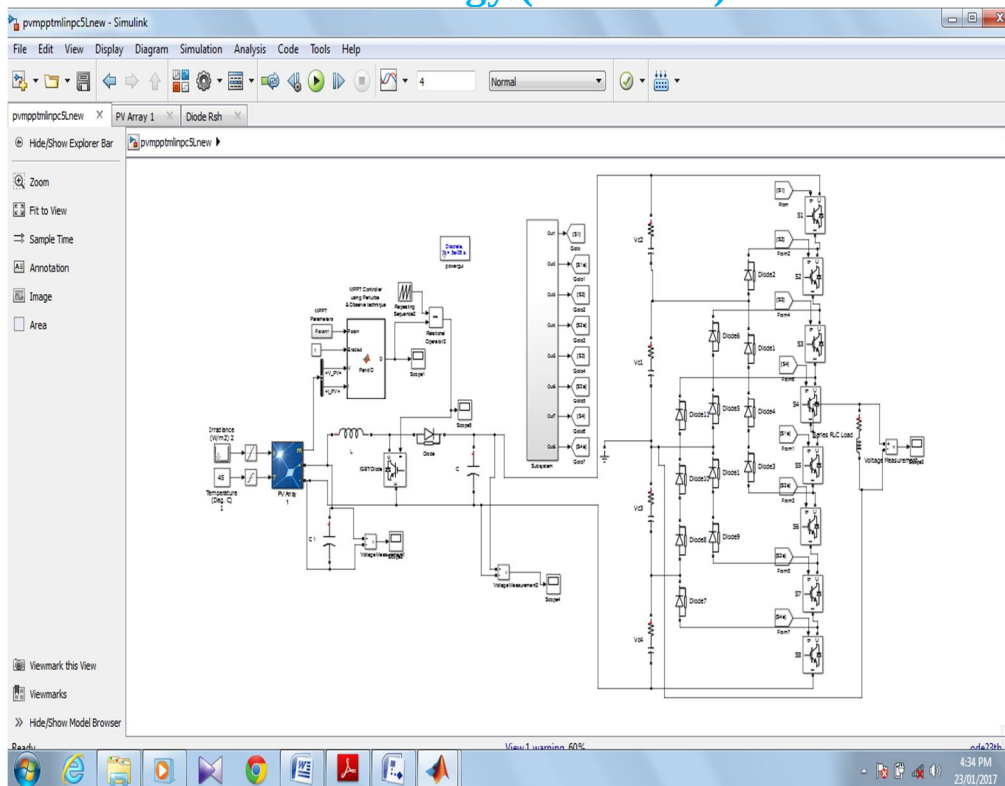


Fig 10. SIMULINK model of the proposed system.

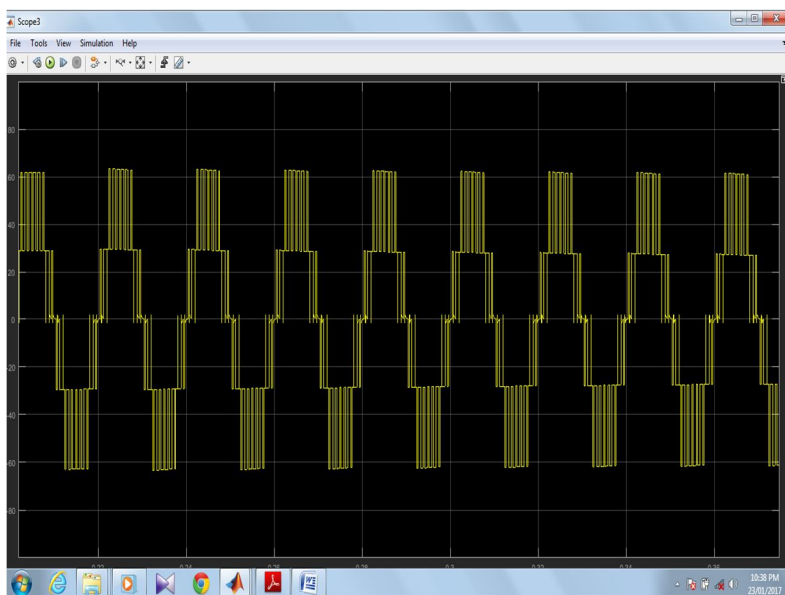


Fig 11. Output Voltage of Multilevel Inverter.

VII. CONCLUSION

This paper manages the outline and usage of single-stage five-level inverter for a resistive and inductive charge. To create a 5-level yield voltage, the proposed multilevel inverter requires a solitary dc voltage source. The PWM control strategy utilized here is extremely basic and aides in decreasing the THD. The outcomes demonstrates that the created multilevel inverter has many merits, for example, lessen number of switches lower EMI, less consonant bending. In this way the proposed inverter can be a decent applicant, which can be utilized as a part of place of traditional PWM inverters in the power rating of a typical utilize.

International Journal for Research in Applied Science & Engineering Technology (IJRASET)

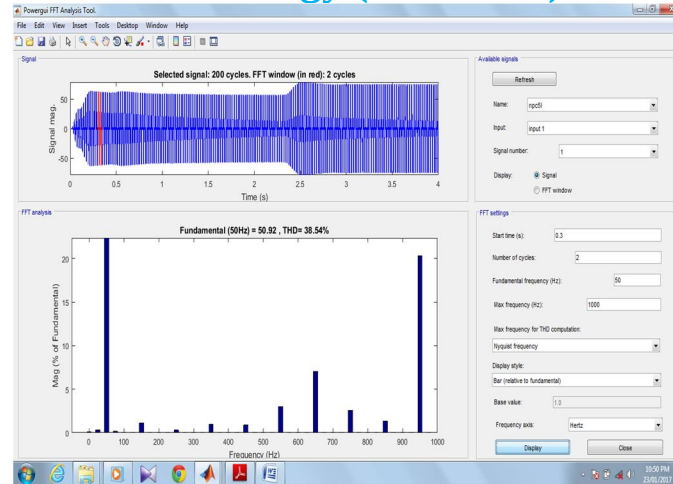
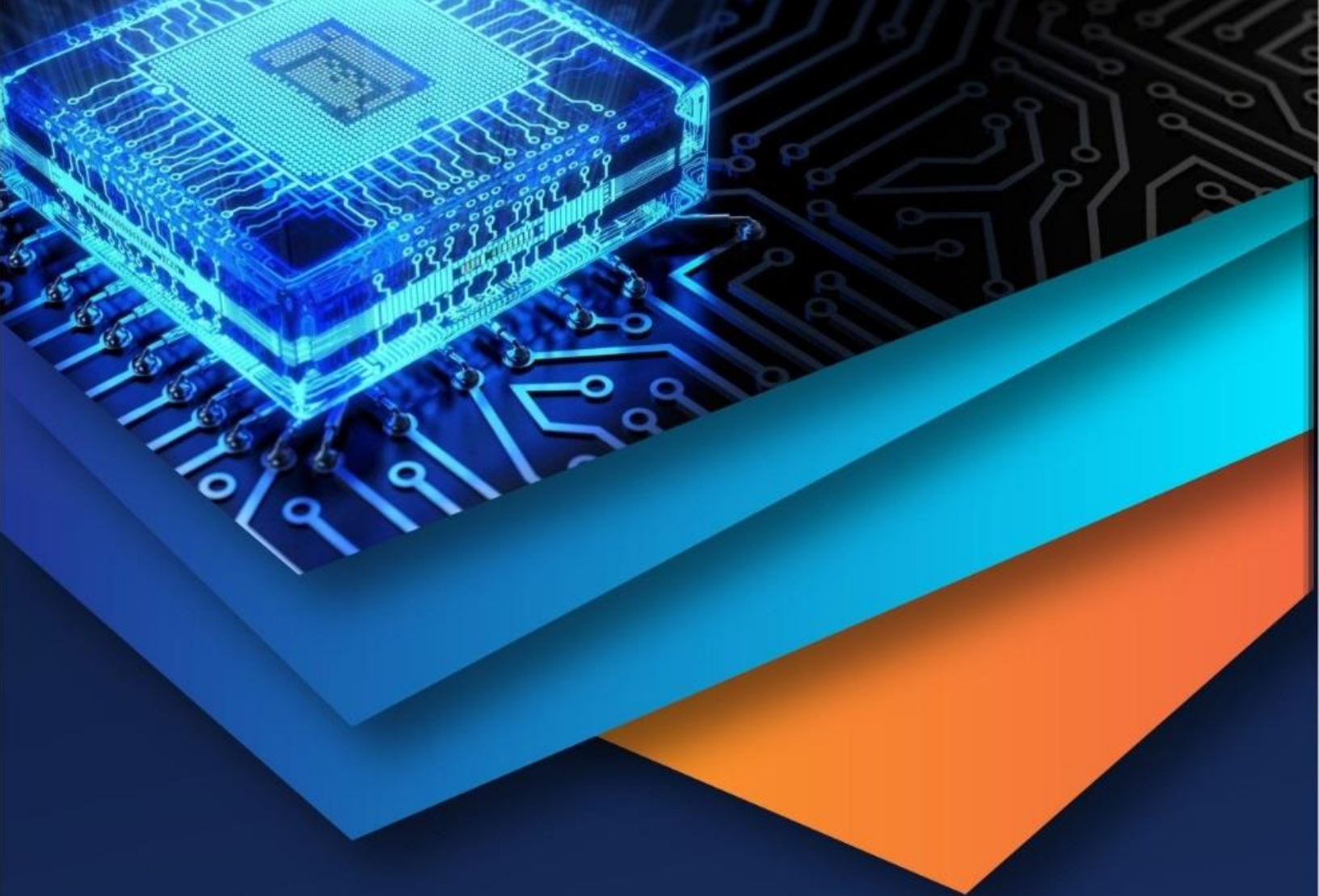


Fig 12. Output voltage THD of the proposed inverter.

REFERENCES

- [1] V.Srimaheswaran, R.Uthirasamy, "Cascaded Multilevel Inverter for pv Cell Application Using PIC Microcontroller," International Journal of Innovative Technology and Exploring Engineering, vol. 2, no. 3, pp.19-24, February 2013.
- [2] C.Veugopal, S.Mathew, "A Single Source Five Level Inverter with Reduced Number of Switches," International Journal of Advanced Research in Electrical Electronics and Instrumentation Engineering, vol.4, no.5, May 2015.
- [3] A.Nabae, I.Takahashi, H.Akagi, "A new neutral-point clamped PWM inverter," Industry Applications, IEEE Transactions, vol.IA-17, no 5, pp.518-523, Sept. 1981.
- [4] G.Gopal, B.Shankaraiah, M.Chinnalal, K.Ganesh, G.Satyanarayana, D. Naik, "A new topology of Single- Phase Seven –Level Inverter with Less Number of Power Elements for Grid Connection," International Journal of Innovative Technology and Exploring Engineering, vol.3, no.4, September 2013.
- [5] M.Pharne, N.Bhosale, "A Review on Multilevel Inverter Topology," International Conference on Power, Energy and Control (ICPEC), IEEE, pp.700-703, Feb 2013.
- [6] P.Vishvakarma, S.Singh, T. Shukla, "Multilevel Inverters and its Control Strategies: A Comprehensive Review," 2nd International Conference on Power, Control and Embedded Systems (ICPES), IEEE, Dec 2012.
- [7] K.Kumar, S.Jain, "Comprehensive review of a recently proposed multilevel inverter," IET Power Electron, IEEE, vol.7, no.3, pp.467-479, March 2014
- [8] H. R. Seo, M. Park, I. K. Yu, and B. M. Song, "Performance Analysis and Evaluation of a Multifunctional Grid-Connected PV System using Power Hardware-in-the-Loop Simulation," IEEE 2011 Applied Power Electronics Conference (APEC 2011), March 2011, pp. 1945-1948.
- [9] J.Mayo-Maldonado, R.Salas-Cabrera, J. Rosas-Caro, J. De Leon-Morales, "Modelling and control of a DC-DC multilevel boost converter," Power Electronics, IET, IEEE, vol.4, no.6, pp.693-700, July 2011
- [10] Ishaque K, Salam Z, Lauss G. performance of perturb and observe and incremental conductance maximum power point tracking method under dynamic weather conditions. Appl Energy 2014;119:228-36.
- [11] Mellit A, Rezzouk H, Messai A, Medjahed B. FPGA-based real time implementation of MPPT-controller for photovoltaic systems. Renew Energy 2011;36:1652-61.
- [12] Buticchi G, Barater D, Lorenzani E, Concarri C, Franceschini G. A nine-level grid-connected converter topology for single-phase transformerless PV systems. IEEE Trans Ind Electron 2014;61:3951-60.
- [13] Elgendy MA, Zahawi B, Atkinson DJ. Assessment of perturb and observe MPPT algorithm implementation techniques for PV pumping applications. IEEE Trans Sustain Energy 2012;3:21-33.
- [14] Tajuddin MFN, Arif MS, Ayob SM, Salam Z. Perturbative methods for maximum power point tracking (MPPT) of photovoltaic (PV) systems: a review. Int J Energy Res 2015;39:1153-78.



10.22214/IJRASET



45.98



IMPACT FACTOR:
7.129



IMPACT FACTOR:
7.429



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Call : 08813907089  (24*7 Support on Whatsapp)