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A Novel Symmetrical Cascade H-Bridge Multi-Level Inverter Topology with Reduced Switching Devices

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Abstract*: This paper proposes a new structure for cascade h bridge (CHB) based modular multi-level voltage source inverter. As with the correct arrangement of power semiconductor switches and voltage sources, the proposed inverter can provide a high number of output levels with minimum requirements to the circuit devices. By reducing these requirements, cost and circuit size significantly reduce, the inverter control becomes easier and also the system reliability enhances. Furthermore the simulation and also experimental results prove the feasibility of implementing the proposed inverter topology.

I. INTRODUCTION

Inverter is one of the most widely used power electronics device in the world today. The application of inverters can be found in three main categories; power supply, motor drives and active filters. Among the many types of inverters, the multilevel inverter is fast emerging as a popular choice in many industrial applications, from oil and gas, power plant to power quality devices. The staircase output waveform produced by multilevel inverter helps to reduce lower level harmonics while increasing power quality. Compared with two-level inverter that uses high frequency switching as in the case of PWM technique – the staircase waveform quality means that the output voltage is generated with very low distortion, reduced dv/dt stress and also electromagnetic compatibility (EMC); smaller common mode (CM) voltage therefore reduce the stress on the bearings of a motor connected to a multilevel inverter; and low distortion in input current drawn by the multilevel inverter. Other advantages are the number of possible output voltage levels is more than twice the number of dc sources and the higher number dc sources or cells are used, the blocking voltage (OFF voltage) requirement of each power switches become smaller –allowing a lower voltage rating power switches used. The main disadvantage of the multilevel inverter is the high number of power switching devices needed in each design. This will increase the size of the overall inverter circuit and may increase the space occupied by the inverter in the system. Subsequently, it also increases the power losses in the conducting switches (usually in the form of heat) and also reduces the voltage available at the output terminal due to accumulation of voltage drops across each of the conducting switches. So, in this paper the aim is to reduce the number of switches and also the number of conducting switches during inverter operations in order to minimize the heat losses and output voltage drop, as this will increase the overall efficiency of the inverter

II. LITERATURE SURVEY

Multilevel inverter technology was first introduced in 1975. In recent years, according to the features and functionality of these converters, they have been attracted more attention of researchers and engineers. On the other hand the growth of technology and the possibility of industrialization of this type of converters have led to increasing use in industry. Various topologies have been proposed for multilevel inverters. In all proposed structures, multi-level inverters composed of a number of semiconductor power switches, DC voltage sources, driver circuits and sometimes passive elements such as capacitors. This inverter has a DC voltage source in input ports and generates AC voltage. So that the output of multi-level inverters is in the form of steps and provided by the combination of DC sources connecting to the inputs. Multilevel inverters have significant advantages over conventional 2-level inverters, such as: higher power quality, less harmonic content, better electromagnetic interface, the higher first harmonic amplitude, higher efficiency, lower harmonic distortion, and lower switching losses. In addition, electromagnetic interference, size and output filter have been reduced. It has to be noted that the mentioned advantages have a direct relationship to the number of the levels of the output voltage. In other words, the higher the number of level of the inverter output voltage is, the closer the inverter output waveform to the sine wave and the mentioned benefits will be strengthened. From the perspective of voltage sources, various structures have been proposed for multilevel inverters. Some of these structures, using different DC voltage values (asymmetrical

structures) to achieve a high number of voltage levels have been established. While providing an asymmetrical DC voltage source imposes extra expenses in implementation. In symmetrical multilevel inverters, DC voltage sources have equal values, so the cost of implementation is less than the other scheme. However, the symmetrical inverters generate lower number of voltage levels than the asymmetric structures. Therefore, the proposed new structure of multilevel inverters with high performance and minimum requirements for circuit devices is a useful idea[1].

In general the cascaded multilevel inverter consist of series h bridge unit in each of its three phase .Each bridge consist of its own dc source. The cascaded multilevel inverter has two types of source such as symmetric and asymmetric dc source. The symmetric source is equal dc voltage applied to an inverter and the asymmetric source has unequal dc source. The cascaded multilevel inverter is able to increase the number of output voltage levels by using a lower number of power electronic devices such as switches, power diodes, driver circuits, and dc voltage sources that lead to reduction in installation space and cost of the inverter. The main aim of this paper is to reduce harmonics with multilevel output voltages without increasing number of switches [2].

However, the important benchmark for designing multilevel inverters is listed below.

Low voltage stress on switches
Low Electromagnetic interference.
Low Harmonic Distortion
Absence of LC Filter
Modularity
More redundant state
Reliability
Low Cost

The conventional multilevel inverter topologies are (i) Neutral Point Clamped (NPC) (ii) Flying Capacitor (FC) and (iii) Cascaded H-Bridge (CHB). These converters provide better output quality by increasing smaller voltage level; they are applied for commercial applications and industrial applications like AC Drives and FACTS Devices [4].

Unfortunately, multilevel converters do have some disadvantages. One particular disadvantage is the need for a large number of power semiconductor switches. Although low-voltage-rated switches can be utilized in a multilevel converter, each switch requires a related gate driver and protection circuits. This may cause the overall system to be more expensive and complex. An attempt has been made and its development to introduce a new topology for multilevel converters as well as reduce the power electronics switches and dc voltage sources compared to conventional multilevel converters. By the proposed algorithm it is not possible to create all steps (odd and even) at the output voltage. Also, for creating the output voltage with a constant number of steps, the converter needs many large numbers of bidirectional switches. This paper suggests a new topology for multilevel converters with a high number of steps associated with a low number of power switches. In addition, for producing all levels (odd and even) at the output voltage, a procedure for calculating the required dc voltage sources is proposed. Finally, the paper includes a design example for a multilevel converter [6].

The main disadvantage of the multilevel inverter is the high number of power switching devices needed in each design. This will increase the size of the overall inverter circuit and may increase the space occupied by the inverter in the system. Subsequently, it also increases the power losses in the conducting switches (usually in the form of heat) and also reduces the voltage available at the output terminal due to accumulation of voltage drops across each of the conducting switches. So, in this paper the aim is to reduce the number of switches and also the number of conducting switches during inverter operations in order to minimize the heat losses and output voltage drop, as this will increase the overall efficiency of the inverter [5].

III. EXISTING SYSTEM

A. Cascaded H-Bridges MLI

It consists of single phase full bridge or h-bridge inverter which is connected in series with each other with separate dc source. The conventional circuit of single phase seven-level cascaded h bridge MLI has three cells in each phase. Each single-phase full bridge inverter cell produces three voltage levels at output: +Vdc, 0 and –Vdc. The output voltage levels can be given by: N = (M+2)/2, Where ‘M’ is number of switches in circuit. The resultant output voltage can be given by addition of different voltage levels generated by each cells. The resultant output voltage level are given by +3Vdc to -3Vdc which gives staircase waveform.

B. Diode-Clamped MLI

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Diode-clamped MLI is also called as neutral-point clamped inverter. Neutral-point clamped inverter was first introduced by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode clamped inverter. In this topology all the power switches are connected in series with each other. In this topology one dc sources is needed and (N-1) capacitor is used to divide the dc link into different voltages levels, where N is numbers of levels. The clamping diode is used to block the current and their number is selected in such a manner to have the same block voltages. The middle point of (N-1) capacitor is defined as the neutral point.

C. Flying-Capacitor MLI

Flying-capacitor MLI was first introduced by Maynard and Foch in 1992. The basic circuit diagram of flying-capacitor MLI is similar to that of diode-clamped MLI but in the place of camping diode these MLI uses extra capacitor to clamp the connecting point of semiconductor devices which are connected in series. In this topology clamped capacitor is connected in series to block the current and their number in each leg is taken in such a manner that all capacitor store same amount of energy. Flying-capacitor can be extended for generating N voltage levels by adding the capacitor. For N-levels flying-capacitor MLI 2(N-1) switching devices, (N-1)*(N-2)/2 clamping capacitor and (N-1) dc link capacitor are required.

IV. PROPOSED METHOD

A. The New Cascaded Multilevel Inverter Topology

The new cascaded multilevel inverter topology exhibits similar characteristics with the cascaded H bridge multilevel inverter topology – it has modular structure and can be easily implemented through a series of identical units. For an 11-level inverter with 5 dc cells, a total of 10 switches used to construct the inverter, with only 3 switches turned on at any time of operation. If the new topology used to build a 21-level inverter with 10 dc cells, 15 switches are used in the design with only 3 switches turned on at any time of inverter operation. To build a 41-level inverter with 20 dc cells using the proposed topology, only 25 switches needed, again with only 3 switches turned on at any time of inverter operation. Compared with other topologies discussed before, the new topology has fewer switches used, and also regardless of the size of the inverter, the number of conducting switches is constantly maintained with only 3 switches turned on at any time of operation. The new cascaded multilevel inverter topology is compared with the cascaded H-bridge inverter topology and the cascaded multilevel inverter topology proposed by Babaei and Hosseini. The cascaded H-bridge multilevel inverter is chosen because it is the most basic and most commonly discussed multilevel inverter topology and can be found in various technical papers; while the topology proposed by Babaei and Hosseini shares similar characteristics with the cascaded H-bridge multilevel inverter and the proposed new cascaded multilevel inverter topology – it has modular structure and can be easily implemented through a series of identical units [5].

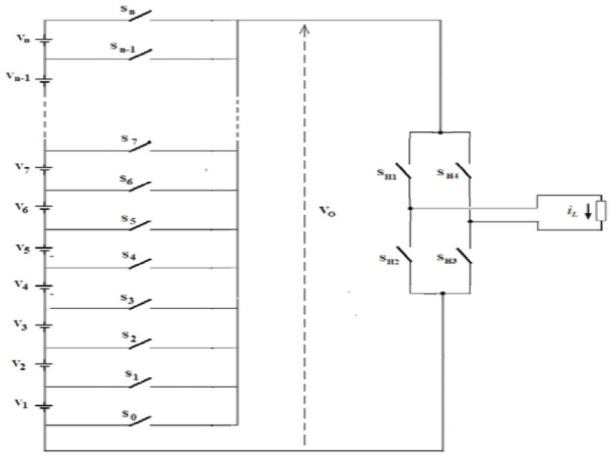

Fig 1. The new cascaded multilevel topology

For a cascaded H-bridge multilevel (see Figure 1) inverter with *n* cells that produce *2n+1* output voltage levels, *m*, there are *4n* switches needed in the inverter construction. At any time of inverter operation, there are *2n* switches needed to be turned on. For the cascaded multilevel inverter proposed by Babaei and Hosseini [10] (see Figure 2), using *n* cells, the inverter can produce *2n+1* output voltage levels, *m*. The number of switches needed in the inverter construction is *2n+4*, with *n+2* switches turned on at any time of inverter operation. The new cascaded multilevel inverter (see Figure 3) with *n* cells also produces *2n+1* output voltage

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levels, *m*. However, the number of switches needed is only *n+5*, with only 3 conducting switches at any time of inverter operation. Table I shows the comparison between the three topologies in term of number of switches; while Table II shows the comparison between the three topologies in term of number of conducting switches during operation respectively.

TABLE I

Output voltage levels	Number of Switches		
	Cascaded H-bridge topology	*Babaei & Hosseini Topology*	*The proposed new topology*
7-level	12	10	8
11-level	20	14	10
21-level	40	24	15
31-level	60	34	20
41-level	80	44	25

Comparison of Number of Switches Needed For Different Output Voltage Levels

TABLE II

Output voltage levels	Number of Conducting Switches During Operation		
	Cascaded H-bridge topology	*Babaei & Hosseini Topology*	*The proposed new topology*
7-level	6	5	3
11-level	10	7	3
21-level	20	12	3
31-level	30	17	3
41-level	40	22	3

Comparison of Number of Conducting Switches during Inverter Operations

V. GENERAL STRUCTURE OF PROPOSED TOPOLOGY

General structure of the proposed CHB multi-level inverter module is shown in Fig. 8(a). Based on this figure, each module contains two DC voltage sources and three switches and can generate three voltage levels, a positive and a zero voltage levels on the output. Switches used are of two types. A type of switch includes IGBTs with anti-parallel diodes and another type just includes IGBTs. Table III presents the switching modes of the proposed module. In addition, various states of the switching displayed in Fig.8 (b) to (d). In this table, state 1 indicates the conduction mode and zero indicates that the switch is off. In the proposed CHB multi-level voltage source inverter all of the DC voltage sources have the same value. Therefore the proposed multi-level module is symmetrical.

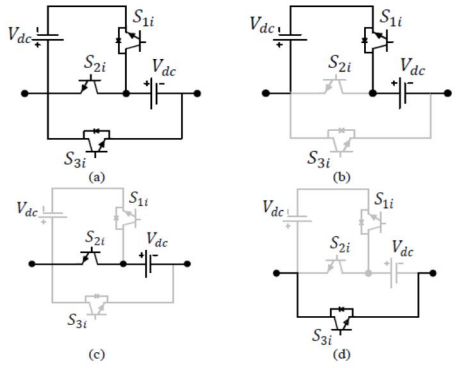

Fig 2. Topology and also operation modes of the proposed CHB multi-level inverter

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Main topology of the proposed module (b) Equivalent circuit of the module in voltage production mode 2Vdc (c) Equivalent circuit of the module in voltage production mode Vdc (d) Equivalent circuit of the module in zero voltage production.

Overview of the proposed multilevel voltage source inverter is shown in Fig. 9. The proposed structure composed of *k* -modules, two isolated DC voltage sources and required switches. *dc V* and *s V* displays the two isolated DC voltage sources. Source amplitude *s V* specified by the number of the DC voltage sources which depend on the levels of the output voltage. In this regard the range of *s V* can be zero or *dc V*.

TABLE III

Voltage level	*S1i*	*S2i*	*S3i*
2Vdc	1	0	0
Vdc	0	1	0
0	0	0	1

Switching modes of the proposed module

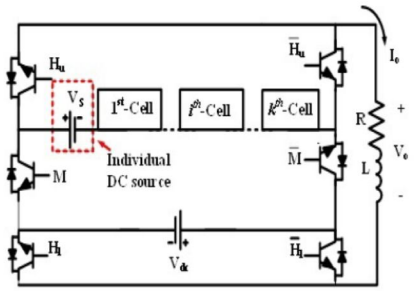

Fig 3. Overview of the proposed CHB multilevel inverter

Appropriate connection of modules with the help of switch *Hl* ،*M* and *Hu* , and also with the supplements of these switches, creates various current paths for producing output voltage waveform with both positive and negative polarity. The maximum output voltage is obtained from (1).

$$V_{o,\max} = \sum_{i=1}^{n} V_i \quad (1)$$

Where n is the number of DC voltage source at the input side. This DC voltage sources can be provided through renewable energy sources such as solar panels or fuel cells or energy storage system such as batteries. When the AC source is present, the use of isolation transformers and rectifiers can create several DC supply. If the smallest DC voltage source amplitude is assumed to be Vdc, so the output voltage waveform would be the step with the height of Vdc. Sample waveform for proposed multilevel voltage source inverter shown in Fig. 3. Different combinations of switching modes for the proposed inverter generates output voltage level from – Vo,max to +Vo,max. The number of output voltage levels (m) can be calculated from (2).

$$m = 2\frac{V_{o,\max}}{V_{dc}} + 1 \quad (2)$$

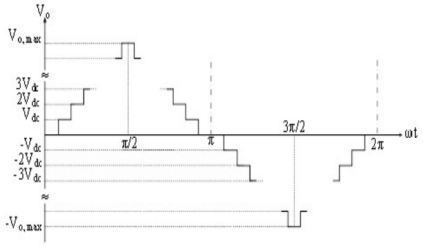

Fig 4. Output waveforms of multilevel inverter

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As previously mentioned, Vs is determined according to the number of voltage levels. In order to make it more transparent, we need to define the parameter *L*. *L* is an integer *L*=1, 2, 3… It is clear that for generating *m*-voltage levels at the output, *n* DC voltage source is required. Eq. (3) represents the number of DC resources required to produce *m* level at the output.

$$n = \frac{m-1}{2} \quad (3)$$

In symmetrical mode, the only way to increase the number of output levels, is to increase the number of DC voltage sources. Because there are two identical DC voltage sources in each module, so that the *n* voltage sources can form *k* modules [1].

VI. SIMULATION AND EXPERIMENTAL RESULTS

The simulation studies involve the deterministic small network topology with 5 nodes as shown in Fig.1. The proposed energy efficient algorithm is implemented with MATLAB. We transmitted same size of data packets through source node 1 to destination node 5. Proposed algorithm is compared between two metrics Total Transmission Energy and Maximum Number of Hops on the basis of total number of packets transmitted, network lifetime and energy consumed by each node. We considered the simulation time as a network lifetime and network lifetime is a time when no route is available to transmit the packet. Simulation time is calculated through the CPUTIME function of MATLAB. Our results shows that the metric total transmission energy performs better than the maximum number of hops in terms of network lifetime, energy consumption and total number of packets transmitted through the network.

he network showed in Fig. 1 is able to transmit 22 packets if total transmission energy metric is used and 17 packets if used maximum number of hops metric. And the network lifetime is also more for total transmission energy. It clearly shows in Fig. 2 that the metric total transmission energy consumes less energy than maximum number of hops. As the network is MANET means nodes are mobile and they change their locations. After nodes have changed their location the new topology is shown in Fig .3 and energy consumption of each node is shown in Fig. 4. Our results shows that the metric total transmission energy performs better than the maximum number of hops in terms of network lifetime, energy consumption and total number of packets transmitted through the network.

In order to prove implementation of the proposed CHB multilevel voltage source inverter, the result of simulation is presented. Ten, the result of the construction of the circuit will be shown. Asymmetrical 13 level inverter, (*m* = 13) has been chosen. In Fig. 13 the proposed symmetrical 13 level inverter circuit is shown. Switching modes of the symmetrical 13 level inverter were collected in Table 2.

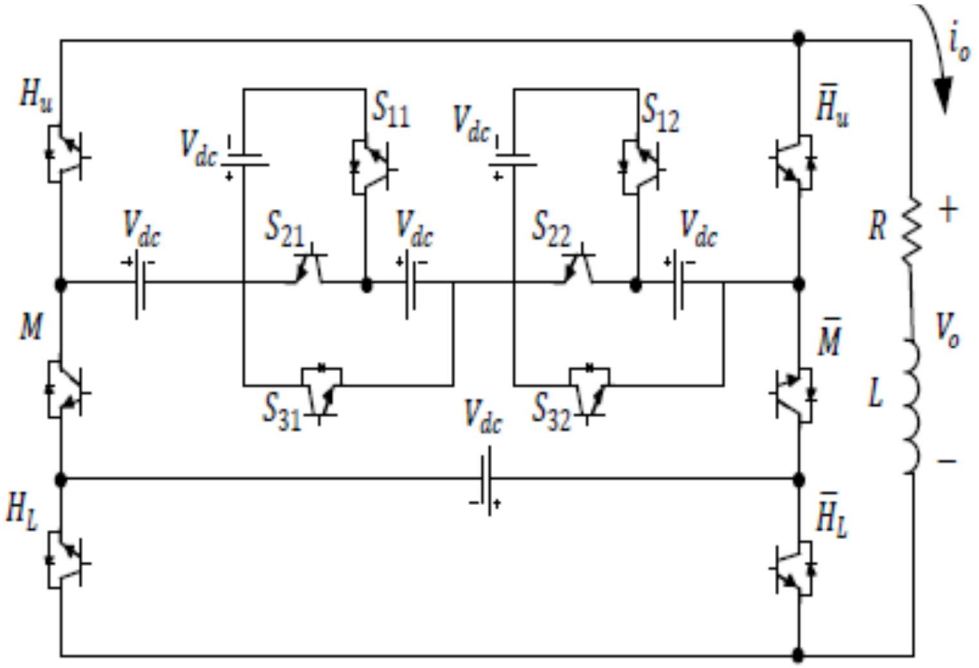

Fig 5. The proposed symmetrical 13 level inverter circuit

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In Fig. 6 and 7, the results of the simulation and experimental for the symmetric 13-level voltage source inverter are shown.

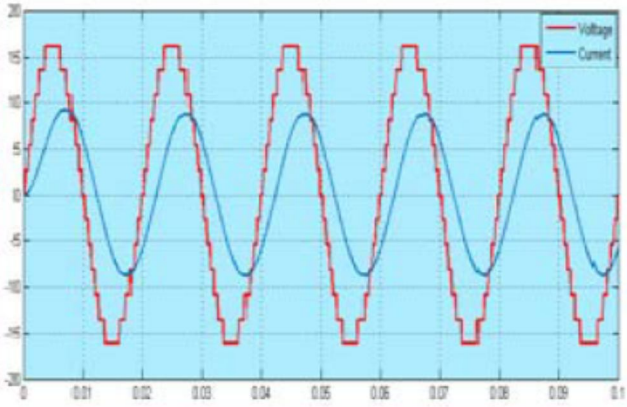

Fig 6. The result of the simulation for the symmetrical 13-level voltage source inverter

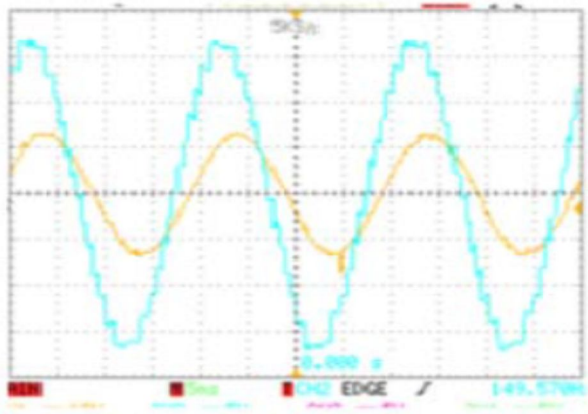

Fig 7. Voltage and current waveforms measured from the laboratory setup

In the multi-level voltage source inverters, the number of required components, including DC voltage sources, semiconductor switches and driver circuits, toward the number of output voltage levels are important because marginal cost, circuit size and also the installation space, reliability and control complexity are directly dependent on them. Therefore, reducing the circuit components from a design perspective is a big challenge. In this section a comparison have been made between the proposed multi-level voltage source inverter, conventional CHB (R1) and proposed CHB in (R2). For a fair comparison, the maximum output voltage (Vo,max) is assumed the same for all listed inverters. Therefore, the comparison was based on the number of output levels. Fig. 16 shows the number of IGBTs needed for inverters.

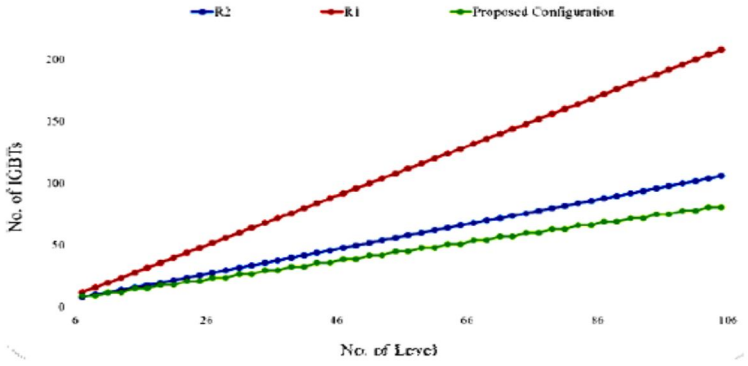

Fig 8. Number of needed IGBTs in terms of the output voltage levels

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The comparison shows that the number of required IGBTs used in the proposed structure for the same output voltage levels is far too low than the other structures. As a result, losses reduction is followed by the reduced operational costs. Fig. 17 shows the number of diodes needed for Suggested inverter for the same output voltage. Based on this figure, the number of diodes in the proposed inverter is far much less than other inverters.

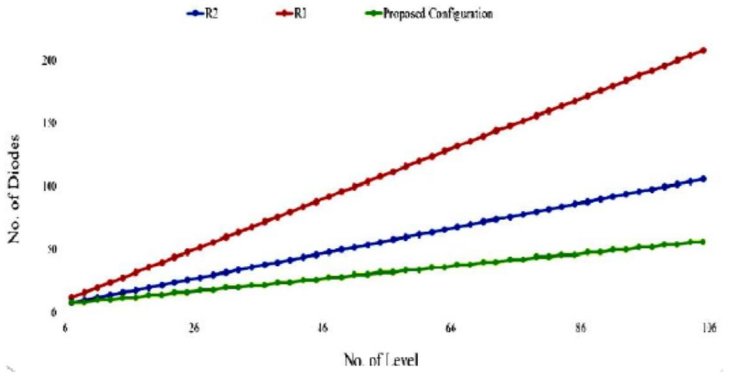

Fig 9. Number of diodes in the proposed inverter in terms of the output voltage levels

VII. CONCLUSION AND FUTURE WORK

In this paper a novel symmetrical CHB multi-level voltage source with reduced switching device is proposed. This topology has less count of power switches, capacitor, diode and less complexity as compare to other multilevel inverter. The simulation results indicate that the structure of the proposed symmetrical 13-level voltage source inverter can generate all voltage levels. To prove the viability of the inverter, laboratory setup has been implemented. This multilevel inverter can be implemented in industrial where the minimum switches are required. The voltage output and current is verified to confirm the performance of proposed multilevel inverter. The nearest level modulation technique is implemented. Future work on this proposed topology considers: (i). High voltage applications by cascading the proposed topology. (ii) In practical applications such as, Induction motor drives and FACTS controllers.

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