iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 5 **Issue:** III **Month of publication:** March 2017

DOI: http://doi.org/10.22214/ijraset.2017.3161

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

Volume 5 Issue III, March 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

An Efficient Reused VLSI Architecture of FMO/Manchester Encoding using SOLS Technique for DSRC Applications

I. V. Rameswar Reddy[1], C. Ashok Kumar Reddy[2], H. Mamatha[3], L. Swaroopa[4], B. Ashok Kumar[5]
[1,2,3,4,5]*ECE, JNTUA*

Abstract: ***the dedicated short-extend correspondence (DSRC) is an effective procedure to push the clever transportation framework into our day by day life. The DSRC guidelines for the most part receive FM0 and Manchester codes to achieve dc-adjust, upgrading the flag unwavering quality. By and by, the coding-differing qualities between the FM0 and Manchester codes truly constrain the possibility to outline a proficient reused VLSI engineering for both. In this paper, the comparability arranged rationale disentanglement (SOLS) system is proposed to defeat this impediment. The encoding capacity of this paper can completely bolster the DSRC benchmarks of America, Europe, and Japan. This paper builds up a proficient reused VLSI design, as well as displays an effective execution contrasted and the current works. The proposed engineering of this paper investigation the rationale size, region and power utilization utilizing Xilinx 14.2***
Keywords: ***Dedicated short-range communication (DSRC), FMO, Manchester, SOLS.***

I. INTRODUCTION

The committed short-extend correspondence (DSRC) is a full duplex short range remote correspondence particularly for car frameworks. The DSRC can be quickly separated into two classifications: vehicle to, car to-roadside. In car to-car, the DSRC empower the messages closure and broadcasting among cars for security issues and open data declaration. The security issues incorporate blind side, crossing point cautioning, entomb autos separation, and crash alert. The car to-roadside concentrates on the clever transportation) administration, for example, electronic toll gathering (And so on framework. With And so on, the toll gathering is electrically proficient with the contact less IC-card stage. In addition, the and so forth can be reached out to the installment for stopping - administration, and gas-srefueling.

Thus, in modern automobile industry the DSRC system plays an important role. The upper and bottom part dedicated for transmission and receiving, respectively.Tranciever is classified into three basic modules they are 1.microprocessor, 2.baseband processing, and 3.RF front-end. The microprocessor interprets instructions from media access control for scheduling the tasks of base band processing, RF front-end, correction, clock synchronization, and encoding. The antenna can receive and transmits the wireless signal from RF front end.

II. LITERATURE SURVEY

Committed short-run correspondences are fullduplex short-range to medium-run remote correspondence channels particularly intended for vehicles utilize and a comparing set of conventions and guidelines.commited short-Go Correspondence (DSRC) Gave correspondence between a vehicle and the roadside in particular area,for instance toll squares.

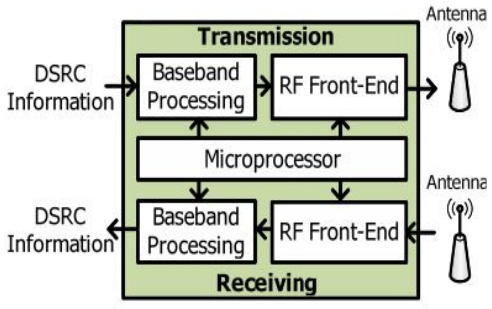


Fig 2.1 System architecture of DSRC transceiver

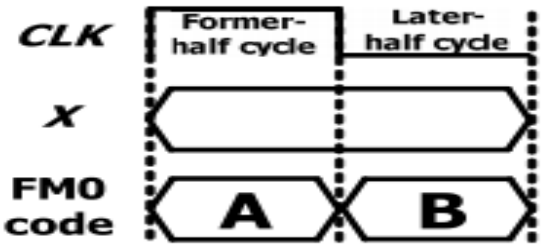
Volume 5 Issue III, March 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

DSRC used to bolster particular wise transport framework application, for example, electronic charge gathering DSRC framework comprise of street side units(RSUs) and the on board units(OBUs) with handsets and transponders. The DSRC indicate the operational frequencies and framework transmission capacities, additionally take into consideration discretionary frequencies which are secured (inside Europe) by national directions. The DSRC standards have been established. The balance techniques fuse abundancy move keying, stage move keying, and orthogonal recurrence division multiplexing. By and large, the waveform of transmitted flag is required to have zero mean for vigor issue, and this is likewise alluded to asdc-adjust. The transmitted flag comprises of self-assertive parallel arrangement, which is hard to get dc-adjust. The reasons for FM0 and Manchester codes can give the transmitted flag dc-adjust.

Both FM0 and Manchester codes are widely used in encoding for downlink. The basic of DSRC is vehicle-to-vehicle communication. Directly using LPCP and LPP realizes the road-to-vehicle communication.

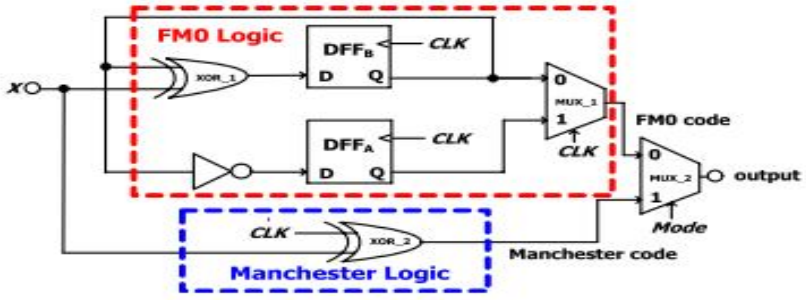
III. PROPOSED METHODS

VLSI design of manchester encoder for optical interchanges. This outline embraces the CMOS inverter and the gated inverter as the change to build manchester encoder. CMOS innovation and the greatest operation recurrence is as high as 5ghz. The writing builds up a rapid VLSI design completely reused with manchester and mill operator encodings for radio recurrence recognizable proof (RFID) applications. This plan is acknowledged in 0.22-µm CMOS innovation and the greatest operation recurrence is 200mhz.the writing likewise proposes a manchester encoding engineering for ultra high recurrence (UHF) RFID label emulator. This equipment engineering is directed from the limited state machine (FSM) of manchester code, and is acknowledged into field-programmable door exhibit (FPGA) prototyping framework. The most extreme operation recurrence of this plan is around 256 mhz the comparative outline approach is further connected to exclusively build fm0 and mill operator encoders additionally for UHF RFID label emulator. Its most extreme operation recurrence is around 192 mhz moreover, joins recurrence move keying (FSK) adjustment and demodulation with



CodeWord Structure Of FM0

VLSI design of Manchester encoder for optical interchanges. This outline embraces the CMOS inverter and the gated inverter as the change to build Manchester encoder. CMOS innovation, and the greatest operation recurrence is as high as 5GHz. The writing builds up a rapid VLSI design completely reused with Manchester and Mill operator encodings for radio recurrence recognizable proof (RFID) applications. This plan is acknowledged in 0.22-µm CMOS innovation and the greatest operation recurrence is 200MHz. Manchester encoding engineering for ultra high recurrence (UHF) RFID label emulator. This equipment engineering is directed from the limited state machine (FSM) of Manchester code. The most extreme operation recurrence of this plan is around 256 MHz.



Hardware architecture of FM0 and Manchester encodings

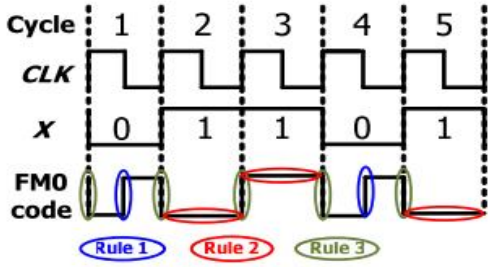
Volume 5 Issue III, March 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

A. FM0 Encoding: The FM0 code consists of two parts: 1.one for former-half cycle of CLK, A, 2. the other one for later-half cycle of CLK, B.

1) The main coding principle of FM0 is listed as 3rulesthey are If *X* is the logic-0, the FM0 code must exhibit a transition between *A* and *B*

2) If *X* is the logic-1, no transition is allowed between *A* and *B*. The transition is allocated among each FM0 code no matter what the *X* is.

3) A FM0 coding example is shown in Fig. At cycle1, the *X* is logic-0; therefore, at FMO code transition occurs according to rule 1. For simplicity, this transition initially set from logic-0-1.According to rule 3, a transition is allocated.

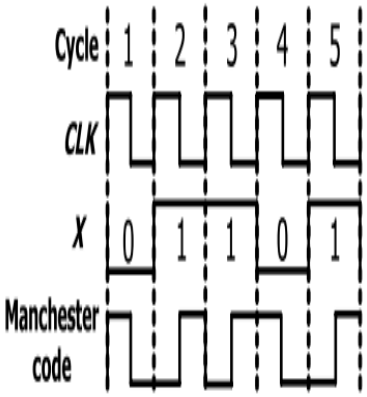


B. Manchester Encoding

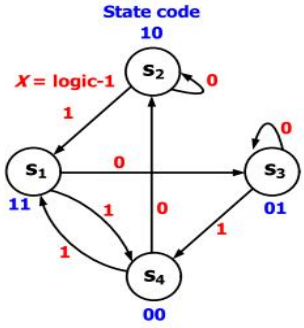
The Manchester coding example is shown in Fig. The Manchester code is derived from

$$X \oplus \text{CLK} \text{---(1)}$$

The Manchester encoding is realized with a XOR operation for CLK and *X*. The clock always has a transition with in one cycle, and so does the Manchester code may either 0 or 1.



The hardware architecture of Manchester encoding is a XOR operation. However, the conduction of hardware architecture for FM0 is not as simple as that of Manchester.By using state code as shown below we can design hardware architecture .



Volume 5 Issue III, March 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Each state code consists of *A* and *B*,and individually assigned to each state. According to the coding principle of FM0, the FSM of FM0 is shown in above fig. Suppose the initial state is *S*1,and its state code is 11 for *A* and *B*, respectively.If the *X* is logic-0, the state-transition must follow both rules 1 and 3. The only one next-state that can satisfy both rules for the *X* of logic-0 is *S*3. If the *X* is logic-1, the state move must take after both standards 2 and 3.

TRANSITION TABLE OF FM0

Previous-state		Current-state			
		$A(t)$		$B(t)$	
$A(t-1)$	$B(t-1)$	$X=0$	$X=1$	$X=0$	$X=1$
1	1	0	0	1	0
1	0	1	1	0	1
0	1	0	0	1	0
0	0	1	1	0	1

The just a single next express that can fulfill both principles for the X of rationale 1 is S4. In this manner, the state-move of each state can be totally developed. The FSM of FM0 can likewise direct the move table of each state, as appeared in Table. A(t)and B(t) speak to the discrete-time state code of current-state at time moment t. Their past states are signified as the A(t – 1) and the B(t − 1) ,separately. With this move table, the Boolean functions of *A(t)* and *B(t)* are given

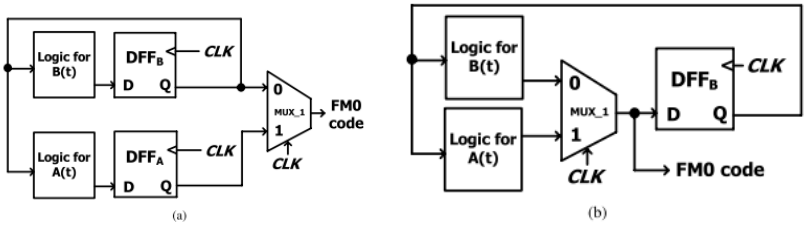
$$\begin{cases} A(t) = \overline{B(t-1)} & (2) \\ B(t) = X \oplus B(t-1). & (3) \end{cases}$$

With both *A(t)* and *B(t)*, the Boolean function of FM0 code is denoted as

$$\text{CLK}\ A(t) + \overline{\text{CLK}}\ B(t). \qquad (4)$$

C. Area-Compact Retiming

The FM0 encoding requires a single 1-bit flip-flop to store the *B(t* −1*)*. If the DFF*A* is removed directly, a non-synchronization between *A(t)* and *B(t)* causes the logic fault of FM0 code. To avoid this logic fault, the DFF *B* is placed right after the MUX−1,as shown in fig(a),where the DFF*B* is assumed to be positive-edge triggered. At each cycle, the FM0 code, including An and B, is gotten from the rationale of A(t) and the rationale of B(t), separately. The FM0 code is on the other hand exchanged between A(t)and B(t)through the MUX−1 by the control flag of the CLK. In Fig.(a), the Q of DFFB is straightforwardly refreshed from the rationale of B(t) with 1-cycle inertness. In Fig. (b), when the CLK is rationale 0, the B(t)is gone through MUX−1 to the D of DFFB. At that point, the up and coming positive-edge of CLK updates it to the Q of DFFB.



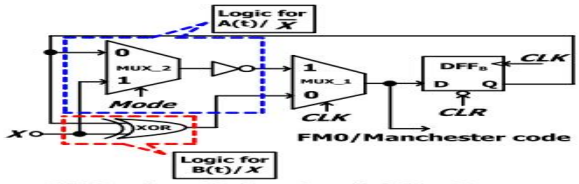
a) FM0 encoding without area-compact retiming. (b)FM0 encoding with area-compact retiming.

The FM0 and Manchester rationales have a typical purpose of the multiplexer like rationale with the choice of CLK.As shown in fig., the idea of adjust rationale operation sharing is to coordinate the Xin to A(t) and X into B(t), separately. The rationale for A(t)/X is appeared in Fig. The A(t) can be gotten from an inverter of B(t−1),and X is acquired by an inverter of X. The rationale for A(t)/X can have a similar inverter, and after that a multiplexer is set before the inverter to switch the operands of B(t − 1) and X. The Mode shows either FM0 or Manchester encoding is received. The comparative idea can be additionally connected to the rationale for B(t)/X, as appeared in Fig. (a). By the by, this engineering displays a downside that the XOR is committed for FM0

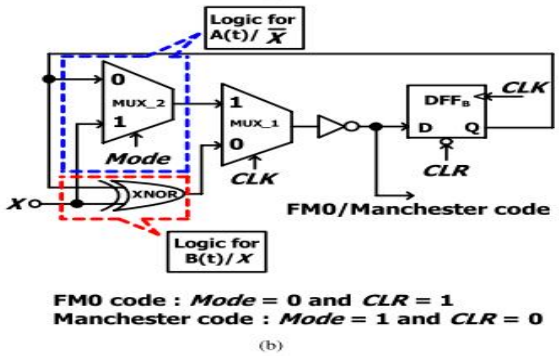
Volume 5 Issue III, March 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

encoding, and is not imparted to Manchester encoding. Consequently, the HUR of this engineering is surely constrained. The X can be likewise deciphered as the X ⊕ 0, and in this way the XOR operation can be imparted to Manchester and FM0 encodings., where the multiplexer is dependable to switch the operands of B(t−1) and rationale 0. This engineering offers the XOR for both B(t) and X, and consequently expands the HUR.

The proposed VLSI architecture of FM0/Manchester encoding using SOLS technique is shown in Fig.(a).The logic for *A(t)/X* includes the MUX−2 and an inverter. Instead, the rationale for B(t)/X just consolidates a XOR door. In the rationale for A(t)/X, the calculation time of MUX−2 is practically indistinguishable to that of XOR in the rationale for B(t)/X. Be that as it may, the rationale for A(t)/X additionally joins an inverter in the arrangement of MUX−2. This unbalance calculation time between A(t)/X and B(t)/X brings about the glitch to MUX−1, perhaps creating the rationale blame on coding. To reduce this unbalance calculation time, the design of the adjust calculation time between A(t)/X and B(t)/X is appeared in Fig. (b). The XOR in the rationale for B(t)/X is converted into the XNOR with an inverter, and after that this inverter is imparted to that of the rationale for A(t)/X. This mutual inverter is put in reverse to the yield of MUX−1. In this way, the rationale calculation time between A(t)/X and B(t)/X is more adjust to each other. The appropriation of FM0 or Manchester code relies on upon Mode and CLR. In addition ,the CLR further has another individual function of a hardware initializaton.



To avoid this conflict, both Mode and CLR are assumed to be separately allocated to this design from a system controller.



D. Static CMOS Topologies

The SOLS technique enables the VLSI architecture to be efficient sharedfor Manchester and FM0 encoders, their critical paths are not identical. For Manchester encoding, the delay time is given as

$$T_{\text{Man}} = \max\{T_{\text{MUX}}, T_{\text{XNOR}}\} + T_{\text{MUX}} + T_{\text{INV}} \qquad (7)$$

where TMan indicates the defer time of Manchester encoding. The TMUX, TXNOR, and TINV speak to the postpone time of the multiplexer, the XNOR entryway, and the inverter, individually. The DFFB is constantly kept at rationale 0 in Manchester encoding; in this way, it is rejected from TMan. This defer way is likewise combined into that of FM0 encoding. In addition,the FM0 encoding applied the DFFB to store the satisfy code, and along these lines the defer time of DFFB is

$$T_{\text{FM0}} = T_{\text{Man}} + T_{\text{DFF}} \qquad (8)$$

The static CMOS topologies of two-info multiplexer and twoinput XNOR are appeared in Fig. (a) and (b), respectively.The pull-

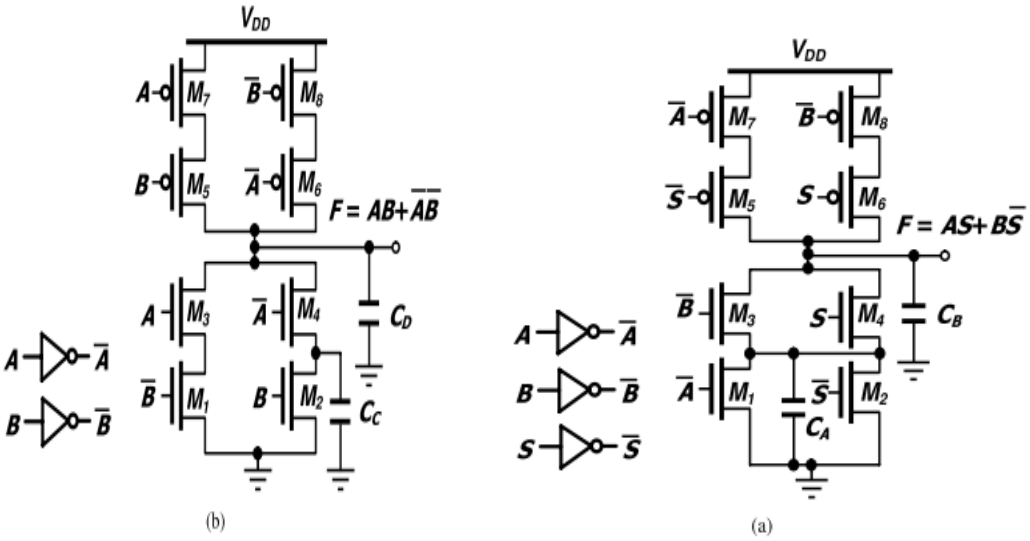
Volume 5 Issue III, March 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

down system of two-information multiplexer incorporates M1, M2, M3, and M4. The M1 and M2 are in parallel, as are M3 and M4. The proliferation postponement of the static CMOS two-input multiplexer is given as

$$T_{\text{MUX-SC}} = T_{\text{INV}} + C_A R + C_B 2R \qquad (9)$$

The *R* represents the equivalent resistor of each transistor in pull-down network. The *CA* aggregates the junction capacitances of *M*1, *M*2, *M*3, and *M*4. The *CB* gathers the junction capacitances of M3 ,M4, M5 and M6. Similarly, the static CMOS two-input XNOR of propagation delay is given as

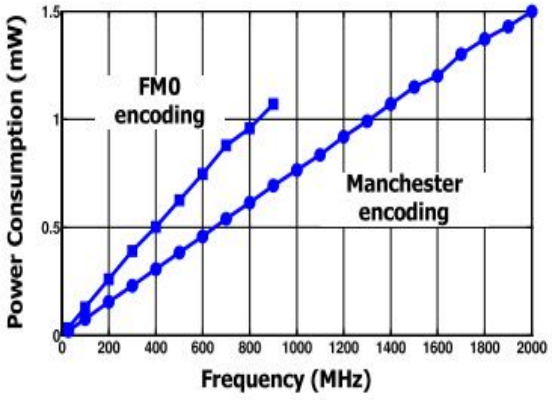
$$T_{\text{XNOR-SC}} = T_{\text{INV}} + C_C R + C_D 2R. \qquad (10)$$



(a) Two-input multiplexer. (b) Two input XNOR.

E. Performance of the SOLS Technique

The total components are reduced from 7 to 5. Without SOLS technique, 57.14%of poor HUR is obtained in hardware architecture of FMO/Manchester . With SOLS technique, the total transistor count.



is reduced from 98 to 44, and every transistor is reused in either FM0 or Manchester encoding. The limitation of HUR is eliminated by SOLS technique by using two core techniques: area-compact retiming and balance logic operation sharing. By using the area-compact retiming relocates the hardware resource to reduce 22 transistors. The static CMOS topologies of two-info multiplexer and twoinput XNOR are appeared in Fig. (an) and (b), respectively.

Volume 5 Issue III, March 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Simulation Results For FMO/Manchester

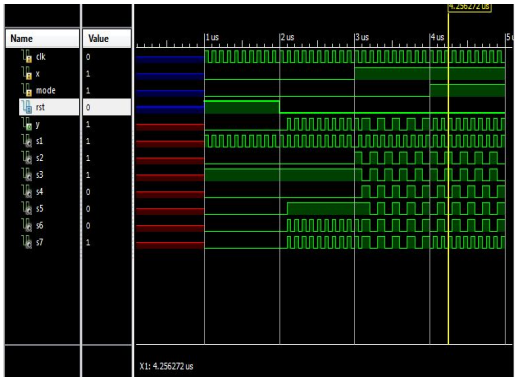


Fig 4.1 FMO and Manchester output

Simulation Results For SOLS Technique

Fig 4.2 FMO output x=0

Fig 4.3 FMO output x=1

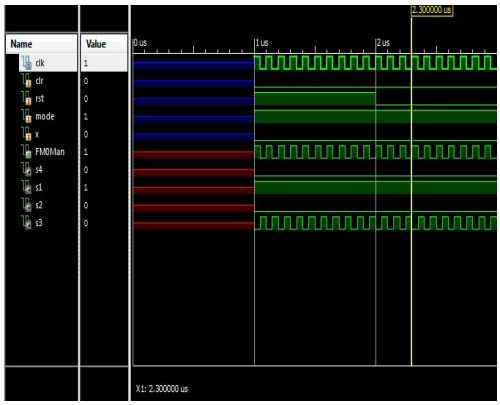


Fig 4.4 Manchester output

IV. CONCLUSION

The coding-assorted qualities amongst FM0 and Manchester encodings cause the impediment on equipment use of VLSI engineering plan. An impediment investigation on equipment uti¬¬lization of FM0 and Manchester encodings is talked about in detail. In this paper, the A Productive reused VLSI engineering utilizing SOLS strategy for both FM0 and Manchester encodings is proposed. The SOLS system evacuates the constraint on equipment usage by two center methods: territory minimal retiming and adjust rationale operation sharing. The range minimized retiming moves the equipment asset to lessen 22 transistors. The adjust rationale operation sharing effectively consolidates FM0 and Manchester encodings with the indistinguishable rationale parts. The maximum operation frequency is 2 GHz and 930 MHz for Manchester and FM0 encodings, respectively.

REFERENCES

[1] Ahmed-Zaid, F. Bai, S. Bai, C. Basnayake, B. Bellur, S. Brovold, et al., "Vehicle safety communications—Applications (VSC-A) final report," U.S. Dept. Trans., Nat. Highway Traffic Safety Admin., Wash- ington, DC, USA, Rep. DOT HS 810 591, Sep. 2011.
[2] J. B. Kenney, "Dedicated short-range communications (DSRC) standards in the United States," Proc. IEEE, vol. 99, no. 7, pp. 1162–1182, Jul. 2011.
[3] J. Daniel, V. Taliwal, A. Meier, W. Holfelder, and R. Herrtwich,"Design of 5.9 GHz DSRC-based vehicular safety communication,"IEEE Wireless Commun. Mag., vol. 13, no. 5, pp. 36–43, Oct. 2006.
[4] P. Benabes, A. Gauthier, and J. Oksman, "A Manchester code generator running at 1 GHz," in Proc. IEEE, Int. Conf. Electron., Circuits Syst., vol. 3. Dec. 2003, pp. 1156–1159.

BIBLIOGRAPHY

Mr.I.V. Rameswar Reddy has pursued his B.Tech from Sree vidyanikethan Engg college ,A.P. and M.Tech from SVPCET, A.P. Presently he is working as assistant professor in the Dept of ECE of Brindavan institute of Technology &Science ,Kurnool. His research areas of interests are VLSI for signal processing, Low power VLSI design & Wireless Communication.

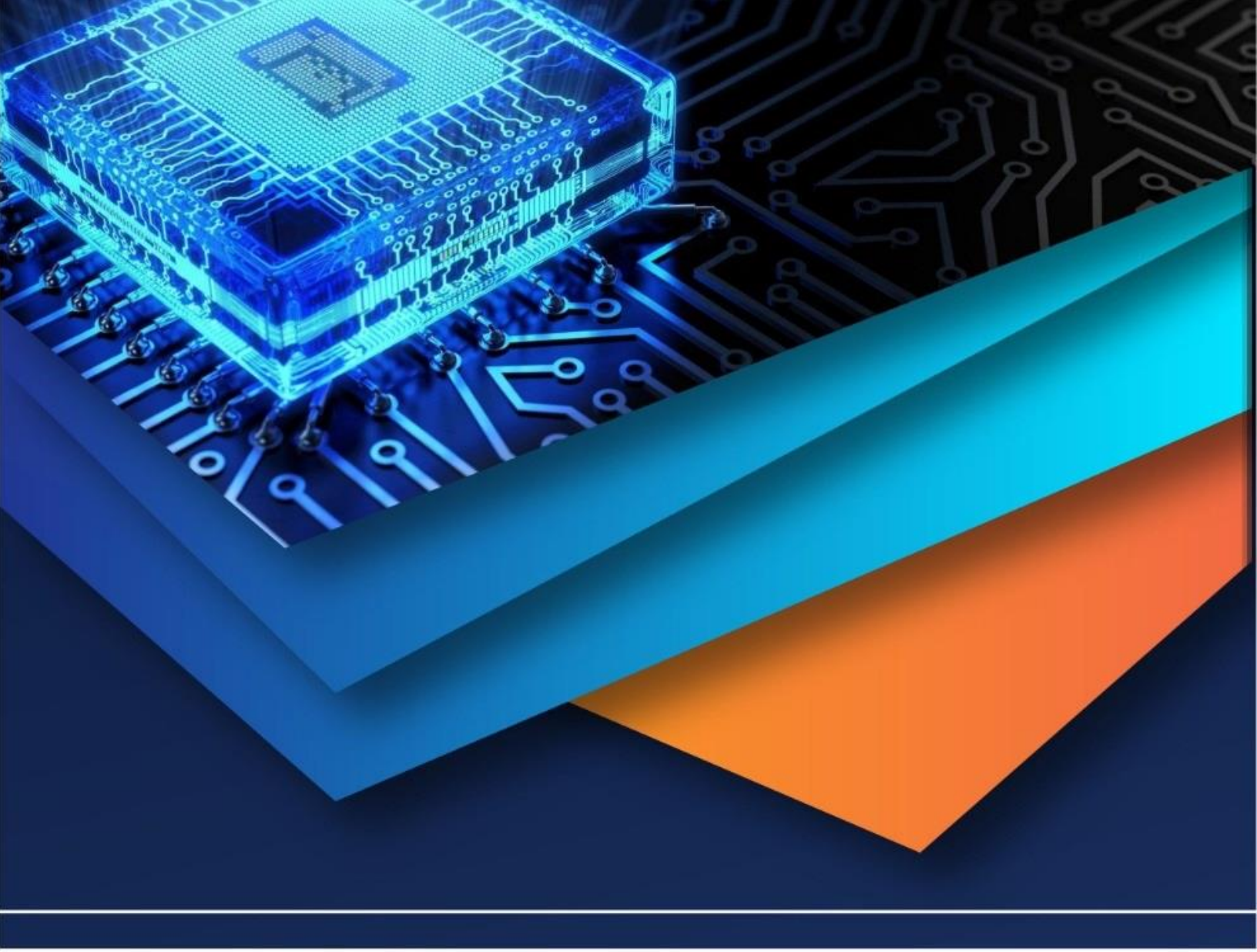
Volume 5 Issue III, March 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Mr C. Ashok Kumar Reddy is pursuing his B.Tech from BITS-KNL in the department of ECE.

Miss H.Mamatha Reddy is pursuing her B.Tech from BITS-KNL in the department of ECE.

Miss L.Swaroopa is pursing her B.Tech from BITS-KNL in the department of ECE. Her areas of interest in VLSI designing.

Mr B. Ashok Kumar is pursing his B.Tech from BITS-KNL in the department of ECE. Her areas of interest in VLSI designing



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY