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Physical Design Implementation of Ternary Arithmetic Circuits

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Abstract: ***Trivalent logic is also called as ternary logic is a promising alternative to the conventional Boolean space. In modern VLSI, CMOS technologies are invented and the die size is reducing day by day. So the complexities on the die increases resulting into the high integration on the same die size. I order to drive the logic, we have to think about the multi-valued logic cell as there are some limitations with the conventional Boolean space. Ternary logic provides simplicity and energy efficiency in digital design as the logic reduces the complexity of interconnects and chip area along with the higher density of information storage.***
The proposed paper presents the physical design implementation of the various ternary arithmetic circuits which involves the universal gates as T-NAND and T-NOR. The ternary arithmetic based design are aimed to achieve the low power consumption, high stability. The physical designs are implemented and simulated using the Microwind 3.5 EDA tool with CMOS 45nm technology.
Keywords: T-NAND, T-NOR, 45 nm, Physical Design.

I. INTRODUCTION

In modern days, as the logic inside the chip increases as the chip have to run numerous applications. The design made up using the MOS transistor have many advantages as compared to the other technologies. The power of the chip is very crucial factor in the todays design. The people working on the design are pretty concerned about power than the speed and area of the chip. This paper provide the comparative analysis between the Binary universal gates with the ternary gates. The universal gate are very important and we can realize any logic by using these types of gates. The NAND and NOR gate can give rise to many terminologies in VLSI domain. As far as the theory concern, multivalued circuits have many advantages over their binary circuits
Ternary arithmetic based circuits can transmit more information than binary, the number of connections inside the chip can be reduced.
Ternary arithmetic based circuit element can process more information than a binary element, so the complexity of circuits may be decreased.
The speed of serial information transmission is faster since the transmitted information time is increased.

II. TERNARY ARITHMETIC

In case of the binary Boolean algebra, there are two logic levels as “0” and “1”. The total logic implementation is based on these two logic levels. But in case of the ternary arithmetic, there are three logic levels as “0”, “1/2” and “1”. In terms of voltages ass input, these input values will become, if we are having vdd as 1.2V, the logic input will be like 0V,, 0.6V and 1.2V. So applying such logic levels in terms of the voltages will give the feel of the ternary arithmetic circuit. In case of T-NAND and T-NOR gate the truth table have to follows as per the logic provide. The table-I given below provides the logic truth table for the TNAND and TNOR gates. PAGE STYLE

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TABLE I: Truth table for TNAND and TNOR

Ternary Inputs		Ternary Outputs	
A	**B**	**T-NAND**	**T-NOR**
0	0	2	2
0	1	2	1
0	2	2	0
1	0	2	1
1	1	1	1
1	2	1	0
2	0	2	0
2	1	1	0
2	2	0	0

As per the logic levels, the ternary NAND gate provides me the lowest level only for the 2-2 combination of the inputs. Also the output will be level high for the low level combination of the inputs. For middle level of the input, the output aging provides me the middle level.

III. DESIGN IMPLEMENTATION

A. T-NAND Gate

The schematic design of Ternary NAND gate is shown in figure 1. It consists of 10 transistors. Out of these 10 transistor, 4 transistors are PMOS and 6 are NMOS. The overall working of the NOR gate is depends upon the width and length calculations of each transistor used in the design. Also the threshold voltage plays a vital role is assigning the voltage levels coming at the output node.

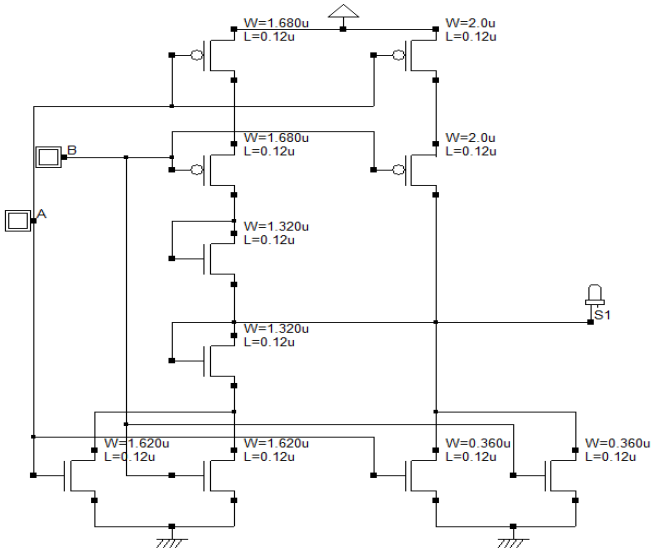

Figure 1: Schmatic design of T-NAND

B. T-NOR Gate

The schematic design of Ternary nor gate is shown below. It also consists of 10 transistors. Out of these 10 transistor, 4 transistors are PMOS and 6 are NMOS. The overall working of the NOR gate is depends upon the width and length calculations of each transistor used in the design. Also the threshold voltage plays a vital role is assigning the voltage levels coming at the output node.

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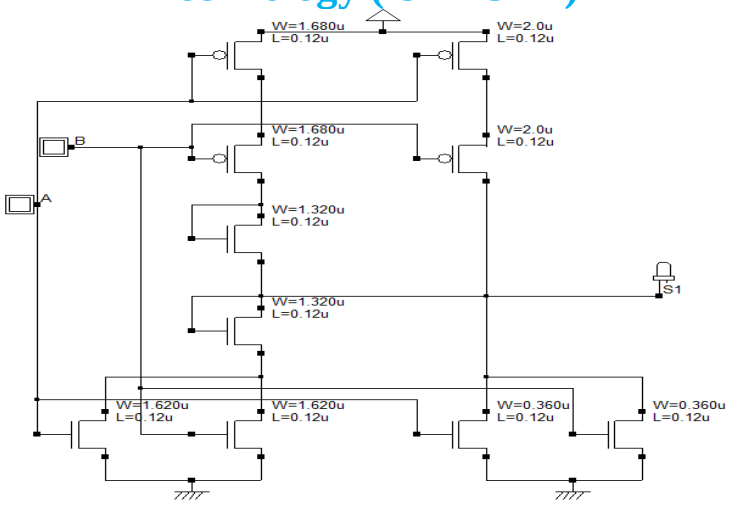

Figure 2: Schmatic design of T-NAND

The Ternary gate called T-gate qualifies as a universal element in several different senses as,

1) It should be logically complete with simple operation.
2) It should be easily implemented with its straightforward construction.
3) It should possess two essential elements that must be embodied in any logic gate, namely, logic-value thresholding and logic-signal connection of switching.

These all 3 set of elements makes ternary arithmetic to be popular and to be used in the highly dense application systems.

IV. PROPOSED PHYSICAL LAYOUT DESIGN

A. T-NAND Gate

The cell architecture has been optimized for easy supply and input/output routing. The supply bars have the property to connect the potential values. The threshold voltage plays a vital role in understanding the behavior of the ternary NAND gate. Now by generating the physical design putting the W/L values.

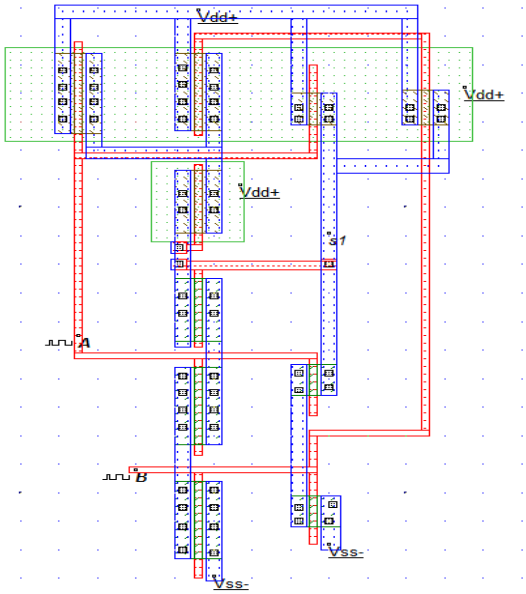

Figure 3: Physical design of T-NAND gate

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Table III: W/L ratio for Ternary NAND gate

Transistor	**Width (um)**	**Length (um)**
T1 (PMOS)	0.980	0.040
T2 (PMOS)	0.980	0.040
T3 (PMOS)	0.420	0.040
T4 (PMOS)	0.420	0.040
T5 (PMOS)	0.770	0.040
T6 (NMOS)	0.770	0.040
T7 (NMOS)	0.945	0.040
T8 (NMOS)	0.945	0.040
T9 (NMOS)	0.385	0.040
T10 (NMOS)	0.385	0.040

B. T-NOR Gate

Table IV: W/L ratio for Ternary NOR gate

Transistor	Width (um)	Length (um)
T1 (PMOS)	1.680	0.040
T2 (PMOS)	1.680	0.040
T3 (PMOS)	2.00	0.040
T4 (PMOS)	2.00	0.040
T5 (NMOS)	1.320	0.040
T6(NMOS)	1.320	0.040
T7(NMOS)	1.620	0.040
T8(NMOS)	1.620	0.040
T9(NMOS)	0.360	0.040
T10(NMOS)	0.360	0.040

The cell architecture has been optimized for easy supply and input/output routing. The supply bars have the property to connect the potential values. The threshold voltage plays a vital role in understanding the behaviour of the ternary NAND gate. Now by putting the physical design putting the W/L values.

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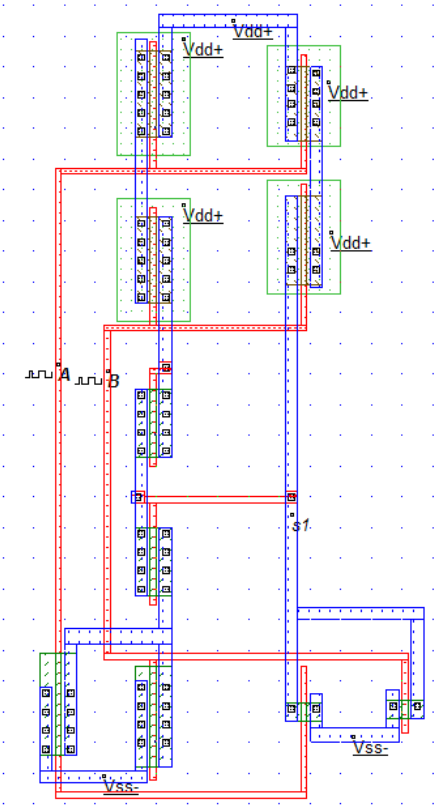

Figure 4: Physical design of T-NOR gate

V. SIMULATION RESULT

For simulation of the ternary arithmetic circuits, we need to design a special type of input which will exhibit three voltage levels. In Microwind software tool, we can use several number on input forms. The input form PWL stands for Piese-wise-linear. In such form of input, we can provide the sequence of input in the data stream format. It is the special type of input which is useful for worst case delay finding in any combinational circuits. It provides you two voltage levels as shown in figure as level 0 and level 1. For 45 nm CMOS technology, the Vdd is 1 V, as level 1 and we start the input value from 0, as level 0. In this case, our input will start from 0v and will ends up at 1v.

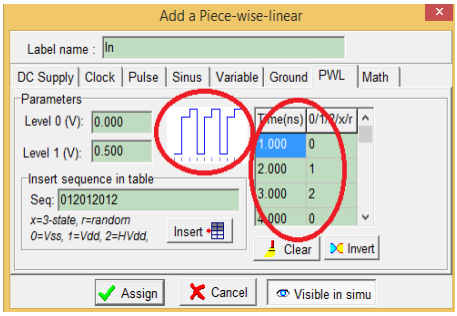

Figure 5: Three level input form with voltage levels

After assigning the PWL to the physical design, the simulation shown n figure 5.
The above simulated output shows the transient analysis of voltage. As per the truth table we are coming across the values of output.

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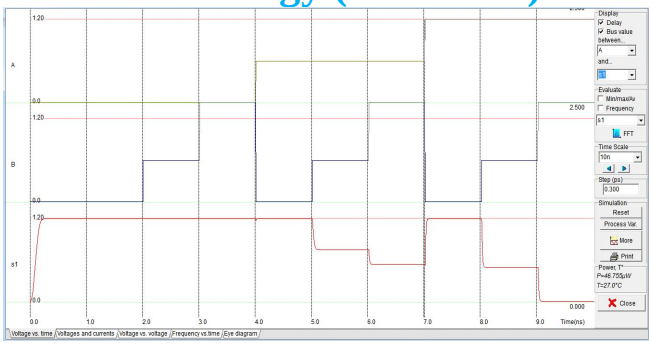

Figure 5: Transient analysis for voltage for T-NAND gate

From the figure it is clear that the physical design follows the truth table of the T-NAND gate.

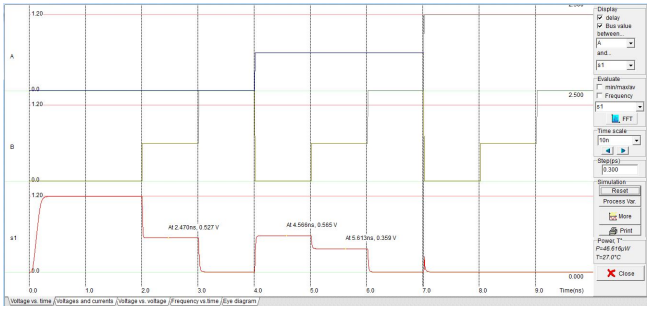

Figure 5: Transient analysis for voltage for T-NOR gate

From the figure it is clear that the physical design follows the truth table of the T-NOR gate.

Table V: comparison of power and delay

Parameters	T-NAND Gate	T-NOR Gate
Area	9.8µm2	12.8µm2
Power	20.276 µW	20.284 µW
Delays	1.27ns	1.98ns

VI. CONCLUSION

This paper presents the simulation and Implementation of and simulation of CMOS based circuitry. Here for the design, Microwind 3.5 VLSI Backend software is used for generating, designing and testing ternary circuits. This software allows designing and simulating an integrated circuit at physical description level.

For our design, the VDD is 1 V and for a perfect designed, it must be 0.5. The different parameters such as area, power and speed of the design is optimized and calculated during the real time simulation

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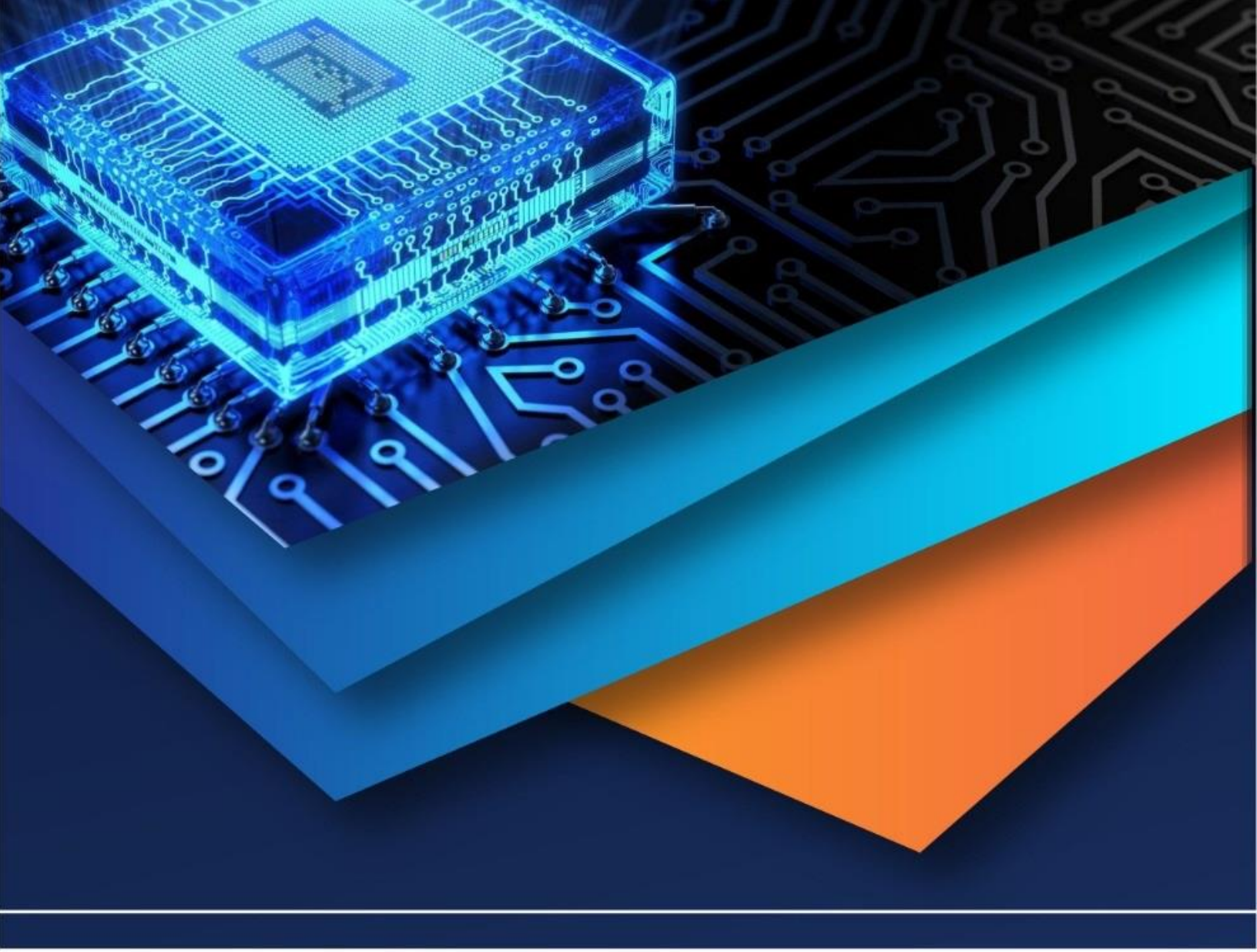

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