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D Flip Flop with Low Power Clocking System by using MTCMOS and Slumber Keeper Technique

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Abstract: ***power utilization plays an significant function in any integrated circuit. We are having three main challenges in semiconductor technology. in any integrated circuit clock sharing networks and storage elements such as flip-flop consume more power. in this paper, an assortment of techniques to implementing flip-flops with low power clocking structure is analyzed. among those different techniques clocked pair communal flip-flop using mtcmos(cpcff-mt) consume smallest amount of power than conditional statistics mapping flip flop (cdsff),conditional expulsion flip flop (ceff) and conservative twin edge triggered flip-flop (teff). we put forward a new (cpcff-mt) with slumbery keeper technique which reduces the power consumption by approximately 30% to 75% than the original cpcff-mt.***
keywords: flip-flop; mtcmos ; low power clocking; clocked pair ; slumbery keeper; Tanner ED tools.

I. INTRODUCTION

In the former arena the VLSI designers were more turned towards the performance and area of the circuits. Reliability and cost also gained nucleus importance whereas power utilization was a marginal reflection for them. In recent years, however, this has begun to change hurriedly and power is also being given identical significance in comparison to area and speed . yet growing demands for portable electronic devices and notable sensation and development of the class of wireless communication systems as special digital assistants and special communicators which require multifaceted functionality and elevated speed has improved the necessity of the use of power proficient VLSI circuits. There are four key mechanisms of power debauchery in digital circuits which are summarize in the following equation

$$P_T = \alpha C_L V_{dd}^2 f_{clk} + V_{dd}(I_{sc} + I_{leakage} + I_{static}) \quad (1)$$

PT represent for total power debauchery, which constitute Isc, Ileakage and Istatic currents and switching power debauchery. The first component αCLVdd 2fclk in equation (1) represents the power debauchery for the duration of switching occurrence, where CL represents the capacitance load; the fclk represents clock frequency and α is the transition node factor. The following constituent is the Isc represents the shortcircuit current, which arise when both the NMOS and PMOS transistors perform concurrently for a precision period, establishing a straight current pathway from power supply to the ground. The leakage current, Ileakage, in the circuit is conquered by two essential sub-threshold current and another component is a diode reverse leakage current in the fabrication technology. The static current, Istatic, is the direct current from power supply.

As technology scales down, short-circuit currents and power leakages becomes analogous to dynamic power debauchery .accordingly, the detection and modeling of different leakage and switching mechanism is very imperative for the assessment and diminution of power utilization particularly for high-speed and low-power applications. The two capable techniques to reduce power consumption is Multi-Threshold voltage CMOS (MTCMOS) with slumbery keeper technique[10] and voltage scaling technique.

Fip-Flop is an electronic circuit that is used to store a logical condition of any data input signals with the retort to a clock pulse. Flip-flops are extensively used to collect and maintain data in selected sequences throughout inveterate clock intervals for a limited time period plenty for other circuits within a system. A massive section of the on-chip power is obsessive by clock systems, which consists of timing elements such as flip-flops, latches and clock distribution network. These clock network systems have disused evolution and the evolution probability of the clock is 100% while an ordinary logic has one-third on average so clock systems are one of the most power intense components in a VLSI system .These components consume 20% to 60% of the whole power debauchery in a system . As a result, reduction in the power consumed by flip-flops will show a deep impact on the total power consumption. Several techniques as well as various flip-flops have been planned in recent times to condense redundancy in clock system. There are many flip-flops given in the literature [1]-[7].Many digital and computational circuits selectively use master-slave and pulsed-triggered flip-flops [4]. There are two types of edge triggered flip-flops given in literature firm edge(transmission gated edge triggered flip-flops and sense amplifier-based flip-flops) and squashy edge (pulse-triggered flip flops).

The firm edge triggered flip-flops consist of two stages, one master and one slave which basis large D-to-Q delays and are

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characterized by a positive setup time. Alternatively, squashy edge triggered flip-flops reduce the two stages into one stage. The categorization of the pulse triggered flip-flops can be made in two ways, first being overt-pulsed triggered and the other being oblique-pulsed triggered flip-flops. As the pulse originator in the case of overt flip-flops is present externally thereby distribution of the pulse originator in this case becomes realistic than in the case of the oblique-flip flops where the pulse originator is internal to the circuit. The distribution in the case of overt-pulse triggered flip-flops can help in distributing the power slide of the pulse originator across many flip-flops, so to have the advantage of better performance, since the height of the NMOS stack in this case is less than that in the oblique flip-flops .

This paper is organized as follows. Section II surveys various flip-flops for low power design. Section III describes MTCMOS technique and slumbery keeper for the abatement of stand-in leakage power consumption. Section IV presents the proposed Multi-Threshold CPCSF (CPCFF-MT) with slumbery keeper technique for low power and better performance. Section V presents simulation results. Section VI clinches this paper.

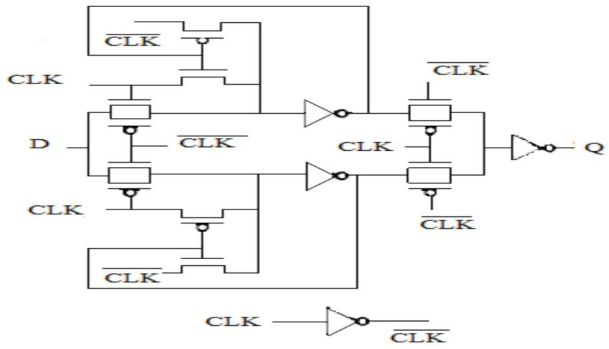
II. TECHNIQUES FOR REDUCING CLOCK ACTIVITY

We analysis various D flip-flops and classify them into four different groups as shown in the Fig. 1: conservative twin edge triggered flip-flop (TEFF), conditional expulsion flip-flop (CEFF), conditional data mapping flip-flop(CDSFF) and clocked pair shared flip-flop (CPCSF).

Fig. 1 shows that sampling of the data is done on both the rising and the falling edge of the clock signals by TEFF. It has the same number of transistors as that of the conservative single edge triggered flip-flop (SEFF) [2]. Reduction of the frequency to half in case of TEFF results in abatement of the power dissipation to approximately half of the value of SEFF. CEFF is suitable for both implicit as well as explicit pulse triggered flip-flops. CEFF uses a pulse originator which eventually generates the pulses for implementing the circuit in Twin edge triggered technology. As shown in Fig. 1 [7] CEFF operates in two stages. The first stage is mainly for the LOW to HIGH transition, while the second stage being. Responsible for HIGH to LOW transition. Removal of extra switching activity takes place by controlling the expulsion path when the input is at stable level '1'. Controlling of the expulsion path results by adding NMOS, this is controlled by Qb. The expulsion path of the first stage helps in preventing assessment in the coming clock cycles as long as input remains at stable level '1'[7].

CDSFF uses pulse–triggered structure for high performance in contrast to CEFF which uses twin edge clocking. As shown in Fig. 1 [6] CDSFF uses only 7 clocked transistors in comparison with CEFF which uses 13clocked transistors resulting in reduction of the power consumption. The conditional statistics mapping (CSM) methodology exploits the property of the flip-flop, by providing the flip-flop with a stage to map its inputs to (0, 0) if a redundant event is predicted, such that the outputs will be unaffected when clock signal is triggered. A conditional statistics mapper is deployed in the circuit to map the inputs by using outputs as control signals. CDSMFF annihilate CEFF in terms of power consumption [9]-[11].

Although CSMFF reduces the power consumption but it is more vulnerable to redundant clocking in addition to a floating node [9]. CPCFF overcomes the problem of floating node in CDSFF by reducing the number of clocked transistors as shown in Fig. 1 (d) [12]. CPCFF uses 4 clocked transistors in comparison with CSMFF which uses 7 clocked transistors; hence reducing the clock load. In CPCFF the clocked pair is communal by the first and second stage. The always on PMOS in CPCFF allows the internal node to be always connected to Vdd thus prevents the floating problem. Thus in terms of power utilization of clock circuit CPCFF is more efficient than CSMFF.



fig(1). conservative twin edge triggered flip-flop (TEFF)

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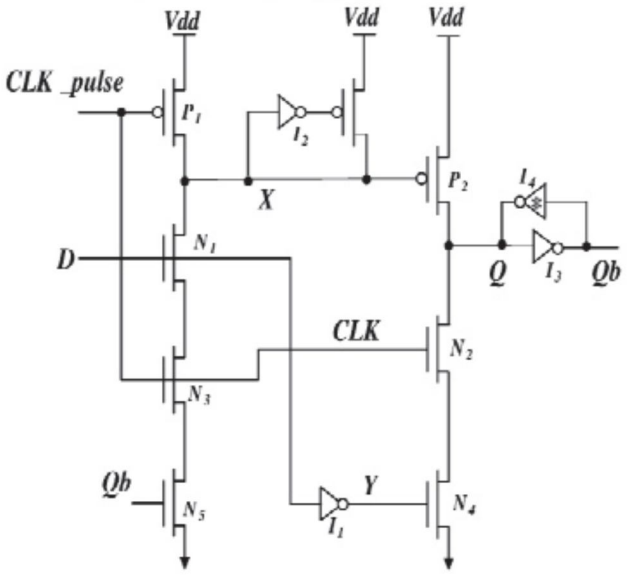
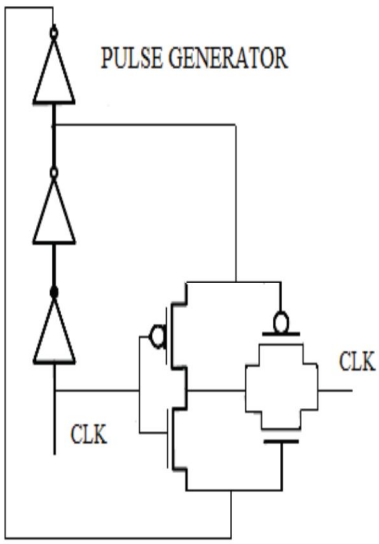
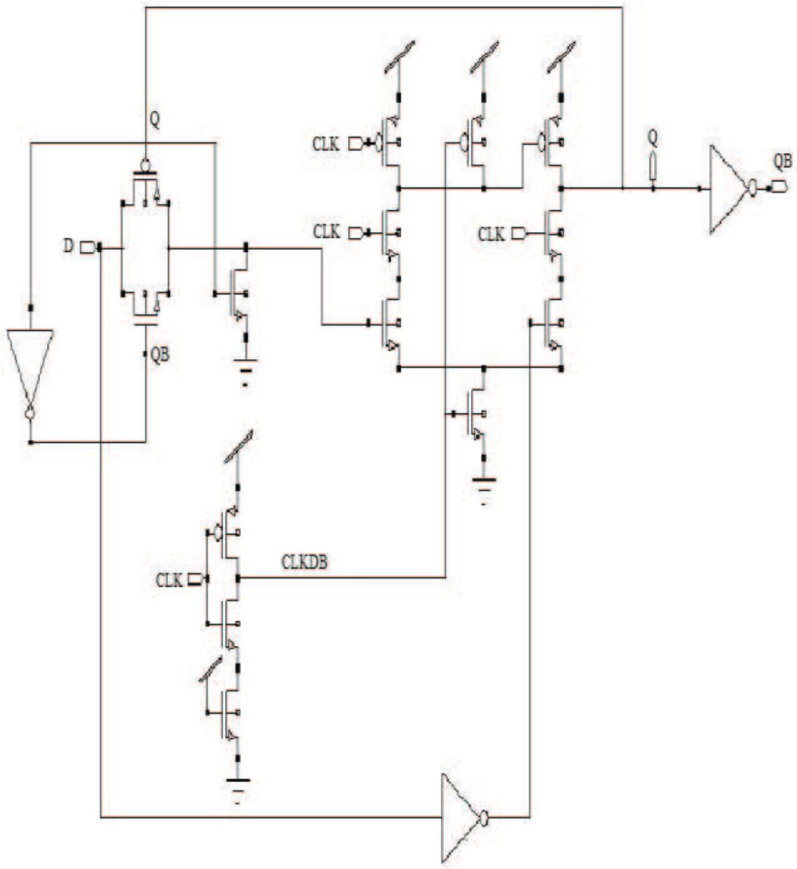


fig(2). conditional expulsion flip flop (CEFF)



fig(2.1).Pulse Generator



fig(3). conditional statistics mapping flip flop (CDSFF)

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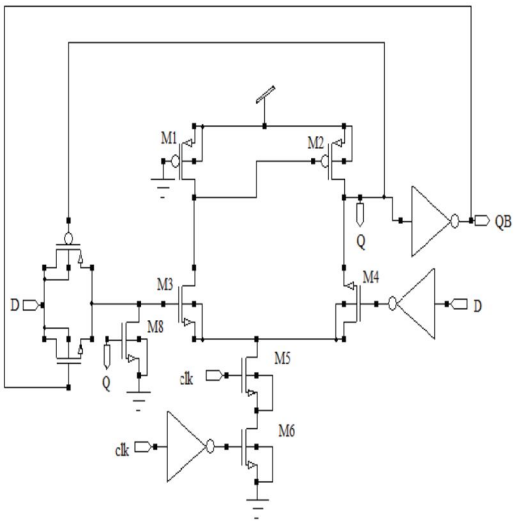


Fig. (4). clocked pair communal flip-flop (CPCSFF)

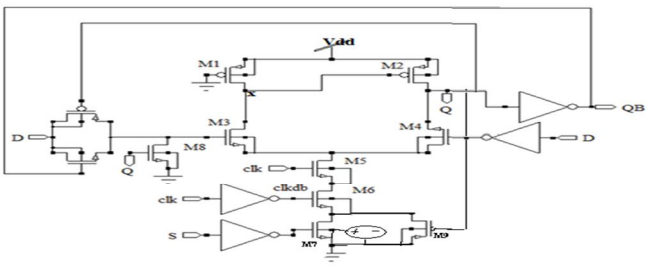
III. MTCMOS TECHNIQUE AND SLUMBERY KEEPER TECHNIQUE

Reduction in supply and threshold voltages is attainable by the scaling of the CMOS technology. An absolute increase in the sub threshold current arises from the lowering of the threshold voltages. In modern high performance integrated circuits (ICs), more than 40% of the total dynamic form energy can be dissolute due to the leakage currents. With more transistors integrated on-chip, leakage currents will almost immediately dominate the total energy consumption of high performance ICs. Moreover, the sole source of energy consumption in an idle circuit is the leakage current.

The power gating technique using MTCMOS is shown in Fig.2. The diagram consists of two slumber transistors S1 and S2 with higher Vt. The logic circuit between the S1 and S2 is not directly connected to real supply lines Vdd And Gnd, but in turn it is connected to virtual power supply

lines Vddv and Gndv and has low Vt. Both the slumber transistors are given complementary inputs S and SBAR. The above circuit operates in two modes dynamic mode and stand-in mode. In dynamic mode, S=0 and SBAR=1 such that S1 and S2 are ON and virtual supply lines Vddv and Gndv work as real supply lines therefore the logic circuit operates normally and at a higher speed. In slumber mode, S=1 and SBAR=0 such that S1 And S2 are OFF and this will cause virtual power supply lines to float and large leakage current present in circuit is suppressed by slumber transistors S1 and S2 resulting in lower leakage current and thus reducing power consumption.

IV. PROPOSE CLOCKED PAIR COMMUNAL FLIP-FLOP USING MTCMOS(CPCFF-MT) WITH SLUMBERYKEEPER TECHNIQUE



fig(5):cpcff-mt with slumbery keeper technique

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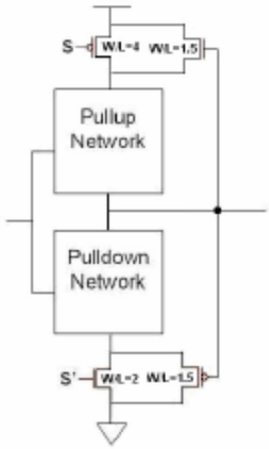

Fig(6):slumbery keeper technique

To reduce stand-in leakage power consumption and to ensure efficient implementation of sequential elements, we propose clocked pair shared flip-flop using MTCMOS technique. We are designing this circuit keeping the number of clocked transistors same as in the actual circuit. The schematic of MT-CPSFF is shown in Fig. 3.In this proposed Clocked Pair communal Flip Flop, a high threshold voltage nMOS transistor is provided with a sleep signal S, which is high in the dynamic mode and low during the stand-in mode. Here, the first and the second stage shares the same clocked pair (M5 and M6). Furthermore, the pMOS M1 is always turned on and is connected to the power supply Vdd, thus charging the internal node X all the time. This reduces the floating of node X and enhances the noise robustness. The flip flop works, when both clk and clkdb are at logic '1'. Pseudo nMOS and conditional mapping technique both are combined using the above scheme. The nMOS M3 is controlled by a feedback signal. For input D=1and S=1,Q will be high, switching ON the transistor M8, and turning OFF M3 thus parrying redundant switching activity and flow of shortcircuit current at the node X. When D transits to 1 the output Q is pulled up by pMOS M2 whereas M4 is used to pull down Q when D=0 and Y=1 at the arrival of clock pulse.

When the input D transits from 0-1 the short-circuit occurs for once even though M1 is always ON, thus disconnecting the discharge path and turning off M3 after two gates delay by

feedback signal. There will be no short-circuit even if the input D stays high as M3 disconnects the discharge path. The output of the flip flop depends upon the state previously acquired by Q and QB along with the clock and the data signal inputs provided.The above figure(5) shows the MT-CPSFF using slumbery keeper technique. In slumbery keeper transistor approach two PMOS transistors are placed in the pull down network. In sleep mode, the sleep transistor is off, transistor N1 is also off. Now we see that the other 2 transistors P4, P6 connect the main circuit with power rail. Here we use 2 PMOS in the pull down network .The advantage is that PMOS degrades the low logic level. Due to the body effect, they further decrease the voltage level. So, the pass transistors decreases the voltage applied across the main circuit. As we know that static power is proportional to the voltage applied, with the reduced voltage the power decreases but we get the advantage of state retention.

V. SIMULATION RESULTS AND CONCLUSION

The simulation results for all existing and proposed flip-flops were obtained in a 90nm CMOS technology at room temperature using Tanner EDA Tools 13.0 over various supply voltages and frequencies. Table I show power comparison results for the TEFF, CEFF, CDSFF, CPSFF and the proposed MT-CPSFF for 1.5, 2.5,3.5 and 5 supply voltage (Vdd) over 750MHz and 500MHz clock frequencies. Table I show that CDSFF has 20% less power consumption than conventional CEFF at 500MHz clock frequency and 1.5Vdd. Similarly at 500MHz and 3Vdd CEFF consumes 24.02% less power than conventional CEFF. With the reduction in the number of clocked transistor in the CDSFF as compared to CEFF, the power consumption by CDSFF is reduced. Albeit CDSFF reduces the power consumption to a considerable amount, but it is susceptible to redundant clocking in addition to a floating node. The CDSFF overcomes this drawback by reducing the number of clocking transistors. For 500 MHz and at 3Vdd CPCFF consumes 3.80% less power than CDSFF. Similarly at 750MHz and 1.5Vdd CPCFF consumes 5.74% less power as compared to CDSFF. The comparison shows that reducing the clocked transistors has a major effect on reducing the total power consumption of the design circuit. The proposed MT-CPSFF which makes use of MTCMOS technique shows higher performance as well as smaller stand-in

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leakage current. The low Vt MOSFETs enhances the speed, while the higher Vt MOSFETs reduces the stand-in leakage current.Table I show that for MT-CPCSFF with slumber keeper technique 750MHz and 5Vdd, the proposed circuit consumes 57.7% less power as compared to conventional TEFF. Similarly at 750MHz and1.5Vdd MTCPCFF with slumber keeper consumes 15.2% less power than conventional TEFF. The MT-CPSFF using slumbery keeper technique consumes 5.3% less than the MTCPSFF.

Design name	Number of transistors	Number of clocked transistors	Frequency							
			500MHZ				750MHZ			
			Power consumption(mW)				Power consumption(mW)			
			Supply voltage(Vdd)							
			1.5	2.5	3	5	1.5	2.5	3	5
TEFF	22	12	58	89	121	258	72	124	125	265
CEFF	26	13	55	72	100	161	67	159	115	227
CDSFF	19	7	44	69	93	151	57	101	106	182
CPCFF	15	4	26	46	52	148	31	58	73	175
CPCFF-MT	16	4	26	45	51	148	31	58	73	175
CPSFF-MT slumbery keeper	17	4	25	46	52	150	29	62	73	153

Table1: Power consumption comparison for various flip flops

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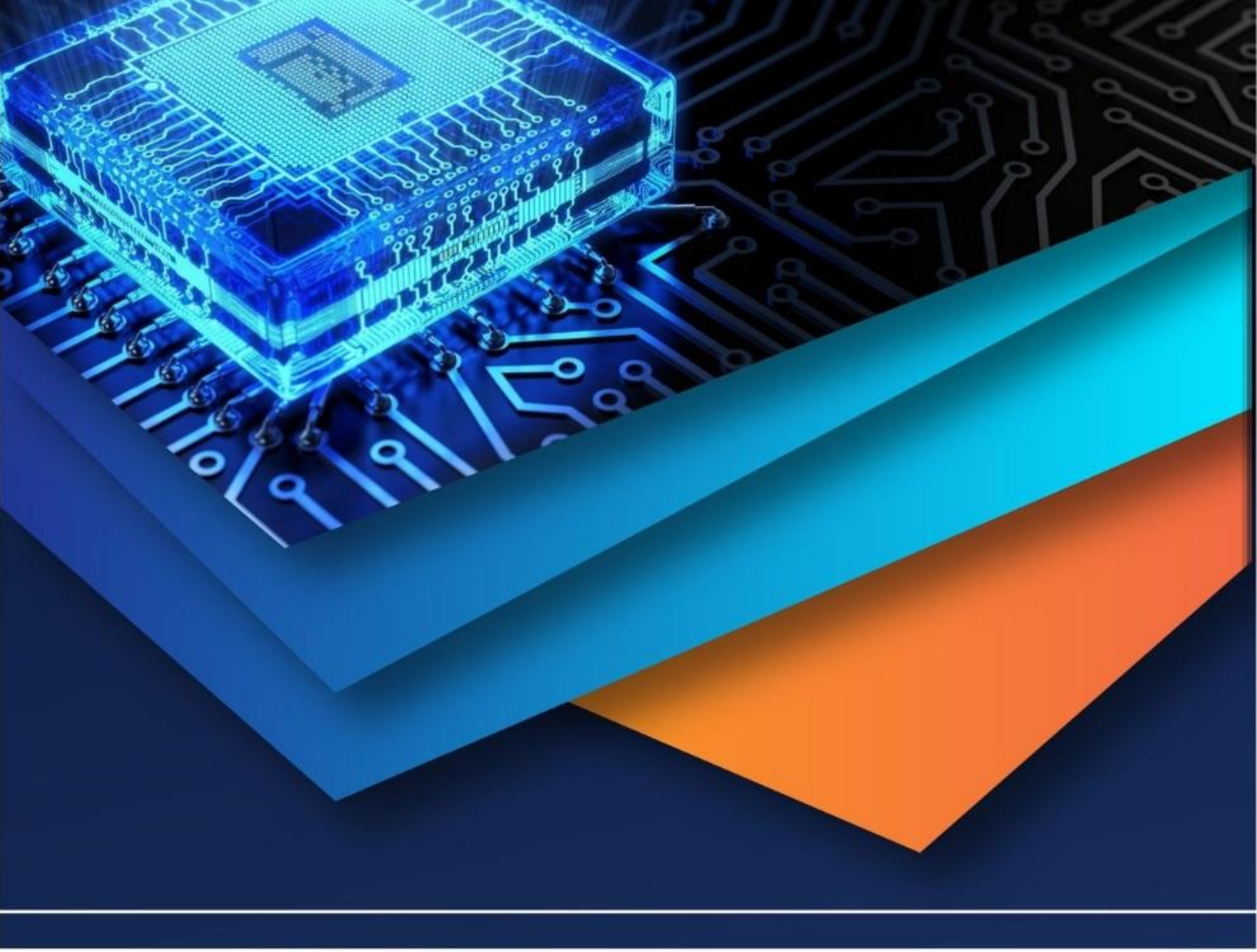

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