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Area Delay Power Efficient Carry Select Adder for Modern Signal Processors

Chandrabose. J[1], M. Ravikumar[2]
[1]M.E VLSI Design, [2]Assistant Professor, ECE
Mahendra Engineering College, Namakkal DT, India

Abstract: ***The area, power-efficient and high speed and data path logic systems forms the largest areas of research in VLSI system chip design. The addition speed is limited by the time necessary to send a carry via the adder. Carry Select Adder (CSLA) is the fastest adders used in several data manipulation processors to perform fast arithmetic operation purpose. From the architecture of the CSLA, it is confident for decreasing the area and delay in the CSLA. This project uses a simple and efficient gate level modification is reduces the area and delay of CSLA. Based on this modification 16, 32, 64 and 128-bit square-root Carry Select Adder (SQRT CSLA) architectures have been improved and compared existing SQRT CSLA architecture. The proposed design is less area and delay to a great extent when compared with the regular SQRT CSLA. This project estimates the performance of the designs with the regular designs in terms of delay area and synthesis are implemented in Xilinx FPGA. The results analysis shows that the result is CSLA is better than the regular SQRT CSLA.***
Keywords: ASIC, CSLA, SQRT,FPGA.

I. INTRODUCTION

To minimize the area and high speed data path logic are the major areas of research in VLSI system design. High-speed addition and multiplication is always a fundamental necessity of high-performance processors. In digital adders, the speed of addition is part by the time necessary to move a carry through the adder. The sum for each bit position in an basic adder is generated serially only after the previous bit position has been summed and a carry propagated into the next position. There are different types of adder designs available CSA, RCA, CLAA which have its own advantages and disadvantages. The main drawback is in the production of carries and many authors considered the addition problem. To solve the carry propagation delay CSLA is created it is decreases the area and delay. The CSLA architecture is used in most computational systems design to moderate the problem of carry propagation delay by separately generating multiple carries and then select a carry to generate the sum. It uses independent ripple carry adders for Cin=0, Cin=1 to generate the resultant sum. The Regular CSLA is not area and speed efficient because it uses multiple pairs of Ripple Carry Adders to create partial sum and carry. The final sum and carry are selected by the multiplexers (mux). This logic can be removed in RCA for Cin=1 to further improves the speed and thus decreases the delay. By use the Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA will achieve lower area. The main application of this BEC logic comes from the low number of logic gates than the Full Adder (FA) structure because the no of gates used will be less. This new SQRT CSLA is developed using ripple carry adders and multiplexers. The architecture of the Modified SQRT CSLA is presented and compared in the paper.

A. Basic Adder Block

The adder block in a Ripple carry adder, BEC and Mux is described. In this we calculate and explain the delay & area using the theoretical approach .Then explain how the delay and area effect the total implementation done in FPGA. The AND, OR, and Inverter implementation of an XOR gate is shown in Fig. 1. The delay and area development methodology considers all gates to be made up of AND, OR, and Not, each having delay equal to 1 unit and area equal to 1 unit. We then add the no of gates in the lengthy path of a logic block that contributes to the maximum delay.

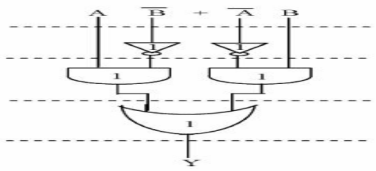


Fig 1: Delay and area evaluation of xor

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The design shows the basic 8 bit addition procedure which includes 8-bit data, a 8-bit BEC logic and 16:8 mux. The addition is performed for Cin=0 and for Cin=1.For Cin=0 the addition is performed by ripple carry adder and for Cin=1 the operation is performed using 8-bit BEC. The result is selected based on Carry in signal from the earlier group. The total delay depends on mux delay and Cin signal from earlier group.

II. BINARY TO EXCESS CONVERTER (BEC)

The basic work is to use Binary to Excess-1 Converter (BEC) in the regular CSLA to get lower area and improved speed of operation. This logic is removed in RCA with Cin=1. This logic is implemented for different bits which are used in the modified design. The main advantage of this BEC logic comes from the fact that it uses low number of logic gates than the n-bit Full Adder (FA) structure. As stated above the main idea of this work is to use BEC instead of the RCA with Cin=1 in order to decrease the area and increase the speed. To remove the n-bit RCA, an n+1 bit BEC logic is required. The structure and the function table of a 8-bit BEC are shown in Figure 2.

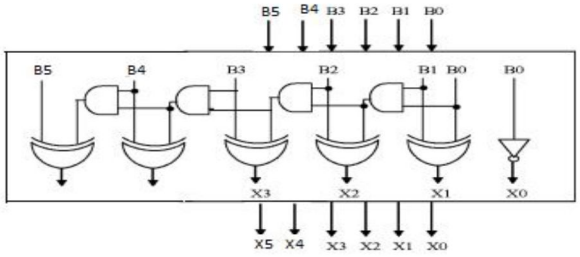


Figure 2 .binary to excess-1 converter

III. ARCHITECTURE OF REGULAR 128-BIT SQRT CSLA

A 16 bit CSA can be designed in 2 different sizes namely uniform block size and variable block size. Similarly a 32, 64 and 128-bit can also be developed in two modes of different block sizes. Ripple carry adders are the simple and compact full adders, but its performance is limited by a carry that must spread from the least-significant bit to the MSB. The various 16, 32, 64 and 128-bit CSLA can also be designed by using ripple carry adders. The speed of a CSA can be enhanced upto 40% by performing the additions in parallel, and reducing the maximum carry delay. Fig 4 shows the Regular structure of 128-bit SQRT CSLA. It includes many ripple carry adders. The carry out of the Group 0 which acts as the selection input to mux which is in group 1, selects the result from the consequent RCA (Cin=0) or RCA (Cin=1). Similarly the remain groups will be selected depending on the Cout from the previous groups. In Regular CSLA, there is only one RCA to achieve the addition of the least significant bits [1:0]. The Cin from the previous parts selects one of the two RCAs. , If the carry-in is 0, the sum and carry-out of the upper RCA is selected, and if the carry-in is 1, the sum and carry out of the lower RCA is selected. For this Normal CSLA architecture, the execution code, for the Full Adders and Multiplexers of different sizes 6:3, 8:4, 10:5 were designed initially. The regular 64-bit, 128-bit CSLA were implemented by calling the ripple carry adders and multiplexers.

IV. ARCHITECTURE OF MODIFIED 128-BIT SQRT CSLA

This architecture is alike to regular 128-bit SQRT CSLA, the only change is that, we change RCA with Cin=1 among the two available RCAs in a group with a BEC. This BEC has a feature that it can perform the alike operation as that of the replaced RCA with Cin=1. Fig 5 shows the Modified block diagram of 128-bit SQRT CSLA.The number of bits compulsory for BEC logic is 1 bit more than the RCA bits. The modified block diagram is also separated into various groups of variable sizes of bits with each group having the ripple carry adders, BEC and corresponding mux. As shown in the Fig.5, Group 0 include one RCA only which is having input of lower significant bit and carry in bit and produces result of sum [1:0] and carry out which is acting as mux selection line for the next group, also the procedure continues for higher groups but they includes BEC logic instead of RCA with Cin=1. Based on the consideration of delay values, the arrival time of selection input C1 of 8:3 mux is before than the sum of RCA and BEC. For remain groups the selection input arrival is later than the RCA and BEC. Thus, the sum1 and c1 (output from mux) are depending on mux and results computed by RCA and BEC respectively. The sum 2 depends on c1 and mux. For the remain parts the arrival time of mux selection input is always larger than the arrival time of data inputs from the BEC's. Thus, the delay of the remaining MUX depends on the arrival time of mux selection input and the mux delay. In this Modified CSLA architecture, the implementation code

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for Full Adder and Multiplexers of 6:3, 8:4, and 10:5 up to 24:11 were designed.

V. RESULTS

The Proposed design in this work has been simulated using Verilog-HDL. The adders (of various sizes 16, 32, 64 and 128) are designed and simulated with Modelsim. After simulation the different size codes are synthesized using Xilinx ISE 9.1i. The simulated V files are imported into the synthesized tool and resultant values of delay and area are noted. The synthesized reports include area and delay values for different sized adders. The similar design flow is followed for both the regular and modified SQRT CSLA of different sizes. From the table it is clear that the delay decreases for 16-bit modified method when compared with regular method. The result table also shows the comparison for the various 32, 64, and 128 bits. The relative values of areas shows that the number of LUT will be more for modified the 16, 32 and 64. This value reduces gradually for 128 bits. For 256 bits the value almost equal to regular method which will decreases more for still higher order bits. Thus the modified method reduces the delay and also area to a great extent.

Table 1 Device utilization summary

Device utilization summary:			
Selected Device : 3s500eft256-4			
Number of Slices:	107	out of 4656	2%
Number of Slice Flip Flops:	182	out of 9312	1%
Number of 4 input LUTs:	53	out of 9312	0%
Number of IOs:	52		
Number of bonded IOBs:	52	out of 190	27%
Number of MULT18X18SIOs:	4	out of 20	20%
Number of GCLKs:	1	out of 24	4%

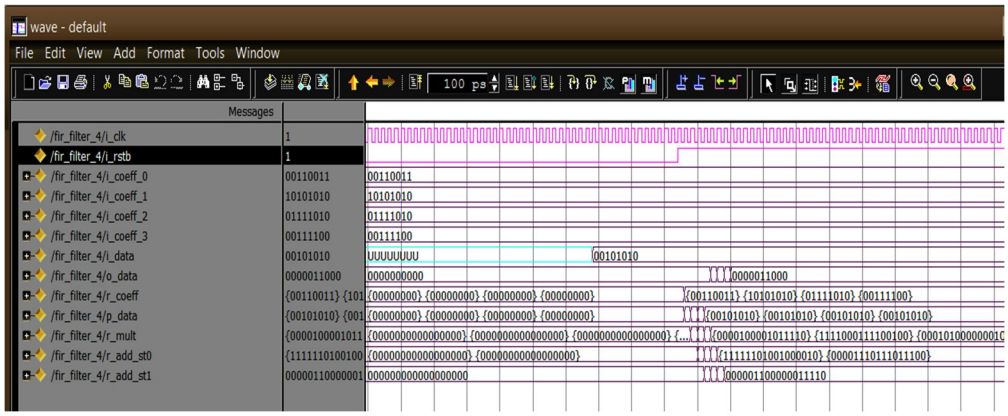


Fig 3.moselsim simulation output

VI. CONCLUSION

An efficient approach is planned in this paper to decrease the area and delay of SQRT CSLA architecture. The reduction in the number of gates is obtained by simply replacing the RCA with BEC in the structure. The compared results shows that the modified SQRT CSLA has a slightly bigger area for lower order bits which further reduces for higher order bits. The delay is reduced to a great extent with the modified SQRT CSLA. Thus the results shows that using modified method the area and delay will reduce thus leads to good alternative for adder implementation for many processors. The modified CSLA architecture is therefore low area and high speed approaches for VLSI hardware implementation. In this project, we evaluated the performance of both sequential and parallel micro programmed FIR filters using SQRT CSA multipliers for different number of taps. Multiplier is the main module and

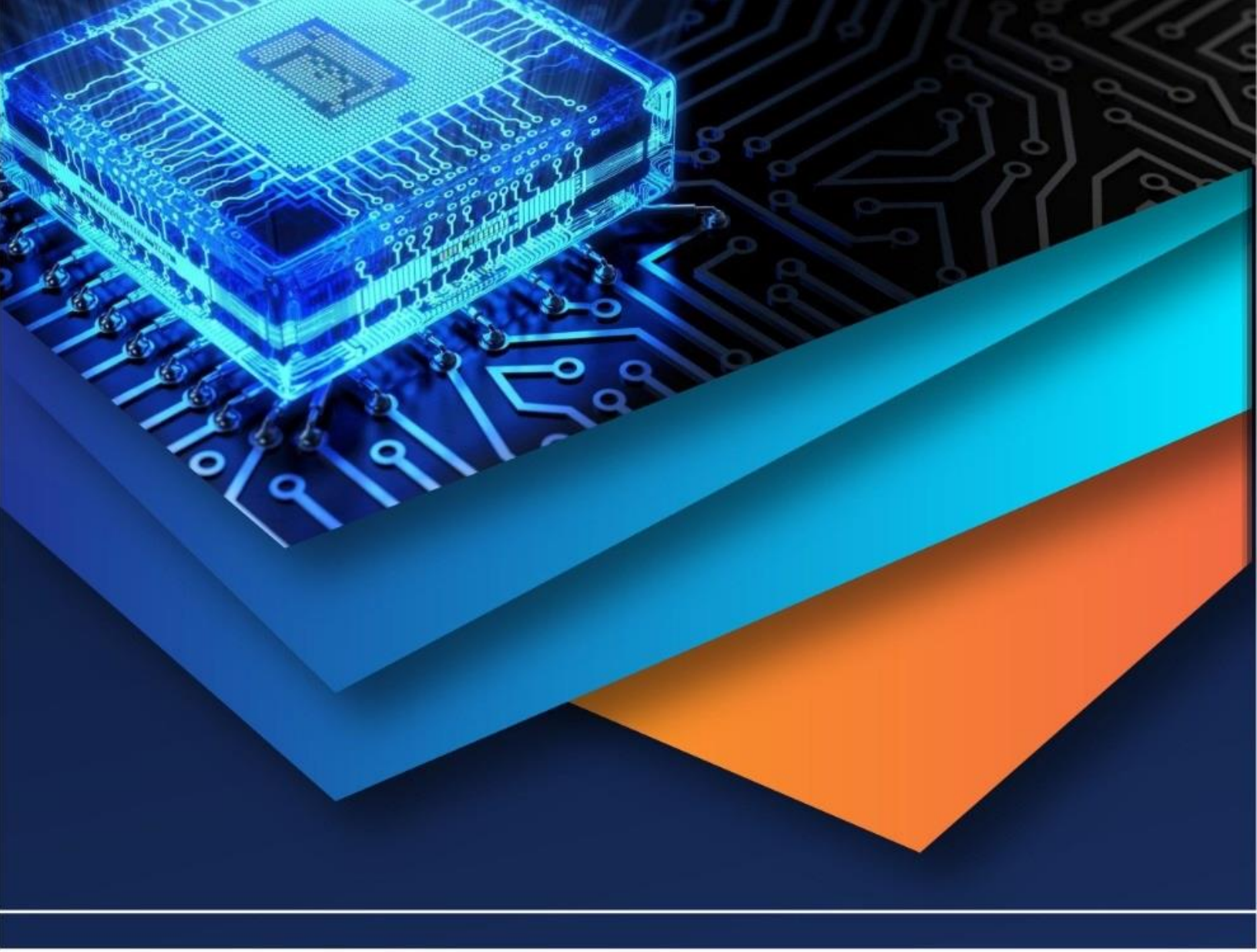
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its performance matters the most while designing a digital FIR filter. Two different variations of carry save adders are designed using Verilog HDL. These adders are then integrated with the micro programmed FIR filters to further analyze the performance based on the area, power consumption and critical path delays. SQRT CSA delivers better performance than traditional adders for both the FIR filter architectures.

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