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FPGA Based Low Power Design of an FIR Filter Using Distributed Arithmetic

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Abstract: ***Standard wireless and mobile communication environments have huge demands on high speed signal processing operations. Finite Impulse Response (FIR) filter is one of the crucial factors in signal and image processing approaches. Traditional FIR filters have the advantage of linear phase, guaranteed stability, fewer finite precision errors and efficient implementation. However, they have a major disadvantage of requirements in higher order than Infinite Impulse Response (IIR) counterpart with comparable performance. Practical issues of higher order of FIR filters are more hardware requirements and power consumption when designing and fabricating the filter. In recent years, there are an increasing number of surveys being focuses on Distributed Arithmetic (DA) approaches for higher order digital FIR filter implementation. DA based multiplication is popular for its potential for efficient memory-based implementation. In this paper, we analyze the multiplier less DA multiplication approaches for higher order digital FIR filter. Many energy efficient DA architectures provide high speed and less area for performing multiplication operation which is absolutely suitable for higher order digital FIR filter implementation. Hence, DA based FIR filter effectively reduces the chip size, delay and power consumption due to storing the multiplication of input values and coefficients in memory as look-up-table (LUT). For reducing the hardware requirements and power consumption of higher order digital FIR filter, various level of DA multiplication approaches like memory based DA and pipeline based DA approaches are discussed and their performances are analyzed in this paper.***
Keywords: ***Distributed Arithmetic (DA) approaches, Memory based multiplier, LUT based multiplier, pipeline based DA approaches.***

I. INTRODUCTION

Digital FIR filter is widely used as a basic tool in various signal and image applications. Also standard wireless and mobile communication has largely demands on digital FIR filter. In digital FIR filter, the transition between a pass-band and adjacent stop-band evaluates the filter efficiency. If these transition band as sharper, then the efficiency of filter is increased significantly. In order to bring the transition band as sharper, higher order of filter is required. Hence, higher order of digital FIR filter helps to increase the performance of digital FIR filter. Many applications in digital communications like frequency channelization, channel equalization, adaptive noise cancellation, noise elimination and several other areas of signal processing require larger order of FIR filters. Implementation of large order FIR filter with help of Multiplication and Accumulation (MAC) through Very Large Scale Integration (VLSI) System design environment is tedious task. To overcome this difficulties, distributed arithmetic (DA) based multiplication is used for digital FIR filter. In DA based multiplication, pre-computed values for fixed multiplications are stored in memory as LUT; hence it is referred as multiplier less distributed arithmetic calculation. Large endeavors have been proposed the approach of DA for digital FIR filter. This paper reports the various levels of DA approaches for digital FIR filter design. Initially, memory based DA multipliers are introduced by crosier in 1973. The complicated multiplication-accumulation operation is converted into shifting and adding operation when DA algorithm is directly applied to realize linear time invariant (LTI) system.

However, the scale of the LUT will increase exponentially with the coefficient. In [Shunwen Xiao, 2010], improved version of DA is proposed to reduce the storage resource. Systolic decomposition of DA based inner-product computation arithmetic approaches are used to design the optimization of one- and two- dimensional fully pipelined computing structures [Pramod Kumar Meher, 2008] for areadelay- power efficient implementation of digital FIR filter. In 2D pipelined computing DA structures, independent serial-toparallel (S/P) and parallel-to serial (P/S) are used for collecting coefficient values and producing filter output respectively. Further to improve the structures of DA based FIR filter 2D pipelined computing DA structures are modified [Pramod Kumar Meher, 2010]with help of single S/P and P/S for filtering operation. In [Yajun Zhou, 2011], a larger LUT is divided into smaller LUT to decrease the required memory units. In addition, pipelined structures are introduced in this approach [V. Sudhakar, 2012] to reduce the asynchronous of input arrival. However this approach causes larger area due to insufficient adder structure. To overcome

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this problem, Carry Save Adder (CSA) is used in pipeline based DA structures [Pramod Kumar Meher, 2011].

In this paper, various levels of DA approaches like memory (LUT) based DA and pipeline based DA are discussed and their performances are analyzed for digital FIR filter. Initially, the structure and algorithm of memory based DA is explained in section II. The improved memory based DA and their influences are briefly analyzed in section III. In section IV pipeline based DA structures are discussed. The results for various DA approaches are analyzed in section V. Finally the conclusions are arrived in section VI.

II. MEMORY BASED DA MULTIPLIER

In memory based DA multiplier, "memory-based structures" or "memory-based systems" are used either as a part or whole of an arithmetic unit. When compared to MAC structure for performing multiplication, memory based structures are more regular and have many other advantages such as greater potential for high-throughput and reduced-latency implementation. Since memory access time is much shorter than usual multiplication time. In memory based DA approaches, a LUT is used to store all possible values of inner products of a fixed N-point vector with any possible N-point bit-vector. Therefore the inner-products are implemented in a straight-forward way, the memory size of DA approaches increases exponentially with the inner-product length [Pramod Kumar Meher, 2010]. The structure of memory based DA multiplier is illustrated in fig 1. Let A be a fixed coefficient and X be an input word to be multiplied with A. If we assume X to be an unsigned binary number of word-length L, there can be 2L possible values of X, and accordingly, there can be 2L possible values of product C=A.X. Therefore in memory based DA multiplication 2L words is required to be used as look-up-table consisting of pre-computed product values corresponding to all possible values of X. The principle os memory based DA multiplication is as follows:

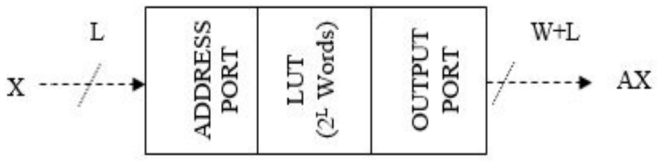

Fig. 1 Structure of Memory-Based DA Multiplier

III. IMPROVED MEMORY (PARALLEL) BASED DA MULTIPLIER

In previous section, memory based DA approaches are described for digital FIR filter. This approach requires more memory size to store the multiplication of coefficient and input values. To reduce the memory size, Offset Binary Coding is used in improved memory based DA multiplier. In this improved memory based DA multiplier LUT size is divided to more than two to improve the speed and reduced the memory size. The design of improved memory based DA multiplier approach as follows From equation (2), Xm can be represented as

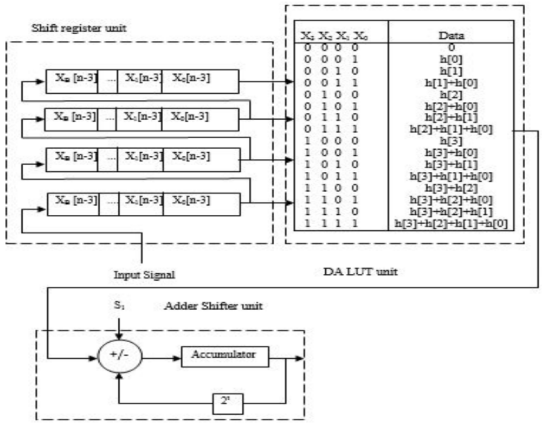

Fig. 2 Memory (LUT) based DA multiplier implementation for 4-tab digital FIR filter

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Through this algorithm the size of LUT is partitioned and speed is improved. The LUT table for improved memory based DA structure is shown in table 1. Further divided LUT's are subdivided in order to reduce memory size and increase the speed in [Ramesh .R, 2012]. Table 1 shows that decomposition of memory size into two parts. Second half of LUT is the inverse symmetry of first half of LUT which are indicated in different color. Table 1 LUT of improved memory based DA architecture for 4-tab digital FIR filter.

IV. PIPELINE BASED DA ARCHITECTURE

The parallel approach for DA based multiplication is described in section III. In this section, further to increase the speed of multiplication process, pipelining technique is introduced on parallel DA approach. In order to implement the pipelining technique, LUTs in table1 are further subdivided into four parts. As shown in fig 1, after taking output form LUT shift/addition unit is processed to provide multiplication results. When dividing the LUT size, two or more shift/addition blocks are required to provide multiplication results. Therefore in general, the outputs of different LUTs are reached to shift/addition block in asynchronous manner. In order to bring synchronism between outputs of LUTs (memories) and input of shift/addition block pipelining techniques are used in this section with help of storage registers. The architecture or pipeline based DA approach is
shown in fig 2 [V. Sudhakar, 2012].

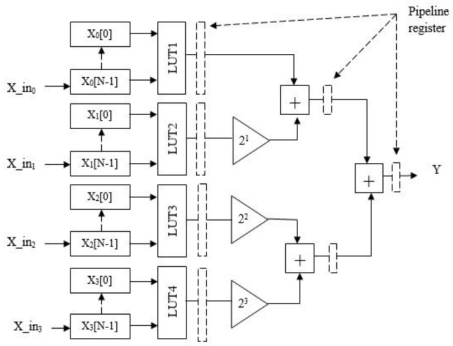

Fig. 3 Pipeline based DA architecture

Dotted line of fig 2 indicates the pipeline register which protect from asynchronous effect. Hence, speed of DA architecture is improved significantly when compared to parallel based DA approach. In shifting and adding block, Ripple Carry Adder (RCA) is used for addition part. This adder structure is replaced by Carry Save Adder (CSA) in [Pramod Kumar Meher, 2011] for further improve the performance.

V. RESULTS AND DISCUSSIONS

In this paper, various level of distributed arithmetic (DA) based multiplication is analyzed for digital FIR filter. Initially memory based DA approach is analyzed for performing multiplication results. In this technique, multiplication results for input samples and data coefficients of FIR filter are pre computed and stored in memories as LUT. The procedure for memory based DA implementation is illustrated in fig 2. The performance of memory DA based FIR filter is better than MAC based FIR filter in terms of delay and speed.

Unfortunately, area utilization of memory based DA multiplication is larger than MAC based multiplication because storage size of memory is increased in order to hold the pre-determined multiplied values. Theoretically 60% of area has increased in DA based multiplication when compared to conventional memory based multiplication. To overcome this problem, memory based DA approach is improved with help of partition of size of LUT. The method of LUT partition is described in section III and partitioned LUT for 4-tab FIR filter is shown in table 1. In this table, inverse symmetry of first half data elements are stored in second half data elements. Design procedure for this technique is theoretically evaluated in section III. This procedure effectively reduced the size of memory as MAC based multiplication. In addition, improved memory based LUT reduces 75% of delay for performing multiplication process. The performance comparison of memory and improved DA based 8-tab FIR filter is illustrated in table 2 [D.Kalaiyarasi, 2014]. Table 2 performance comparison of memory
and improved DA based 8-tab FIR filter ~ Analyzed theoretical values *indicates analysis results from [V. Sudhakar, 2012] and [Pramod Kumar Meher, 2011] Table 2 illustrates the performance of conventional MAC based, memory and improved memory DA

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based FIR filter in terms of slices, delay and power. It proves that memory DA based FIR filter gain 60% of more area than MAC based FIR filter, but it effectively reduces the 75% of delay than MAC based FIR filter. In improved memory DA based FIR filter, memory size has reduced as same as MAC based FIR filter as well as 77% of delay has reduced. Hence, Improved (parallel) memory DA based FIR filter is one of the best effective tools for growing wireless and signal processing technologies.techniques on parallel DA architectures are investigated in section IV. This method suggests that effective reduction of delay due to providing synchronism LUT and shift/addition unit. Hence as parallel based DA multiplication method, pipeline based DA approach also one better performance in terms of area and delay.

VI. CONCLUSION

In this paper, studies of various levels of DA approaches are presented with help of standard benchmarks. DA based approaches performs the multiplication without help of multiplier circuit. It is one of the main advantages in DA approach. Analysis reports of this paper suggests the reduction of VLSI concerns (area, delay and power) in different levels of DA approaches like memory based DA, improved memory (parallel) based DA and pipeline based DA for digital FIR filter. Parallel and Pipeline based DA approaches are effectively performed without help of multiplier circuit than MAC based multiplication. Hence, finally this paper concludes the improved memory (parallel)/pipelined based will be helpful to increase the performance of digital FIR filter. In future, improved pipelined or parallel based FIR filter will be designed for wireless and mobile communication
application.

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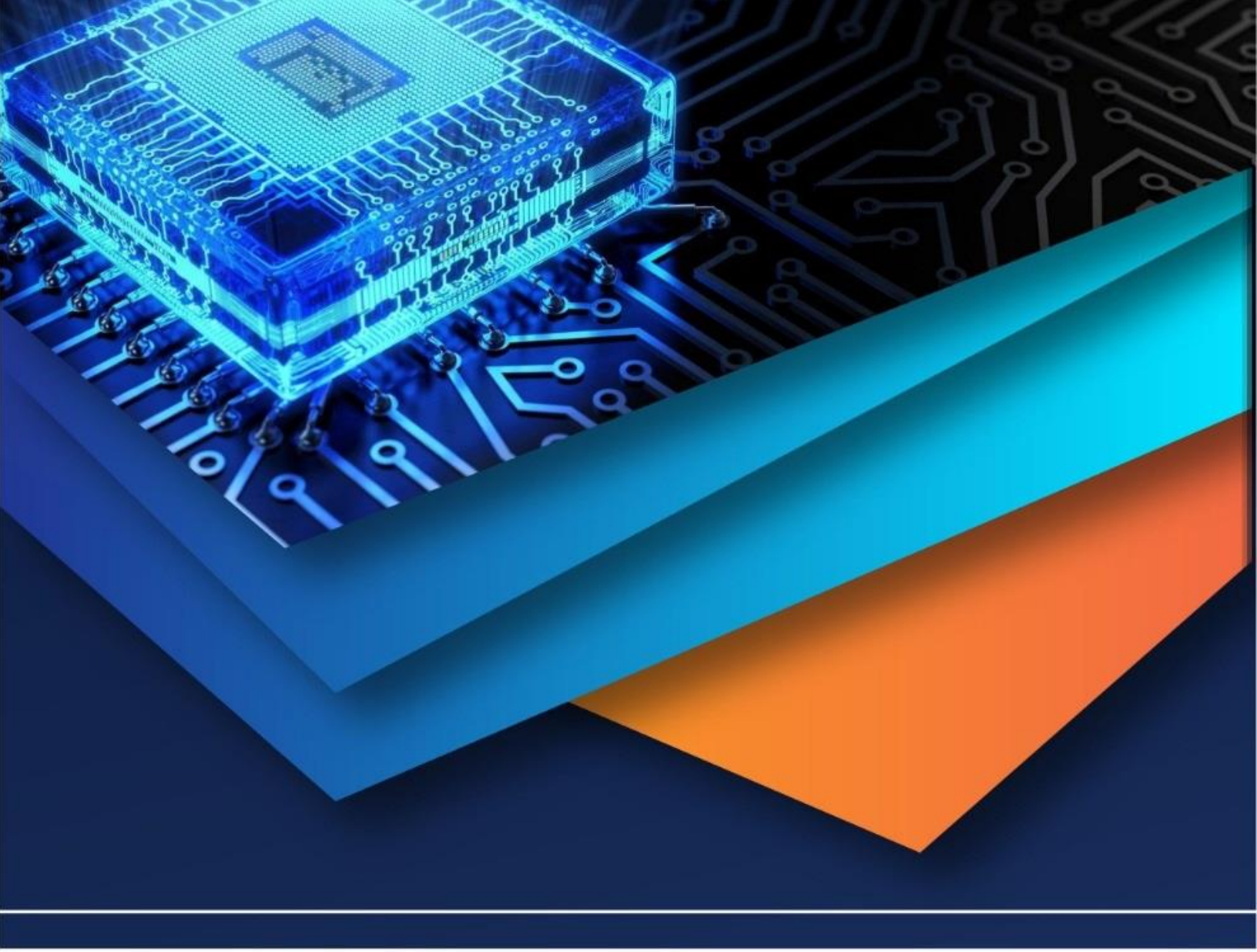

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