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Adaptive Simplified Successive Cancellation for Polar Codes Based on Frozen Bits

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Abstract: ***Polar codes have been recently proposed as the first low complexity of error correcting codes for wireless channels that can provably achieve the capacity of symmetric binary-input memory less channels. Here, the bit error rate performance of finite-length polar codes is performed under Successive-Cancellation decoding. In existing ASM controller is used in high radix computation, utilizes high hardware resources that increase implementation complexity with reduced performance. To overcome this by using proposed architecture, the length of polar code N can be reduced from N-1 to N/2-1 from the decoding latency of the code, it can replace high hardware resources in merged processing elements to control the decoding by state transition method results low power consumption. The 8-point polar coder is proposed that can be easily combined to form efficient N-point polar coder architectures, so that it can achieve parallelism and bit-pipelining techniques result in low power operation and easily expandable architecture with respect to data and/or co- efficient word length. Finally, in this paper the position of frozen bits and architecture of 8-bit SC decoder was analyzed. Our coding scheme also achieves the capacity of the physically degraded channel with better error control performance.***

Keywords: polar codes, frozen bits, Simplified Successive-Cancellation decoding, decoding latency reduction, merged processing elements.

I. INTRODUCTION

Polar codes are the error correcting code the capacity of those codes can be achieved with efficient encoding and decoding algorithm for any symmetric binary memory less channels with explicit construction which produce low complexity [1].The complexity for the block length N of encoding and decoding can be calculated through O (N log N) [2]. Code length of the polar code is $N=2^n$, which requires very long code length. Because of the successive cancellation decoding (SC) scheme, large code length tends to a long decoding latency.

Despite the long code length the polar code is suffer from many problems such as lossless and lossy source coding [3], problems with side information, multiple access channel, etc. And SC decoder also suffer from the long block length by the high latency , so that it can be operate at recursive approach which is multiple bit decision for minimize the decoding length of polar code into pair decoding of length N/2 constituent codes rate as zeros or ones. Due to long latency and low throughput problem SCL is suffer which is corresponding to early SC decoder. To reduce the latency of SCL decoders multiple bit decision approach has been proposed with low power consumption using asynchronous SC decoder. Compared to typical synchronous SC decoders, the proposed Simplified SC decoder operates at much lower clock frequencies and decodes a codeword in one long clock cycle. Hardware usage is high for synchronous decoder combinational architecture. High latency for synchronous decoder is occurred due to shorter block length N=4**.** The input u1 and u2 perform the process through the Function (F) and Gate (G). Computation F and G can be used in merged processing elements (MPE). Output of the function is out_F and the gate has produces the two output which is out_G_0 and out_ G_1.

It can be calculate as follows

Out_F=sign (u1) sign (u2) min(|u1|,|u2|)

Out_G0= u1+ u2

Out_G1=u2-u1

To solve that problem the present work is motivated by using we reduce the long decoding latency of the polar codes by using the merged processing elements (MPE) of F and G computation. Simplified SC (SSC) decoder architecture was proposed by frozen bits and information bits.

II. POLAR CODE

Polar encoding is a linear block error correcting code .It can be denoted by the generator matrix $X=G^{\otimes n}U_N$ where N=2 is the code length, U_N is the permutation matrix of bit reversal and G is the Kronecker power of the kernel matrix. The generator matrix for

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code word length is applying by generating the Kronecker power to kernel matrix. For the generator matrix the co de length is calculated by x=u.

$$G_2 \otimes^3 = \begin{pmatrix} 1\,0\,0\,0\,0\,0\,0\,0 \\ 1\,1\,0\,0\,0\,0\,0\,0 \\ 1\,0\,1\,0\,0\,0\,0\,0 \\ 1\,1\,1\,1\,0\,0\,0\,0 \\ 1\,0\,0\,0\,1\,0\,0\,0 \\ 1\,1\,0\,0\,1\,1\,0\,0 \\ 1\,0\,1\,0\,1\,0\,1\,0 \\ 1\,1\,1\,1\,1\,1\,1\,1 \end{pmatrix}$$

$$X = [u_0\ u_1\ u_2\ u_3\ u_4\ u_5\ u_6\ u_7]\ G_2 \otimes^3$$

The block length of polar code (n, m) can be generated through m-bit source message which is transmitted to n-bit message X= (u0,u1,u2,…..,un-1) by the reliability of n-bit message of u is multiplied with the generator matrix nxn . From the long block length of SC decoder suffer from high latency , so that it can be operate at multiple recursive divide and conquer approach minimize the problem of decoding the length of polar code into pair decoding of length N/2 constituent codes. If the constituent code is 0, the recursion can be simplified as this case decoded recursion can be replaced with 1, thereby avoiding the delay and computation.

The input vector of encoder as x€ F_2^N consist of information part if and a frozen part x_F^c , where f is chosen in according to polar code design rule of binary signal function . Frozen part of x_F^c is fixed up to zero in here. A frozen bit indicator vector b is a 0-1 vector of length N. The receiver can be calculates a vector l=(l1,….l_N) with

$l_i = \log(P(v_i|u_i=0) - P(v_i|u_i=1))$

and connect it into SC decoder

III. SUCCESSIVE CANCELLATION DECODING

The polar code with SC decoding can achieve the capacity of binary symmetric memory less channel. There are many other algorithm can be used to improve the error rate performance in finite block length. We have use SC decoding in this section and other algorithm of polar code such as Belief propagation (BP) decoding, Successive Cancellation List (SCL) decoding and Sphere decoding.

Let u_i^N be the input sequence to the polar encoder, v_i^N be the output. The SC decoding can be sequential manner in nature. The estimation of the bit u_i based on the received vector v and estimation of $u\hat{}_1^{i1}$ pervious bit u_1^{i-1}. Let

$$L_N^{(i)}(v,u\hat{}_1^{i-1}) = \frac{WN(i)(v,u\hat{}_1^{i-1}|u_i=0)}{WN(i)(v,u\hat{}_1^{i-1}|u_i=1)}$$

u_i can be estimated as

$$u\hat{}_i = \begin{cases} 0 \text{ if } L_N^{(i)}(v,u\hat{}_1^{i-1}) \geq 1 \ \&i€f^c \\ 1 \text{ if } L_N^{(i)}(v,u\hat{}_1^{i-1}) < 1 \ \&i€f^c \\ \text{Frozen bit otherwise} \end{cases}$$

For the N length of polar decoding can requires totally 2(N-1) clock cycles by the decoder. It has 50% of largest hardware efficiency in each active stage which means higher than half merged processing element (MPEs) are idle at same time, this is happen because of the previous code depend on the estimation of current bit, which forces all the code bits can produce successive

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output. Fast decoding can be achieve by look ahead techniques, the loop computation can be reformulated which pre calculate all possible output of next code bit and then select proper one with multiplexer. Among all possible part only one with short latency and low hardware complexity can be selected.

IV. SIMPLIFIED SC DECODER ARCHITECTURE

In here, the proposed Simplified SC (SSC) decoder architecture was used to removing the zero node trees (frozen bits) and replacing all one node trees(information bits) by matrix multiplication. Decoding in the system could be made by frozen bit indicator vector. The input of the system is U= (0, 1), the output V and transition probabilities {W (v|u): u€U, v€V} where W is a discrete memory less channel. In each use of system a codeword u€f_2N is transmitted and channel output vector v€VN is received. The number of required decoding procedure for the polar code with length N is N/2. Decoding procedure for the polar code length is N=8.For each stage s_i is active in 2^{s}_{i-1} times and it has N/2si MPE, the numbe r of MPE calculations can be defined as below.
of MPE = N/2x log2N

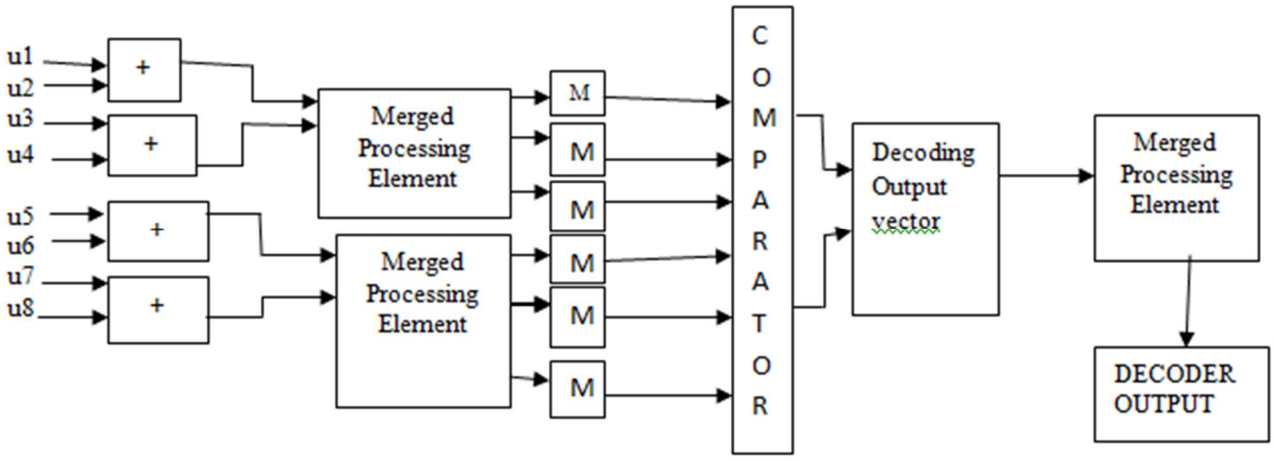

Fig.1 Proposed architecture of 8-bit SC decoder

The decoding latency of 8-bit SC decoder can reduce about 58% and the number of MPE calculation by about 60%. Position of frozen bits and information bit can be determined by using channel polarization technique. The first half the input bits are changed into frozen bits in information bit (u1~uN/2) which is located. By the loss of information bits in previous section is formed according to the rank of the frozen bit position in the second half of the position are occurred based on changes in number of frozen bits in second half (u N/2+1~uN).Decoding of the bit is done in the reverse manner with respect to encoding. It required two separate decoding sections for the block length which are 4 for decodes the code C1 and C2. The input bits u1, u2, u3 and u4 are frozen bits and u4, u6, u7 and u8.

For the N length of polar decoding can requires totally 2(N-1) clock cycles by the decoder. It has 50% of largest hardware efficiency in each active stage which means higher than half merged processing element (MPEs) are idle at same time, this is happen because of the previous code depend on the estimation of current bit, which forces all the code bits can produce successive output. Fast decoding can be achieve by look ahead techniques, the loop computation can be reformulated which pre calculate all possible output of next code bit and then select proper one with multiplexer. Among all possible part only one with short latency and low hardware complexity can be selected. The input from the merged processing element is counted in iteration count. For each input bit is counted in iteration count from that the count value is increased. After counting the input bit the performing the operation processing element. The decoded input is performs the operation successive cancellation in processing element of function generator to store the output in the buffer. Decoding is the opposite process that conversion of encoded format back to the original sequence of characters. The advantage is low power consumption, reduces switching activities and provides area efficient architecture. It can be used in tele- communication, mobile communication , hard drives, memory.

V. SIMULATION RESULT

In this paper I have designed the proposing technique. This process is designed using Verilog. The RTL description is synthesis and simulated in Xilinx ISE 13.2i. The simulated wave forms are presented below.

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The 64-bit input data is given as input to polar encoder. It performs the encoding operation which generated the number randomly such as 1 or 0 using simplified successive cancellation decoder. The noise in the generated random signal can be replaced by the de blocking filter. After encoding the decoder output is obtained using simplified successive cancellation logic and merged processing element. The merged processing array performs the butterfly operation of FFT to produce decoding output as shown in fig 2.

Fig2. Output signal

The simulation using Quartus II is resulted as the power consumption of the total thermal power dissipation is 55.96mw. It has low user provided insufficient toggle rate data. Compared to existing process it can reduce the delay by using the proposed architecture of Simplified Successive Cancellation (SSC) .

VI. CONCLUSION

The latency of polar code can reduce by using Merged Processing Element of proposed architecture by analysis the position of frozen bit and proposed architecture of Simplified SC (SSC) decoder. A very low utilization rate was achieved by the use of butterfly-based 8-point polar code architecture .The technique parallelism and bit-pipelining result in low power consumption is 55.96 mw with reduce area and delay.

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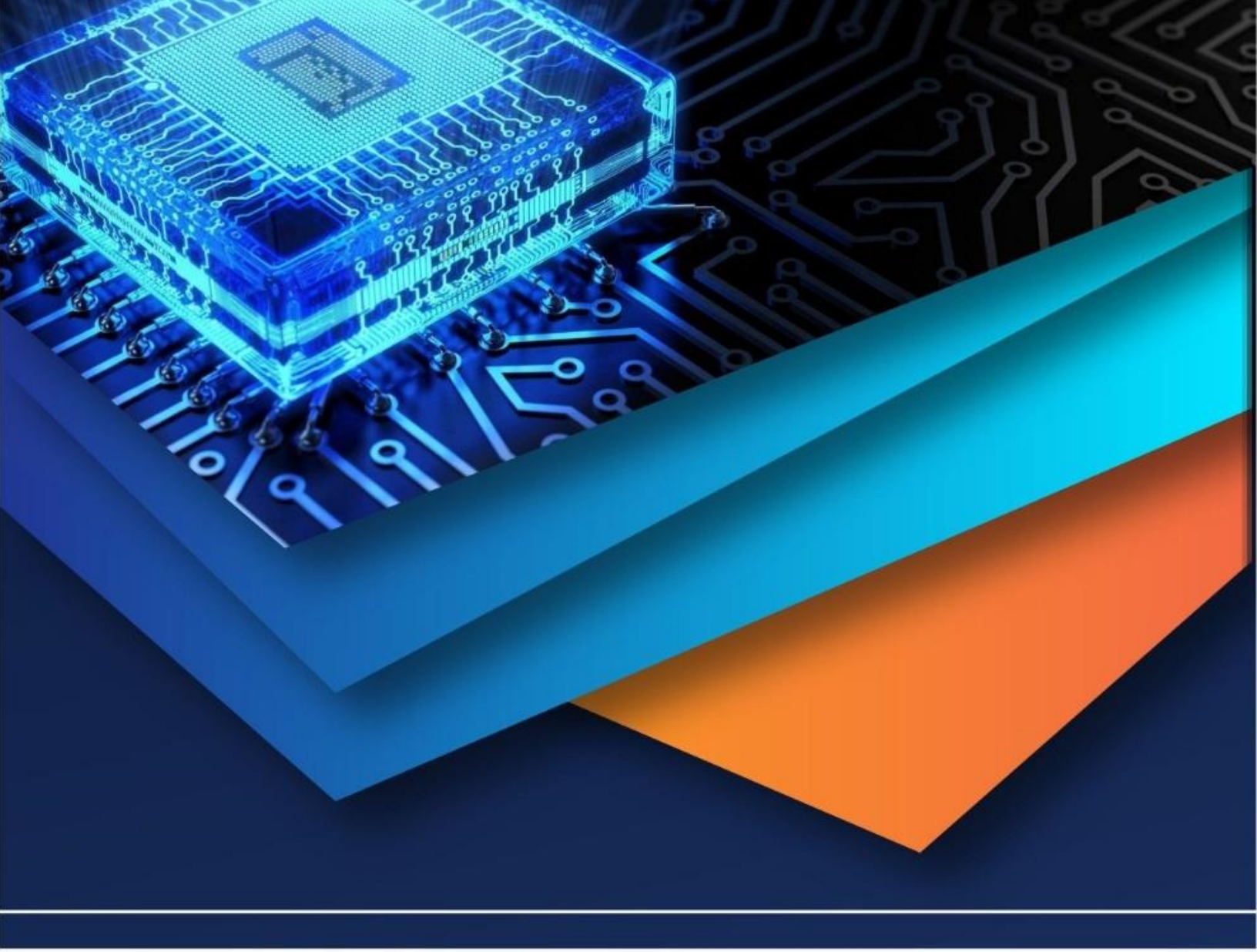

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