iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 5 **Issue:** IV **Month of publication:** April 2017

DOI: http://doi.org/10.22214/ijraset.2017.4122

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

Volume 5 Issue IV, April 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

Design and Implementation of UART with DFT-BIST for Data Communication

P. Surendar [1], G. Gopalakrishnan [2]
[1]PG Scholar, [2]Assistant Professor, Mahendra Engineering College, Namakkal DT, Tamilnadu.India

Abstract : ***The increasing growth of VLSI technology has resulted in the difficulty of testing. Design and test engineers have no choice but to accept new responsibilities that had been performed by groups of technicians in the previous years. Asynchronous serial communication is generally implemented by Universal Asynchronous Receiver Transmitter (UART), commonly used for low distance, low speed, low cost data exchange between peripherals and processor.UART allows full duplex serial communication link. It is also used in data communication and control system. The need for realizing the UART function in a single or a very few chips. The design systems without full testability are open to the increased possibility of product failures and missed market opportunities. Also, there is a need to ensure the data transfer is error proof. In This paper targets the introduction of Built-in self test (BIST) with DFT logic and Status register to UART, to overcome the above two constraints of testability and data integrity. The 8-bit UART with status register and BIST module is coded in V HDL and synthesized and simulated using Xilinx XST and modelsim version 6.3 and realized on Vertex 5 FPGA. The result shows that this model eliminates the complexity, and analysis shows the power and utilization both are minimized by the design.***
Index Terms : UART, BIST, Error check, Status register, LFSR.

I. INTRODUCTION

Manufacturing processes are extremely tough, inducing manufacturers to consider testability as a requirement to assure the functionality and the reliability of each of their designed circuits. The most popular test techniques is called Built-In-Self-Test (BIST). A BIST Universal Asynchronous Receive/Transmit (UART) has the target of firstly to satisfy specified testability requirements, and secondly to generate the lowest-cost with the highest performance implementation. UART has been an important input/output tool for decades and is still mostly used. Although BIST techniques are becoming most common in industry, the additional BIST circuit that increases the hardware overhead increases. In This paper focuses on the design of a UART chip with DFT BIST architecture using Field Programmable Gate Array (FPGA) technology. The paper describes the problems of Very-Large-Scale-Integrated (VLSI) testing followed by the behavior of UART circuit using VHISC Hardware Description Language (VHDL). In the implementation part, the BIST technique will be incorporated into the UART design will synthesused and implemented to the target FPGA device and the power ,utilization and delay are measured and compared with existing system. The UART is targeted at broadband modem, cell phone, base station and PDA designs.

A. VLSI Testing Problems

Now highly integrated multi-layer boards with fine-pitch ICs are virtually impossible to be accessed physically for testing. Traditional board test methods which include functional test, only accesses the board's primary I/Os, providing limited coverage and poor diagnostics for board-network fault. In circuit testing, another traditional test method works by physically accessing each wire on the board via costly "bed of nails" probes and testers. To identify reliable testing methods which will reduce the cost of test equipment, a research to verify each VLSI testing problems has been conducted. The major problems detected so far are as follows:

1) Test generation faults
2) Input and output combinatorial problems
3) The gate to I/O pin ratio problems**.**

II. UNIVERSAL ASYNCHRONOUS RECIEVER AND TRANSMITTER

The final piece to this serial puzzle is finding something to both create the serial packets and control those physical hardware lines. Enter the UART. A universal asynchronous receiver/transmitter (UART) is a block of circuitry responsible for implementing serial communication. Essentially, the UART acts as an intermediary between parallel and serial interfaces. On one end of the UART is a bus of eight-or-so data lines (plus some control pins), on the other is the two serial wires - RX and TX.

©IJRASET: All Rights are Reserved

Volume 5 Issue IV, April 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

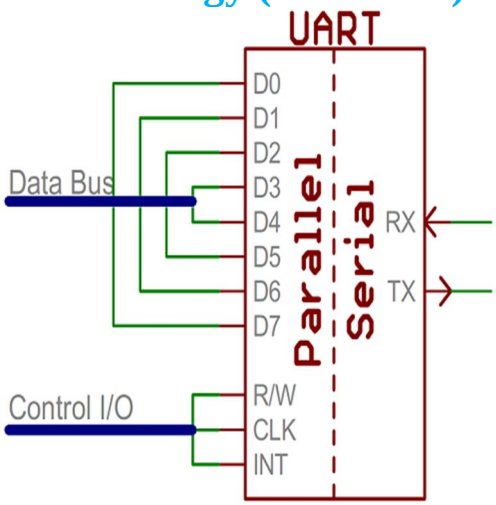


Fig.1. Parallel & Serial UART

UARTs do exist as stand-alone ICs, but they're more commonly found inside microcontrollers. You'll have to check your microcontroller's datasheet to see if it has any UARTs. Some have none, some have one, some have many. As the R and T in the acronym dictate, UARTs are responsible for sending and receiving serial data. On the transmit side, a UART must create the data packet - appending sync and parity bits - and send that packet out the TX line with precise timing (according to the set baud rate). On the receive end, the UART has sample the RX line at rates according to the expected baud rate, pick out the sync bits, and spit out the data. More advanced UARTs may throw their received data into a buffer, where it can stay until microcontroller comes to get it. UARTs will usually release their buffered data on a first-in-first-out (FIFO) basis. Buffers can be as small as a few bits, or as large as thousands of bytes.

III. BUILT IN SELF TEST

Built-in Self Test, or BIST, is the technique designing additional hardware and software features into integrated circuits to allow to perform self-testing.Testing of their own operation (functionally, parametrically, or both) using their own circuits, thereby reducing dependence on an external automated test equipment (ATE).BIST is a Design-for-Testability (DFT) technique, because it makes the electrical testing of a chip easier, faster, more efficient, and less costly. The concept of BIST is applicable to just about any kind of circuit, so its implementation can vary as widely as the product diversity that it caters to. As an example, a common BIST approach for DRAM's includes the incorporation onto the chip of additional circuits for pattern generation, timing, mode selection, and go-/no-go diagnostic tests.

A. Operation of BIST

LFSR is used to generate pseudo-random test pattern for the BIST. A LFSR is a shift register where the input is a linear function of two or more bits (taps). It consists of D flip-flops and linear exclusive-OR (XOR) gates. The bits contained in selected positions in shift register are combined in some sort of function and the result is fed back into the register's input bit. The selected bit values are collected before the register is clocked and the result of the feedback function is inserted into the shift register during the shift, filling the position that is emptied as a result of the shift. The bit positions selected for use in the feedback function are called "taps". The largest state space possible for such an LFSR will be 2n-1, all possible values except the zero state. All zero is not allowed in LFSR, as it will always produce 0 in spite of how many clock iteration. Because each state can have only once succeeding state, an LFSR with a maximal length tap sequence will pass through every non-zero state once and only once before repeating a state. For BIST, UART is set in an internal loop back mode to test both the transmitter and receiver of the UART. This will loop-back the serial data and transmit the data back to the receiver. For the BIST, the test pattern is generated by LFSR as mentioned in the last section and the pattern is loaded to the FIFO of the UART transmitter. Each test byte is padded with start, parity and stops bits and sent from transmitter and looped back to receiver. The receiver will extract the data from frames received and loads to receiver FIFO.

©IJRASET: All Rights are Reserved

Volume 5 Issue IV, April 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

B. BIST Memory Design using HDL

A mechanism that allows a machine to test itself is called built-in self-test (or BIST). It can generate patterns based on a variety of algorithms, each focused on a particular type of circuitry or fault type. Comparison function has a number of unique implementations including actual comparators as well as signal analysers. In this project we will design Memory BIST (MBIST), which uses one or more algorithms specifically designed for testing memory faults. BIST structures generate patterns and compare output responses for a dedicated piece of circuitry. You can implement BIST on entire designs, design blocks or structures within design blocks. Pattern generation as well as output-comparison circuitry can vary depending on the design.

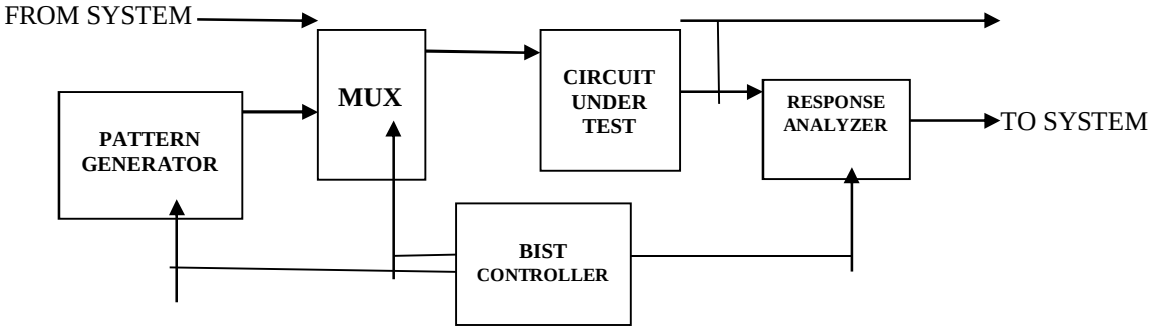


Fig. 2: Circuit with surrounding built-in self-test circuitry

IV. EXPREIMENTAL RESULT

The verilog HDL coding and simulation of the design are done in Xilinx tool . The operating clock frequency used for simulation is 50 MHz. The baud rate set is 9600bps. Data word length is 8-bits.

A. Simulation Results

The fig shows the serial transmission of data. Data transmitted is “10101010”. This 8-bit data is loaded to transmit shift register and start, stop & parity bits are added to form the frame inside TSR and sent to TXD. When the reset is 0 and transmit is 1, the transmitter starts transmitting the data. I.e. the data starts shifting out from the transmitter shift register. Since the desired baud rate is 9600bps, the bits are shifted out on TxD line at the interval of 50MHz/9600=5208 clock cycles. Similarly all the bits are sent. The serial transmission is observed at TXD pin along with frame format (1 logical low start bit, 8-bit data (LSB to MSB), parity bit and finally logical high stop bit).

Table 1 Device Utilization Summary

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	79	19,200	1%
Number used as Flip Flops	79		
Number of Slice LUTs	152	19,200	1%
Number used as logic	152	19,200	1%
Number using O6 output only	152		
Slice Logic Distribution			
Number of occupied Slices	60	4,800	1%
Number of LUT Flip Flop pairs used	165		
Number with an unused Flip Flop	86	165	52%
Number with an unused LUT	13	165	7%
Number of fully used LUT-FF pairs	66	165	40%
Number of unique control sets	14		
IO Utilization			
Number of bonded IOBs	44	360	12%

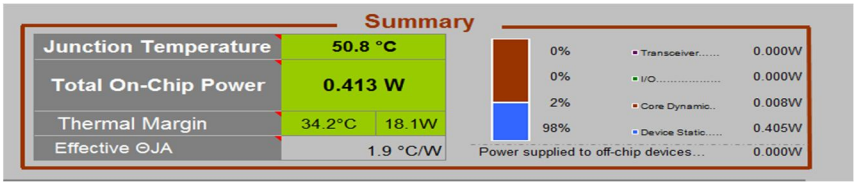
©IJRASET: All Rights are Reserved

Volume 5 Issue IV, April 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

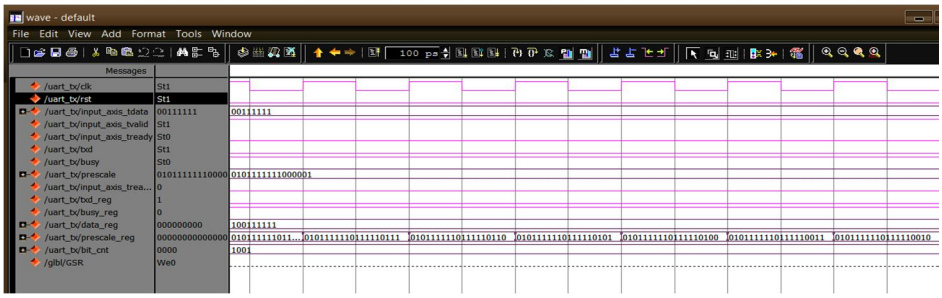
Specific Feature Utilization			
Number of BUFG/BUFGCTRLs	1	32	3%
Number used as BUFGs	1		
Total equivalent gate count for design	1,936		
Additional JTAG gate count for IOBs	2,112		

B. Power Analysis

The above power analysis shows the process of power calculation for the different gates used in the process of pseudo exhaustive tests. The power analysis module tabulated below.



C. Simulation Output



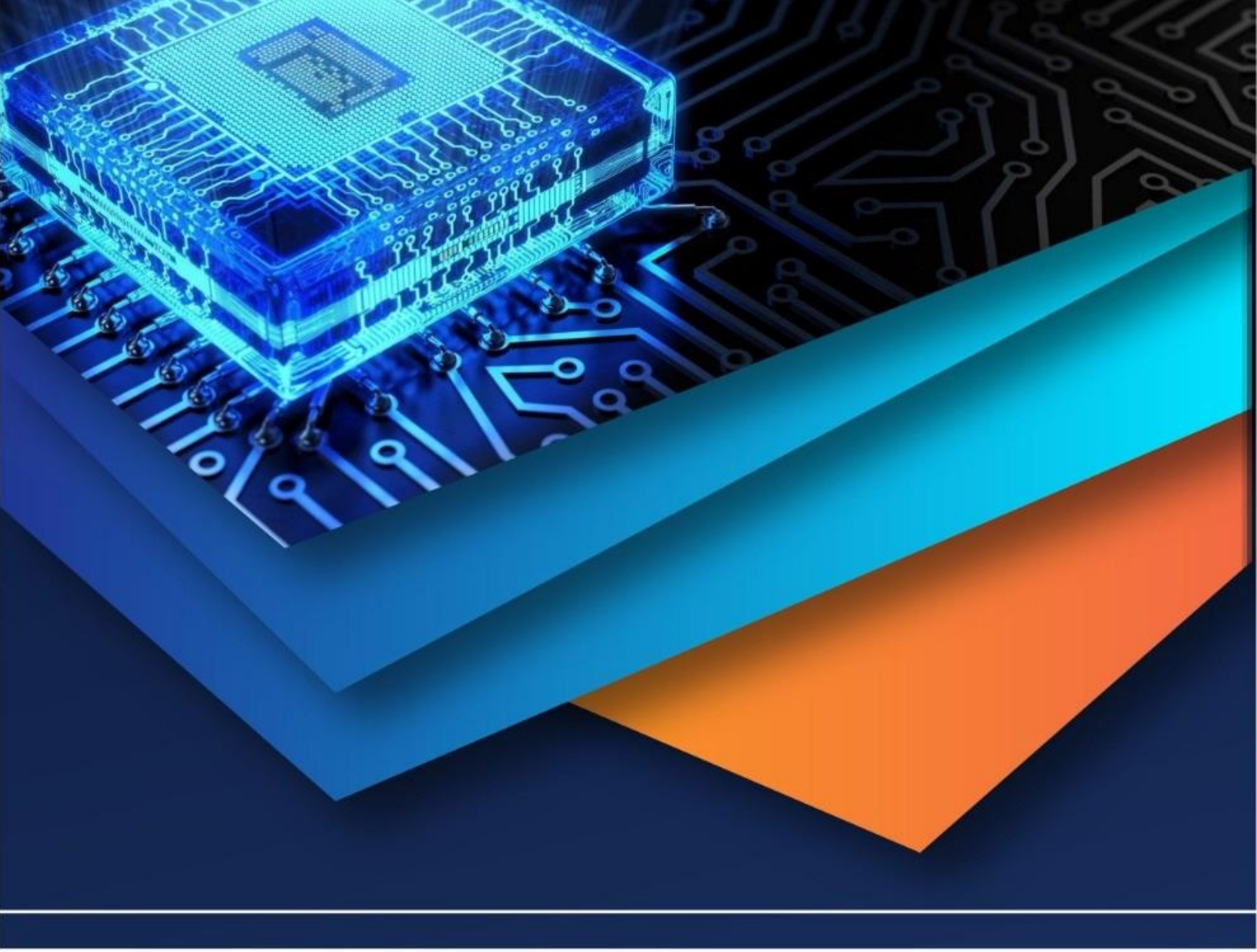
V. CONCLUSION

The designing architecture of UART is supported 8-bit data word length at 9600 bps baud rate for serial transmission of data with the addition of status register for detecting errors in data transfer and BIST which as allows to test the circuit itself, is proposed. Working of UART is tested using Xilinx ISE simulator, which is implemented on vertex FPGA. With error checking status register, i can detect the different types of errors occurred during communication. With the implementation of BIST, expensive tester requirement , testing procedures starting from circuit or logic level to field level testing are minimized. The LFSR replaces the function of the external tester features such as a test pattern generator by automatically generating pseudo random generator patterns to give good fault coverage to the UART module. Although the additional BIST circuit increases the hardware overhead and design time and complexity, it eliminates the need to acquire high-end testers. The reduction of the test cost helps in the reduction of overall production cost.

REFERENCES

[1] Nennie Farina Mahat,memberieee “Design of 9-bitUART module” IEEE-ICSE2012 Proc., 2012, KualaLumpur, Malaysia
[2] J. Norhuzaimin, and H.H. Maimun, “The design ofhigh speed UART,” Asia Pac. Conf. on Appl.Electromagnetics (APACE 2005), Johor, Malaysia,Dec. 200
[3] DoughlasA.pucknell and K.Eshraghian ,Basic VLSIdesign, PHI
[4] Nazeih M Botors, HDL Programming VHDL andVerilog, Dreamtech Press, 2009
[5] Design for testability and BIST , Jin-fu LI, ARES lab
[6] Principles of CMOS VLSI design , by NeilH.E.weste and Kamran Eshragian
[7] Mohd Yamani IdnaIdris, MashkuriYaacob,ZaidiRazak, “A VHDL implementation of UART designwith BIST capability” Malaysian Journal of Computer Science, Vol. 19 (1), 2006.
[8] www.asic.co.in/BIST2- Design for testability
[9] Bibin M C, Premananda BS, “Implementation ofUART with BIST technique in fpga” InternationalJournal of Inventive Engineering and Sciences(IJIES) , Volume-1, Issue-8, July 2013
[10] Peter J Ashenden, Digital Design – AnEmbedded Systems Approach using Verilog.

©IJRASET: All Rights are Reserved



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Call : 08813907089 (24*7 Support on Whatsapp)