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Novel Multilevel Inverter Topologies for Cascaded Voltage Source Architectures

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***Abstract:** this paper proposes two new single phase multi level inverter (mli) topologies configured with reduced switches suitable for cascaded structure on extracting various levels of ac output voltages. The philosophy essays a proportion between the input dc voltage and the preferred number of output voltage levels. The scheme explores incorporation of h- bridge together with a structure to alleviate switching losses for the specific target output voltage. The proposal allows the magnitudes of the voltage sources to be arranged in binary or trinary fashion and there it maximizes the number of output voltage levels of the mlis. It also introduces the multi carrier pulse width modulation technique along with phase disposition sequence (pd-mc-pwm) and a hybrid pwm (hpwm) formulation for generating the firing pulses. The outputs of the proposed cascaded hybrid mli topologies validate the simulated results based on matlab r2010 and entice a fresh scope for the use of mlis.*
***Keyword:** asymmetric mli, field programmable gate array, hybrid topology, multilevel inverter*

I. INTRODUCTION

Multilevel inverters (MLIs) continue to extend the performance credentials to use as power converter interface and support for high power quality demanding applications. MLIs enjoy savvy to incarnate possible turn around and foster structural modifications to leave way for an enhancement in the utility value. The MLIs can be composed in an array of power switches and capacitive voltage sources coiled through the switching devices to serve and translate the dc voltage into a multiple-stepped ac voltage waveform with variable amplitude and frequency [1-3]. The MLIs are destined with lower voltage distortion, common-mode voltage ratio, reduced dv/dt and even abolish the output filters.

A cascaded H-Bridge MLI [4] fed from equal dc voltage sources have been supplied by modified asymmetry dc voltage sources [5-8]. The asymmetric or hybrid cascaded half bridge multilevel inverter (CHBMLI) could generate considerably more output voltage levels than other symmetrical topologies that are using less semiconductor switches and capacitors [9]. A multilevel dc-link inverter topology has been perceived by generating a rectified sine wave and allowing it to pass through a single H- bridge inverter to alternate the polarity thereby producing a perfect sinusoidal voltage [10]. The configuration has been modified to reduce the switch count and to increase the number of output levels as compared to traditionalstructures [9].Emerging other topologies has also been amended with five-level inverters to replace the H-bridge in a cascaded topology and to reduce the number of dc sources. The H-bridge has been attached with different dc voltages in an asymmetric multilevel cascaded two-terminal sub-modules without separate dc sources to form a modular structure [5] and switching the dc sources in series/parallel or forming a cell to build a hybrid cascaded multilevel inverter [6, 11, 12].

hough innumerable ways exist to combine power switches, dc sources and capacitive dividers to generate multilevel output voltages using cascaded clamped diodes with flying capacitor MLI topologies, still they survive a relevance to examine futuristic alternatives and come up with dedicated forms to suit specific needs [4, 13-18].In [21] n-phase multilevel space vector PWM technique have been adopted in theVSI, and the control problem have been solved by the use of Eigen space decomposition of the system matrix. It has used fewest space vectors and minimum total conduction time. Switching losses are more because of the two level multiphase operations. The authors [22] used PWM strategy to achieve balanced line-to-line output voltage in the linear modulation range where the multilevel cascaded inverter output voltage can be linearly adjusted. In [23] GA algorithm has been used to optimize switching angles for multilevel inverters with many DC sources and minimizing several harmonics. Due to optimized switching angle the losses were also minimized. In [24] the converter inherently operated over a wide range of voltage conversion ratios and over a wide average power ranges. A small loss is developed and it has been compensated by the efficiency. In this paper [25] a new technique has been proposed with conventional cascaded H-bridge inverter. The switches and driver circuits used were yielded low initial cost and power losses. In [26] dual bridge multilevel inverter was used with a single DC voltage source. A floating capacitor voltage is regulated using redundant switching states at half of the main DC-link voltage. The efficiency in this inverter is

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better than the 3level NPC inverter and lesser than the dual inverter. The losses are more in floating inverter because of the dual converter operation and two switching process. It is lesser in multilevel inverter topology and also the initial cost is high in dual converter. The authors in [27] used E-type module for asymmetrical multilevel inverter with reduced components to produce 13 levels of output. This method had used less number of switches and DC sources with low switching frequency. Selective harmonics were eliminated to improve the quality of the output. This paper has been organized with five sections of 1.Introduction, 2.Problem statement, 3.Proposed topologies, 4. Simulation results and 5 conclusions.

II. PROBLEM FORMULATION

A. Problem Statement

The main effort endeavors to achieve minimum use of power switches and hence reducing the stress on the switches and thereby createtwo newtopologies for single phase MLIs that are powered using dc voltage sources. In the proposed work the first attempt owes to effectively arrange the input power sources and the second corners to an extension of the cascaded cell topology in which the H- bridge inverter forms the central part and encircles voltage sources arranged in the required pattern. The methodology tailors, to alter the smart use of PWM patterns to return an improved power quality output voltage with higher number of output voltage levels and lower the switching loss.

B. Proposed Topologies

1) Proposed Architecture: The circuit diagram of the proposed cascaded topology cell composed by series connected dc sources $\left((V_{1,1}, \ldots\ldots, V_{n_1,1}) \ldots\ldots\ldots (V_{1,k}, \ldots\ldots, V_{n_k,k}) \right)$ and H- bridge inverter is shown in figure 1. The bidirectional power devices $\left((S_{2,1}, \ldots\ldots\ldots, S_{(2n_1-2),1}) \ldots\ldots\ldots (S_{1,k}, \ldots\ldots, S_{(2n_k-2),1}) \right)$ are used to clamp the voltage sources to the load side and prevent the voltage sources from inter-looping problems. The proposed MLI consists of three permanent structures; one is the two voltage sources $(V_{1,1}, V_{n_1,1}) \ldots (V_{1,k}, V_{n_k,k})$ along with their supported power devices $(S_{1,1}, D_{1,1}), (S_{(2n_1-1),1}, D_{2,n_1})$ and $(S_{1,k}, D_{1,k}), (S_{(2n_k-1),1}, D_{2,n_k})$ forms the first part and the other one is the H- bridge inverter introduced for the polarity reversal leads the second part. Using this permanent structure alone, the proposed inverter requires switch count two less than that of cascaded H- bridge inverter for same number of voltage levels.Figure 2 to 4 depict the operating modes of the proposed cascaded cell MLI topology using one basic cell with three isolated dc sources. The basic module using dotted lines in the first cell of the dc-link part shown in Fig. 1 are connected in series to produce possible values of output voltage (V_0). Also in Figure 1 'k' basic cell units are in series. From which the structure of first unit, second unit… and k th units have n_1, n_2,…,$n_k$isolated dc sources respectively. In this case the number of output voltage level and switches are given by $m = \prod_{i=1}^{k} (2n_i + 1)$ and $N_{switch} = (\sum_{i=1}^{k} (2n_i - 1)) + 4$ respectively.

It is noticed from Figure.2 that the devices $S_{1,1}$, $S_{2,1}$ and $S_{3,1}$ or the pairs S_1& S_2 or S_3& S_4 in the H-bridge are conducting alternately to extract the first level of output voltage further the topology goes on through a similar sequence of operation for other levels also. The efficiency of the inverter is predicted by the number of switches in the current conduction path.As is evident from Figure.2 and 3, the proposed symmetrical MLI utilizes only two switching devices in the first part except for level 1. Due to this inherent first advantage, the proposed inverter has less switching losses compared to its counterparts [9, 8, 11, 12 and 21-27] and hence it has a better efficiency. The second advantage is that only half of the carrier signals are required to generate gating pulses for the power devices.

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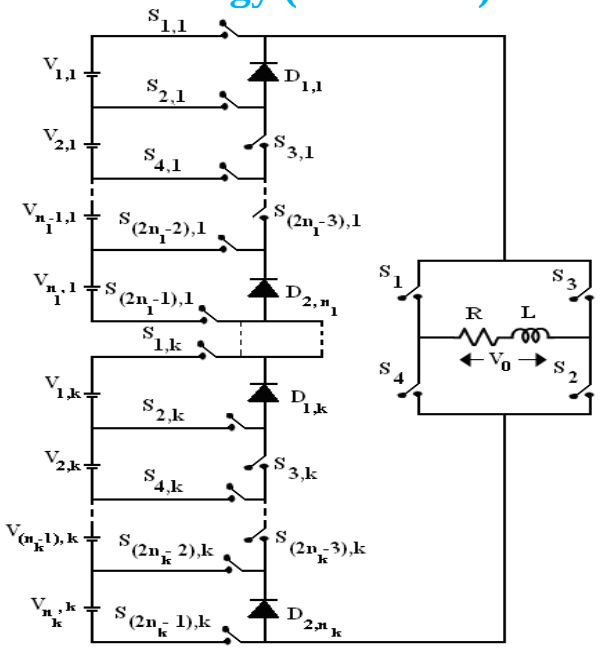

Figure.1. Proposed topology

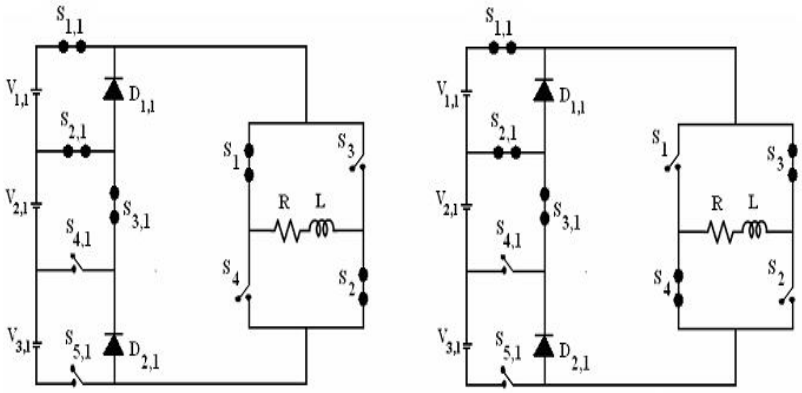

Figure.2.operating mode for level 1 **(a)** $+V_{1,1}$**(b)** $-V_{1,1}$

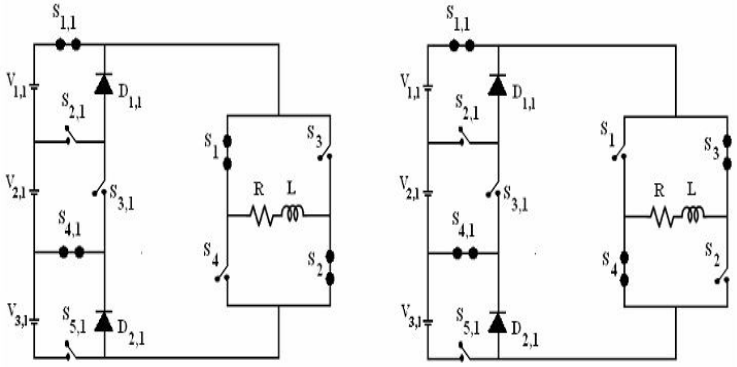

Figure.3.Operating mode for level 2 (a)+ ($V_{1,1}$ +$V_{2,1}$) (b) - ($V_{1,1}$ +$V_{2,1}$)

This topology utilizes isolated dc sources and it is free from voltage balancing problems. Table 1 shows the comparison of power components between the proposed and basic topologies. For generation of 7 levels, the proposed inverter requires only 9 devices, whereas the cascaded MLI requires 12 devices. Table 2 shows comparison in terms of devices in the conduction path of

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multilevel dc-link (MLDCL) inverter and the proposed topology and its counterparts. It is evident

Table.1.Comparison between topologies for 'm' level

MLI Structure / Components	Cascaded H-bridge	Diode clamped	Flying Capacitor	Multilevel dc-link inverter			Series parallel switched MLDCLI (ref. 18)	DBMLDLI (ref. 19)	Proposed topology considering one cell
				Cascaded half bridge	Diode clamped	Flying capacitor			
Main switches	2(m-1)	2(m-1)	2(m-1)	(m-1)+4	(m-1)+4	(m-1)+4	(3m-1)/2	(m+13)/2	(m+2)
Bypass diodes	-	-	-	-	-	-	1	(m-3)/2	2
Clamping diodes	-	2(m-3)	-	-	(m-3)	-	-	-	-
DCsplit capacitors	-	(m-1)/2	(m-1)/2	-	(m-1)/2	(m-1)/2	-	-	-
Clamping capacitors	-	-	(2m-6)/2	-	-	(2m-6)/4	-	-	-
DC sources	(m-1)/2	1	1	(m-1)/2	1	1	(m-1)/2	(m-1)/2	(m-1)/2

Table.2.Comparison in terms of devices in the conduction path of MLDCL for seven levels

Voltage Level	Series parallel switched MLDCLI	DBMLDCLI	Proposed
$V_{1,1}$	4	2	3
$V_{1,1}+V_{2,1}$	3	3	2
$V_{1,1}+V_{2,1}+V_{3,1}$	2	4	2

from Table 2; the proposed topology requires lesser devices in the conduction path except for level ($V_{1,1}$) and decreases with increase in the level.

The algorithm proposes values of dc voltage sources for generating odd and even steps of output levels:

First stage

$$V_{j,1} = V_{dc} \qquad j=1, 2, 3\ldots n1 \qquad (1)$$

Second stage

$$V_{j,2} = V_{dc} + \sum_{i=1}^{n_i} n_i V_{dc} = (n_i + 1) V_{dc} \qquad j=1, 2, 3\ldots n2 \qquad (2)$$

m^{th}stage

$$V_{j,m} = V_{dc} + \sum_{i=1}^{m-1} \sum_{i=1}^{n_i} n_i V_{dc} \qquad j=1, 2, 3\ldots nm \qquad (3)$$

2)Modulation Method: The proposed symmetric topology requires (m-1) triangular carriers of the same amplitude and frequency and disposed horizontally in phase with each other, where, 'n' is the number of output voltage levels. The switching signals that buffer the power devices are obtained by direct comparison between triangular carriers (V_{cr1}, V_{cr2} and V_{cr3}) and the modulating reference sine wave (Msinωt) as indicated in Figure. 4. The output voltage amplitude can be varied by controlling the amplitude of the reference sine wave.

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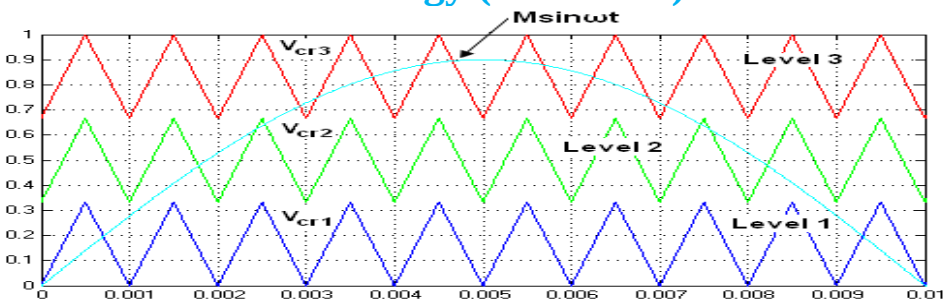

Figure.4.Pulse width modulation phase disposition technique (PD-PWM)

3) Proposed architecture in hybrid form

The hybrid architecture shown in Figure.5 is obtained by connecting H- bridge inverter with the proposed topology. Using this hybrid form, the dc voltage magnitudes are assumed either binary or trinary value to maximize the number of levels in the output voltage.

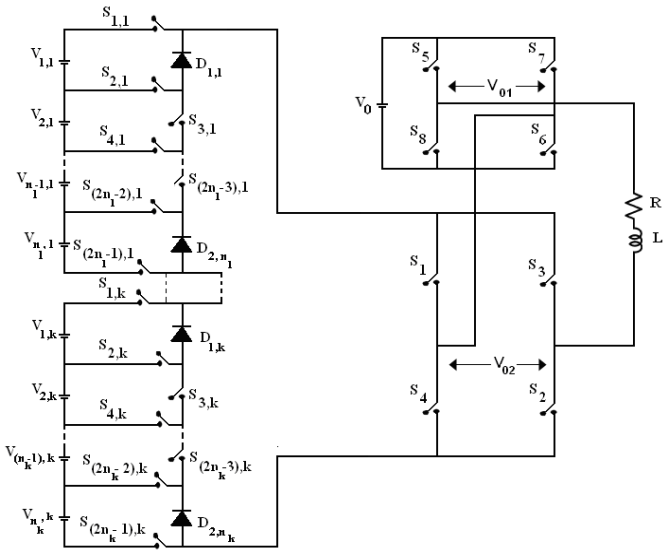

Figure.5.proposed topology in hybrid form

(a) The binary form results increased step output for the dc voltage sources arranged with a factor of 2 using the relation (4)

$$\frac{V_{1,1}}{V_0} = \frac{V_{2,'1}}{V_0} = \ldots\ldots = \frac{V_{n1,1}}{V_0} = \frac{V_{1,2}}{V_0} = \frac{V_{2,2}}{V_0} = \ldots\ldots = \frac{V_{n_k,k}}{V_0} = 2 \quad (4)$$

(b) Similarly the trinary form of equation (5) will result increased step output for the dc voltage sources arranged with a factor 3.

$$\frac{V_{1,1}}{V_0} = \frac{V_{2,'1}}{V_0} = \ldots\ldots = \frac{V_{n1,1}}{V_0} = \frac{V_{1,2}}{V_0} = \frac{V_{2,2}}{V_0} = \ldots\ldots = \frac{V_{n_k,k}}{V_0} = 3 \quad (5)$$

The increased step output voltage for the operation of equations (4) and (5) are summarized in Table 3. It is clear that for two or more DC sources (i.e. for n > 1),trinary arrangement results in most number of output levels as compared to other two arrangements.

Table.3.DC source arrangement and corresponding number of levels for one cell

SlNo.	Arrangement of DC sources	No of levels in the output voltage waveform
1	Unary	2n+1
2	Binary	4n-1
3	Trinity	6n-3

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4) Modulation Method: A hybrid modulation scheme [19] is applied to the proposed hybrid inverter because of the modular structure. Therefore, many switches are driven at low frequency even if PWM method is applied to the proposed inverter. The modulation scheme adopted for a fifteen level inverter has been discussed. Different reference and output waveform of the PWM generator and H- bridge inverter gating pulses for switches S_5 and S_7 and output voltage (V_{01}) across H- bridge inverter and output voltage (V_{02}) across the proposed inverter are shown in figure 6. The reference signal required for PWM operation is formed by intersecting the magnitude of minimum step voltage with the reference sine waveform. It can be seen that the pulse for the switch S_5 is obtained by comparing reference signal (W_r) with carrier wave (W_c) and pulse for switch S_7 is obtained by comparing reference signal ($-W_r$) with the same carrier as shown in Figures. 6(b) and (c). As a result, the output voltage (V_{01}) is obtained across the load terminals of H- bridge inverter as shown in Figure.6 (d).

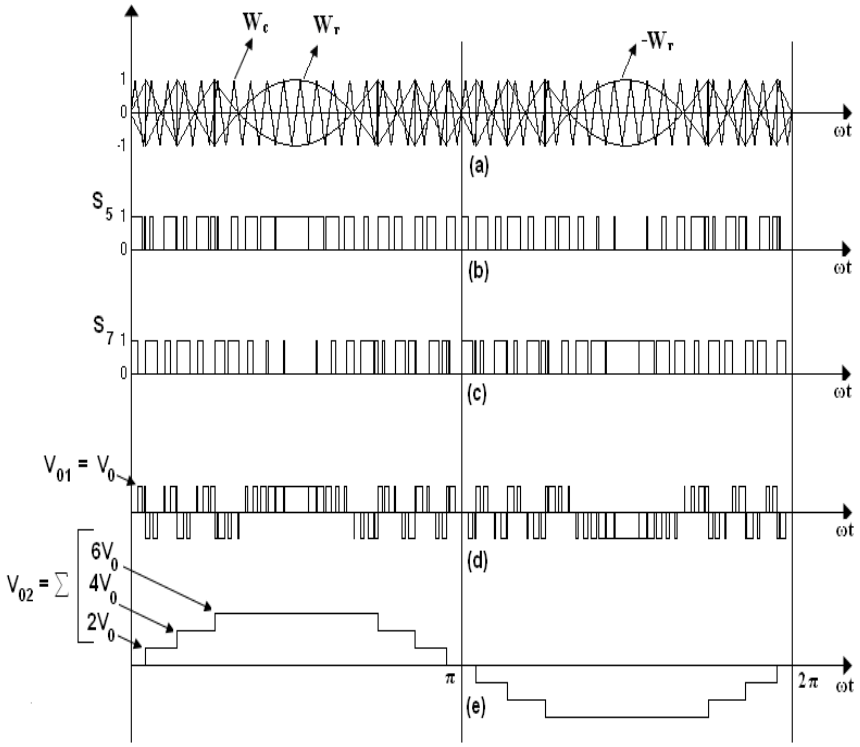

Figure.6. (a) Carrier and reference signal for PWM generator with fifteen level inverter. (b) Gating signal for S_5(c) Gating signalfor S_7(d) Output voltage waveform across H- bridge inverter **(e)** Output voltage waveform across the proposed inverter. Assuming the voltage magnitudes (V_1= V_2= V_3= $2V_0$) and the switches *(S_{a0}, $S_{b0,}$ S_{a1}, S_1, S_2), (S_{a0}, $S_{b1,}$ S_1, S_2) and (S_{a0}, $S_{b2,}$ S_1, S_2)* in the proposed inverter are switched on to obtain the output voltage (V_{02}) across the proposed inverter and it becomes $2V_0$, $4V_0$ and $6V_0$.

Similarly, when the switches *(S_{a0}, $S_{b0,}$ S_{a1}, S_3, S_4), (S_{a0}, $S_{b1,}$ S_3, S_4) and (S_{a0}, $S_{b2,}$ S_3, S_4)*are switched on, the output voltage (V_{02}) across the proposed inverter becomes $-2V_0$, $-4V_0$ and $-6V_0$. Therefore, the output voltage across the proposed inverter is as shown in Figure.6 (e). The hybrid architecture produces fifteen levels of output by adding V_{01} and V_{02}. The proposed inverter requires only 13 devices to generate 15 levels of output whereas the cascaded MLI requires 16 devices.

III. SIMULATION RESULTS

A. Simulation results for the proposed architecture

The proposed symmetric seven levelstructures have been simulated in MATLAB/Simulink platform using insulated gate bipolar transistors (IGBT). The voltage, frequency and other parameters considered under simulation are $V_{1,1}$= $V_{2,1}$= $V_{3,1}$= 100V, f_s= 2 KHz, R=150Ω and L=100mH. A phase disposition multi carrier pulse width modulation (PD-MC-PWM) technique [20] is used for testing the proposed inverter. The load voltage waveform and its respective harmonic spectrum and current waveform for inductive load are shown in Figure.7 and 8 respectively.

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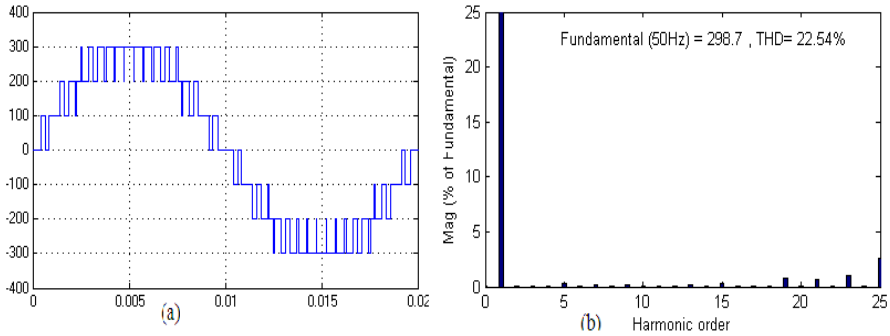

Figure.7.(a) Output voltage waveform (b) Voltage spectrum

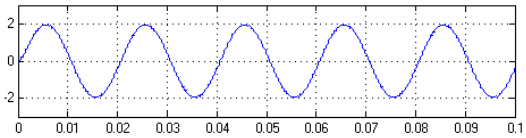

Figure.8.Inductive load current waveform

B. Simulation results for the proposed hybrid architecture

The proposed hybrid 15 level inverter has been simulated with the devices, switching frequency and loading values as in practical case of symmetrical structure and the magnitudes of voltage sources are chosen as V_o= 40V, $V_{1,1}$= $V_{2,1}$= $V_{3,1}$= 80V.A modulation method described in [20] is used for testing. The output voltage waveform along with harmonic spectrum and inductive current waveform are shown in Figures.9 and 10 respectively. The outputs are better than the CHB multilevel inverter and the inverters presented in [11, 12]. From the figure it is visible that the number of switches in the proposed topology is reduced except the topology presented in [12]**.** For instance, the switches used in seven level inverter and the number of switches used in CHB [11, 12] and in the proposed inverter are 12, 10 and 9 respectively. This reduces control system complexity and overall cost of system reliability.

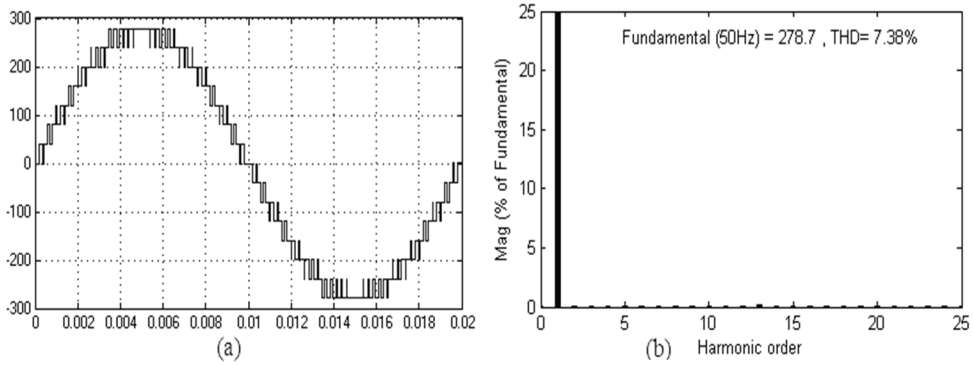

Figure.9**.**(a) Output voltage waveform (b) Voltage spectrum

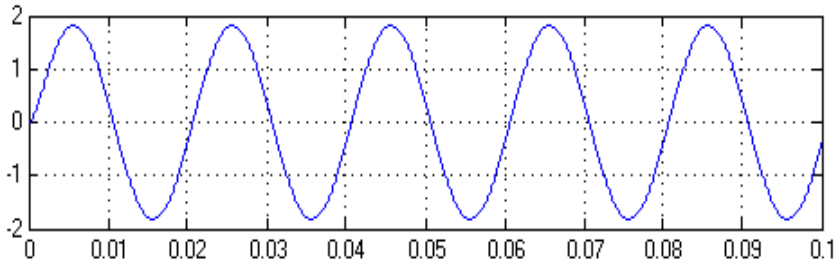

Figure.10.Inductive load current waveform

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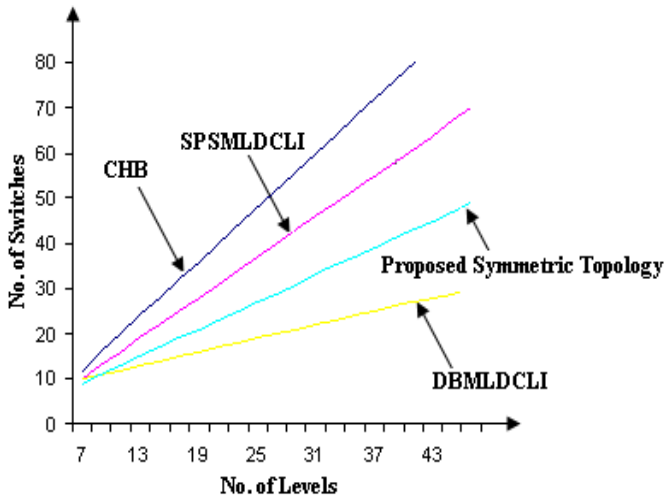

Figure.11Comparison of switches for different multilevel inverters

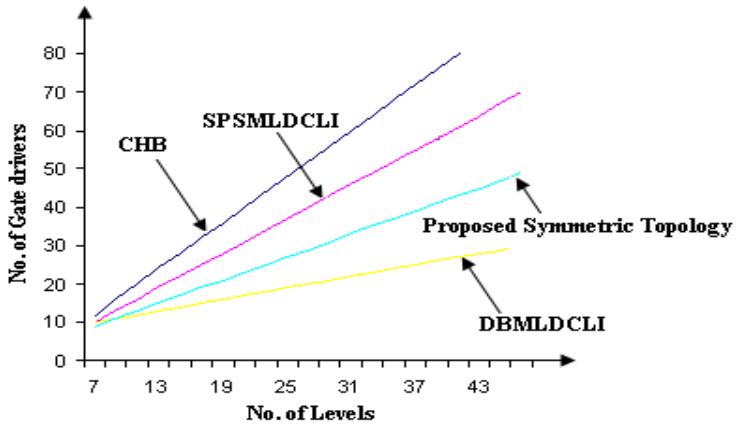

Figure.12Comparison of gate drivers for different multilevel inverters

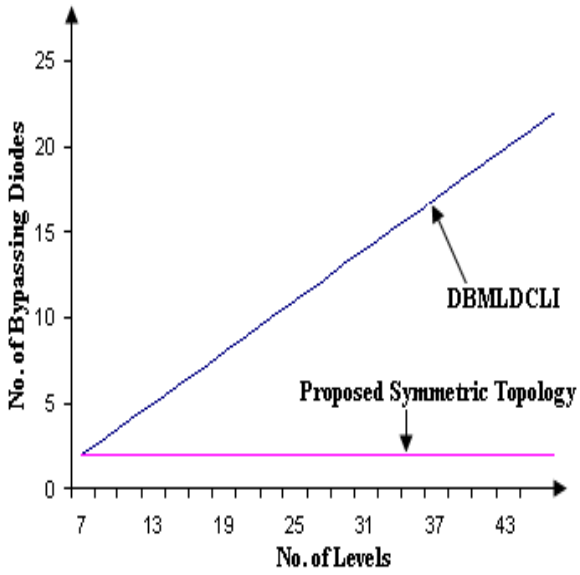

Figure.13Variation of bypassing diodes with number of levels for DBMLDCLI

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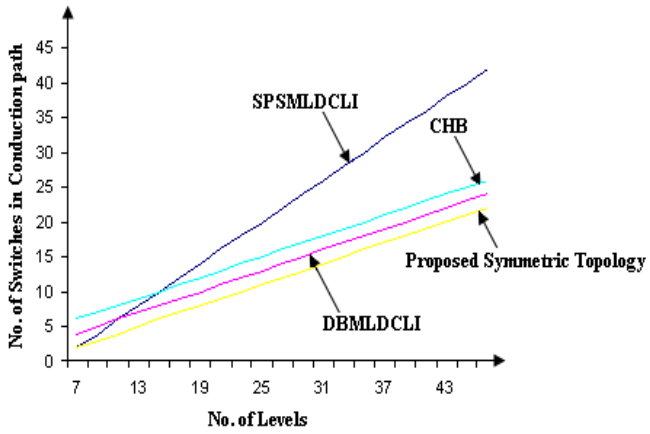

Figure.14No. of devices in conduction path in any instant of time with number of levels

Another case of issue on the comparison is the number of devices in the conduction path. Lower number of devices in current conduction path implies the lower voltage drop and lower conduction losses and hence better efficiency. In the proposed topology as shown in Figures.2, 4/2 switches are in conduction path instantly as a worst case. It is noticed that for some voltage level lesser devices are in conduction path of dc-link with two devices in H-bridge of the proposed inverter. So the switching losses as well as conduction losses and the total losses calculated are always lesser than the other topologies considered in this paper.

IV. CONCLUSION

The proposed asymmetrical topology MLIis having capability of generating all the voltage levels with less voltage stress and reduced conduction losses on minimum conduction devices in any conduction path of each level than the other topologies, similar to the hybrid MLI derived from symmetrical MLI which is suitable for high power applications with reduced standing voltages. From the above discussion in terms of number of switches in conduction path, bypassing diode and total number of switches and diodes the proposed new multilevel topology is having lowest initial cost than the other topologies. The proposed topology has the degree of freedom on choosing either PWM operation or fundamental switching mode depending on the requirement of variable speed and high voltage applications.

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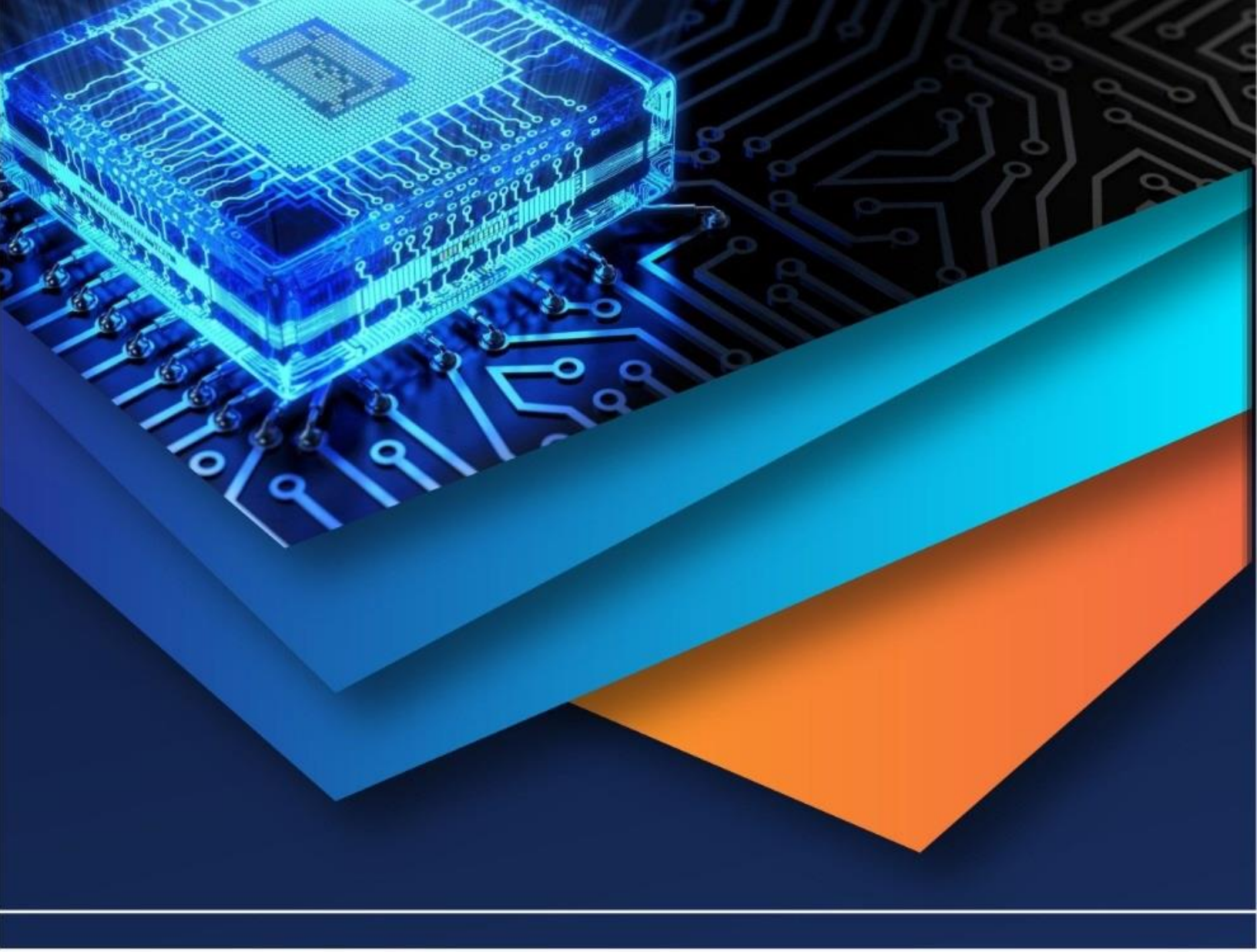

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