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Design of LC VCO With Current Mirror using 180 Nm Technology with Improved Power and Phase Noise

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Abstract: ***A new schematic design of LC-VCO for improving phase noise and lower power consumption. This design is carried out in the cadence software and schematic editor using 180 nm technology. Simulation is done and transient and frequency analysis are obtained. Results have been compared with the reference paper and improvements are obtained in this work.*** ***Keywords: VCO, LC-Tank, Low Phase Noise, Low Power Consumption, Spiral Inductor, pmos, nmos.***

I. INTRODUCTION

Today is increasing the digital technology so demand for wireless and multimedia applications also increase & keeps pushing the CMOS integrated wireless systems to support much communication standards (WLAN, GSM, UWB and DVB etc.). As gigahertz band communication is becoming more mature, the realization of a single chip transceiver becomes more demanding, with the need for reduced cost, reduced size and less power consumption. [1][2]

The oscillator power consumption can be a significant portion of the total power consumption of a system. So that's the overall picture power consumption can be reduced by minimizing the power consumption of the VCO. But there exist a several number of trade-offs among the important parameters like power, noise, frequency, gain in RFIC designs. FOM is a quantity to measure the performance of a device relative to its alternatives. Due to the trade-off between the power and phase noise for a particular frequency of oscillation a standard. [3]

II. CIRCUIT DESIGN AND IMPLEMENTATION

Though the cross-coupled CMOS LC-VCO's are widely used due to ease of implementation but the maximum noise generation in this circuit gives maximum phase noise so this configuration do not use complete potential of the LC tank circuit. In this balanced configuration, many different components are required to obtain a balanced circuit, so it consumes more current. Therefore, a new topology is introduced here, where both the cross-coupled and the balanced configurations gives a better VCO characteristics. Furthermore, a double cross-coupled circuit was built by combining these topologies which guarantee a rapid oscillations start up and a reduction in unnecessary components. This simultaneously helps to reduce the size of chip. It also has reduced noise up conversion properties. In many published papers, a complementary (CMOS) oscillator circuit is the result of combining both PMOS and NMOS cross-coupled pairs in parallel to generate negative resistance. In this proposed VCO (LC current mirror) design we appended up the current control architecture which is employed to decrease the system power consumption and phase noise. In this VCO design will employ two current mirrors circuit one at top and another at bottom, which balance the impedance in both the arm of the circuit and hence the current become the exact replica of the bias current. Because in the case of a single current mirror the impedance is unbalanced resulting in different currents in the mirror arms which will improve the power consumption and also has a negative effect on the phase noise performance of the circuit. In designing the LC-VCO we used the complimentary cross coupled circuit of NMOS and PMOS. In this topology we cascaded two stages in which the output of one stage is given to the input of another stage. This configuration does not latch up because its frequency gain is small. To decrease the large power dissipation. The complimentary cross coupled is used because first it offers higher trans-conductance to compensate for the loss of the tank circuit with less current consumption and hence is more efficient. The second matching PMOS and NMOS transistors that provide better symmetry properties of the oscillating waveform. In this design, current control mechanism reduces even harmonics in the drain current which as a direct impact on the noise component in the drain current which result reduction in phase noise. The proposed design schematic view of VCO. [4-5]

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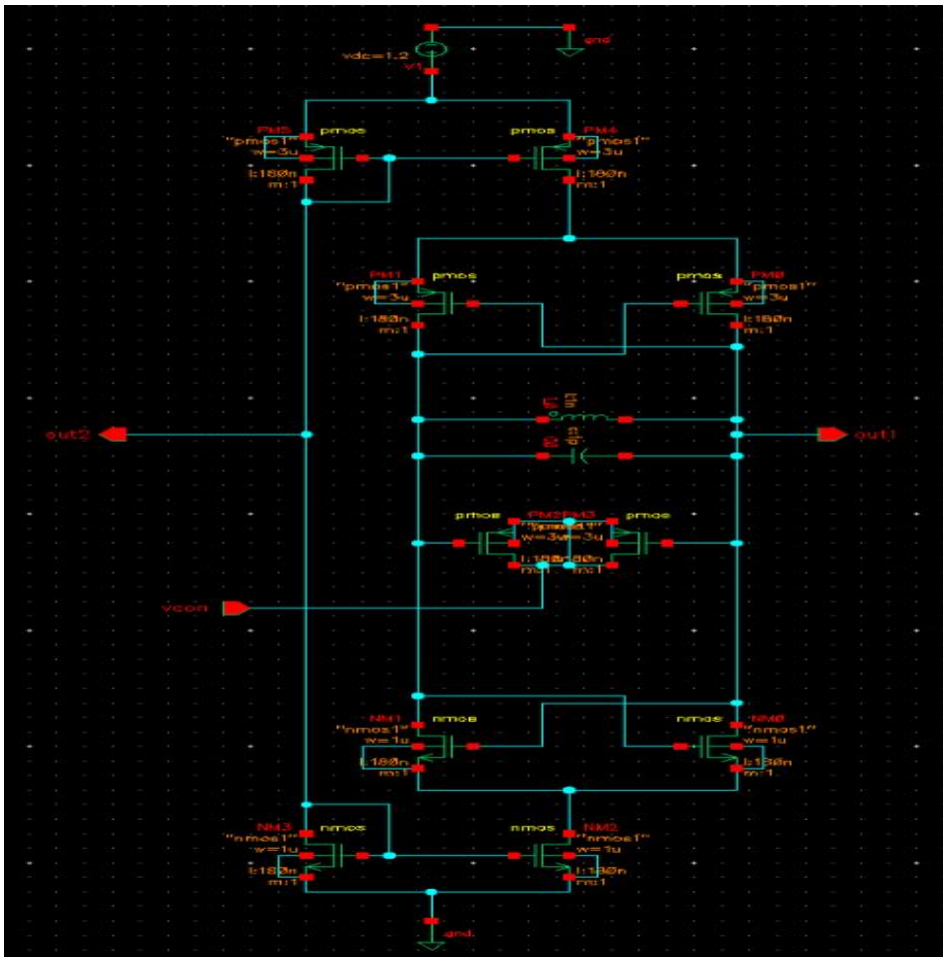


Fig. 2.1 Schematic Design of LC Current Mirror

III. ANALYSIS OF THE LC-VCO

In designing of (lc-vco) oscillator is to choose a circuit topology or type to reduce losses. Figure 3.1 is considered those losses which is associated with the inductor. In practical there would also be losses associated with the variable capacitors (varactors) and the metal oxide semiconductor field effect transistors (mosfets). It is the active devices. In experimental integrated vcos the inductors are on-chip spiral inductors with low quality factor that dominates the losses of the vco tank. This can be shown that the oscillation frequency of the circuit shown in fig. 3.1 [6]

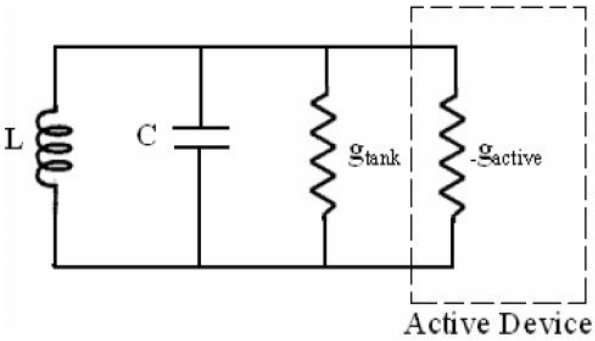


Fig. 3.1 Circuit Diagram of LC Tank

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LC-tank oscillator gives a good phase noise performance with low power consumptions. The phase noise performance of the LC oscillator depends upon the Quality factor of the on chip spiral inductor. The quality factor of the tank is given by:

$$Q = \frac{W_0 L}{R}$$

Where,
W_0 is the oscillation frequency [rad/s]
L is the value of the inductance [H]
R is inductor's equivalent series resistance
Q is the Quality Factor.
The resonance tank consists of a high Q inductor. Resonance frequency of the tank is expressed as:

$$F_{osc} = \frac{1}{2\pi\sqrt{LC}}$$

Where,
L is the inductor in Henry of LC tank and C is the capacitance.
Due to their relatively good phase noise, ease of implementation, and differential operation, cross-coupled inductance-capacitance (LC) oscillators plays an important role in high-frequency circuit design. Figure 3.2 has given a proposed design VCO in blocks form. [7-9]

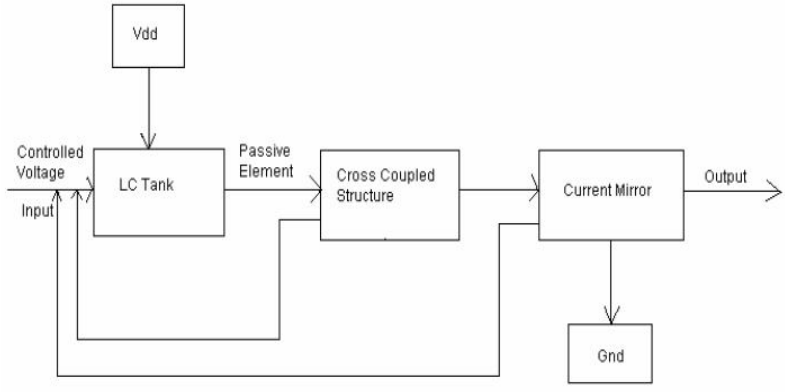


Fig. 3.2 VCO Design in block form

IV. SIMULATIONS & RESULTS

The result is obtained by using the cadence software in this we design schematic of (LC VCO) and do the transient analysis and calculate the phase noise and power consumption. In this design we have used 180 nm technology. The applied voltage is 1.2v at different centre frequencies. Simulation results are obtained with better improvement in phase noise and improvement in power consumption.

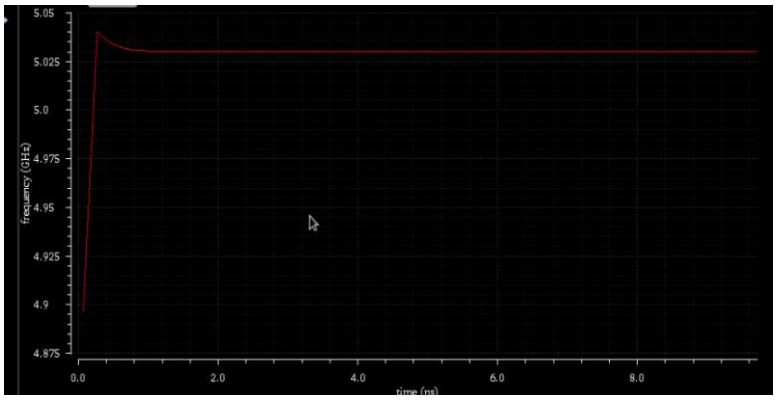


Fig. 4.1 Frequency response of LC current mirror

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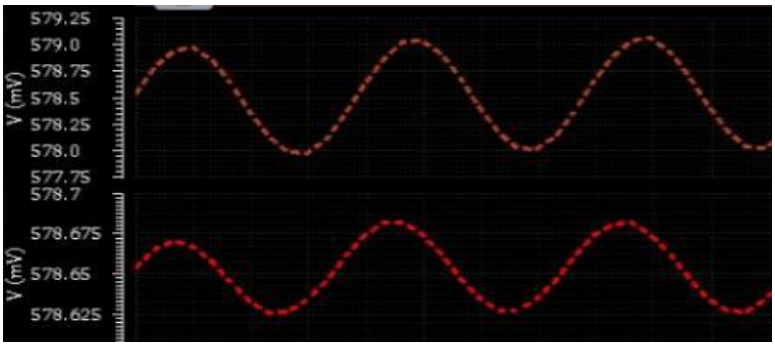


Fig. 4.2 Transient response of LC current mirror

TABLE 4.1

S.No.	*Parameter*	*LC VCO (without current mirror)*	*LC VCO (with current mirror)*
1	Operating Voltage	1.2 v	1.2 v
2	Technology (CMOS)	180nm	180nm
3	Power consumption	15.35mW	9.50mW
4	Operating Frequency	5.03GHz	5.03GHz
5	Phase Noise (dBc/Hz)	-125	-145.56
6	Phase margin	180	180

V. CONCLUSION

In this paper, we have presented a differential tuned LC VCO using 180 nm technology using cadence software at the operating of 5 .03GHz and the phase noise of -145.56. This VCO design is best for the applications where the low power consumption and low phase noise are the main requirements.

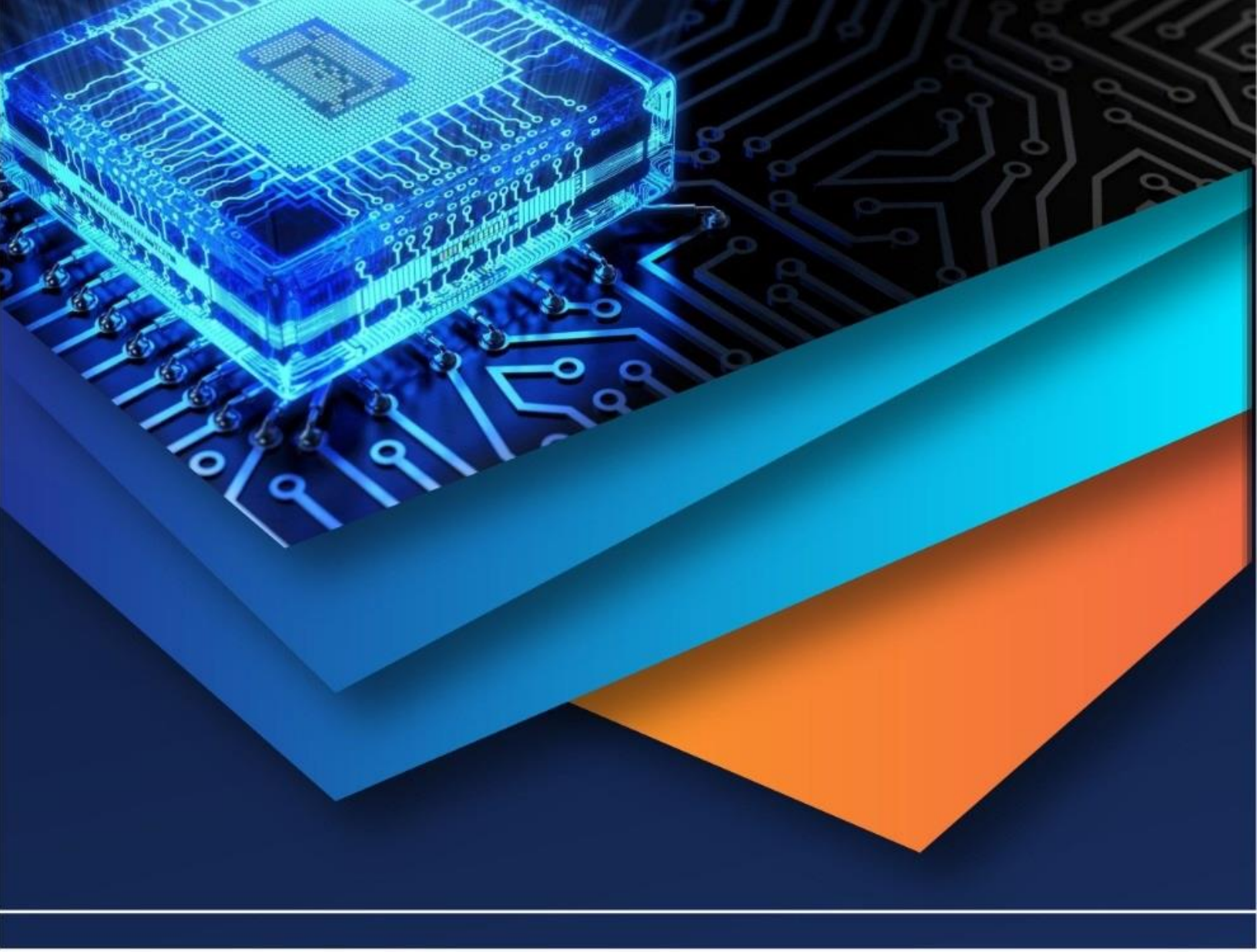
VI. ACKNOWLEDGEMENT

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