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Analysis of Low Leakage Architecture of SRAM 8x1 Using Leakage Power Reduction Technique in Different Technology

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Abstract: ***as the size of ic's is becoming small, day by day the demand of high density vlsi circuits has been increasing .the supply voltage reduction is necessary to reduce the active power. By lowering the supply voltage it is effective ways to suppress the energy consumption because reducing the supply voltage could reduce the dynamic power and leakage power respectively. In this paper, a technique called cluster technique has been proposed to reduce the active power requirement and the simulation has been done on 8x1 sram cell. In this work firstly the power dissipation of all the cells are connected to an without sleep is taken out then sleep transistor shared with two cells and after that all the four cells are connected to only sleep. Leakage reduction techniques for cmos based transistor level design and the techniques have been proposed like leakage lector technique transistor stack based low leakage approach, sleeper keeper technique for leakage reduction, multiple threshold transistor design technique, gated-clock based low power design etc. Various proposed techniques provide benefits with respect to specific design application. Therefore, result with cluster technique improved result than an individual sleep when connected to the sram cell. In this paper, sram cell without sleep transistor dissipates more power during different states as compared to sram cell with an individual transistor.asthe conventional design is simulated on different cmos fabrication technology using microwind tool.***

Keywords: vlsi circuits , nmos , pmos, cmos sram, 8x1 sram cell.

I. INTRODUCTION

As with every generation of technology, the demand of handling the large amount of data in embedded memory has been increasing. To fulfill the requirement handling large data feature size of transistor is continuously reducing. With respect to high transistor density the problem of power consumption is becoming prominent issue to tackle. Static Random Access Memory is the first choice of designing semiconductor embedded memories because of low power dissipation . The low power feature for on chip SRAMs is becoming more important especially for battery operated portable applications .It is however one of the most significant challenges of high density VLSI circuit .The main aim of this paper is to estimate the effect of clustering technique on 6T SRAM cell and to investigate transistor sizing of the 6T SRAM cell for optimum power and delay. In this work , an average power dissipation of 6T SRAM Cell has been compared with SRAM cell using cluster technique.The cluster technique reduces the power dissipation of 6T SRAM cell in read, write , and hold operation .

A. Conventional 6T SRAM Cell

It is shown in Fig 1. At deep sub-micron scale the leakage power of SRAM circuit is comparatively high as compared to the other operational circuits. The concept of SRAM architecture is based on the stabilization of logic values to maintain its existence against any current or power loss with the ease of data modification using two feedbacks coupled CMOS Inverters. The output terminals of the two inverters act as internal load lines of the SRAM cell to store the memory data bit value on one of the internal load line and its complement logic value on the other internal load line.

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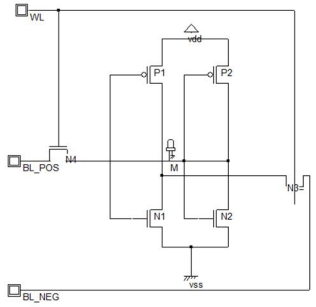


Fig .1 Basic 6-T SRAM

1) Write Operation- The logic data bit to be written in a SRAM cell is provided on the BL_pos and its complement logic value is provided on BL_neg. The WL input is provided a logic high pulse on NMOS data access transistors to enable the transfer of charge from the data lines (BL_pos and BL_neg) to the SRAM cell internal circuit. The duration of pulse should be more than the duration in which the charge on BL_pos and BL_neg should get shared by the SRAM internal load lines to store the desired logic value in the SRAM cell.

2) Read Operation- To read the data from the SRAM cell, logic high values are set on BL_pos and BL_neg. The WL input is provided a high pulse to enable the sharing of charge between the data lines, BL_pos and BL_neg, and the internal load lines. The data line (BL_pos or BL_neg) connected to the cell internal load line with logic value'1' will not show any change in the logic value after sharing of charge because of the same voltage on both the data lines. Whereas, the other data line will be affected by a small change in its voltage value after sharing the charge with the cell internal load line. Since the current driving capacity of the cell is very low, the change sharing will have a small voltage change effect when logic '0' at the internal load line is shared with the logic '1' of the data line. This voltage difference developed in the load lines is measured using the sense amplifier circuit to know the logic value that is stored in the cell.

B. SRAM Cell With Sleep Transistor

To see the effect of sleep transistor on 6T SRAM cell, NMOS sleep transistor is connected between the 6T SRAM cell and ground . During an active mode the NMOS sleep transistor is ON , which increases the speed of the circuit During Standby mode the sleep transistor is off which reduces the leakage current .In this circuit , the effect of W/L ratio on the sleep transistor is observed for the leakage current flowing through the sleep transistor is observed for the leakage current flowing through the sleep transistor is active and standby mode.

It can be seen that the current flowing through sleep transistor increases with respect to the width of the transistor in acyive and standby mode . Whereas , the voltage at drain node of the sleep transistors decrease while increasing the width of that transistor , which is responsible for more and less leakage current flowing through the transistor. As the width of the transistor increases the propagation delay of the SRAM cell increases .

C. 8x1 Cell Without Sleep Transistor

It describes the designing of 8x1 SRAM cell arrays of 1 row and 16 columns . Each block of the array of 6T SRAM cell. There is 1 row and 8 coloumns that are arranged to form a 8x1 SRAM cell Array . There is only one row ,so there is no need of decoder . All the 8 cells are connected to the same word line. As the row consists of 8 cells , it consitutes to form two byte. The data is written into the cell through multiplexers which are connected to the bit lines. To read the data stored on storing nodes out 1 and out 2, sense amplifiers are connected which read the stored values of the SRAM cell. The 8x1 SRAM without any sleep transistor shows the highest power dissipation during all the states(read, write, and hold states)

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II. PROPOSED WORK

In this proposed work , the clustering technique, has been used. In this technique 6T SRAM cell with sleep transistor is used . As there are 8 cells in 8X1 cells array , each cell has got its individual sleep transistor,two or all cells can be connected to the same sleep transistor . This effects the average power dissipation of the memory cell during different modes of operation such as read, write and hold states.

A. Cluster Technique

1) 8x1 cell with common sleep transistor: The 8x1 cells array with two cells having a common sleep transistor. In between eight cells there are eight sleep transistors .The 8x1 cells array where all the eight cells are sharing a single sleep transistors . As in this type of clustering , all the cells are connnected with a common sleep , the number of transistor are reducing as well as it reduces the power dissipation during read ,write and hold state of the memory cell as compared to the cells without sleep and cells with individual sleep.Comparison of all techniques has been carried out in table.

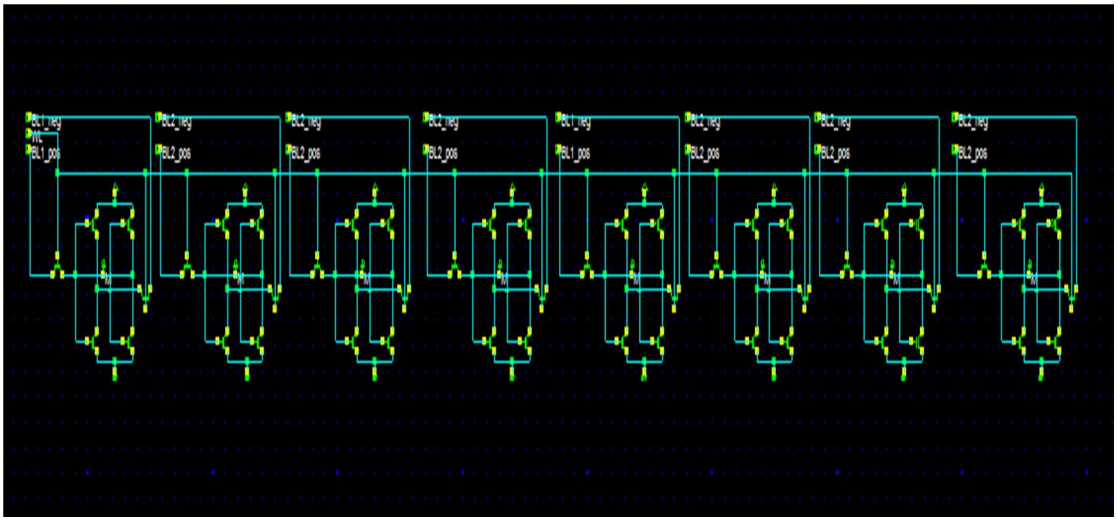


Fig.2. 8x1 cell without sleep transistor

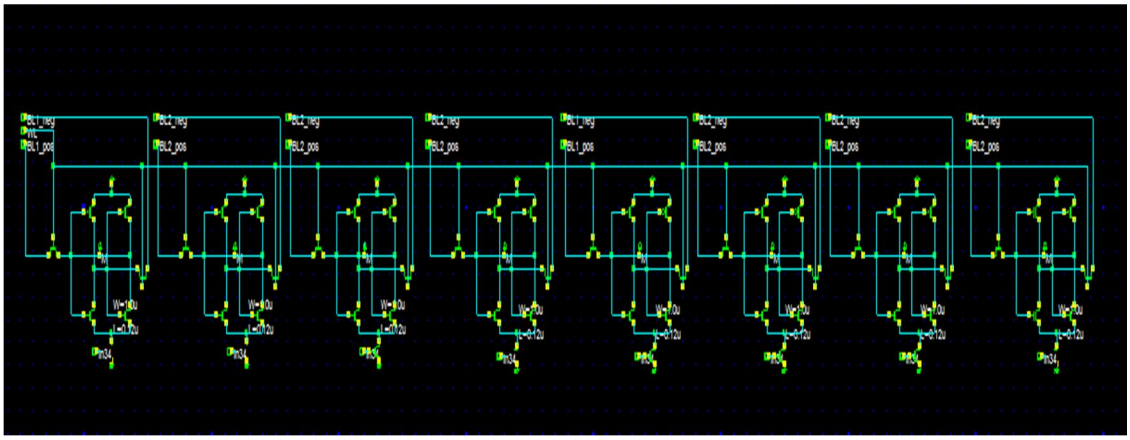


Fig.3. 8x1 cell with sleep transistor

III . SIMULATION RESULTS

We have estimated the impact of clustering technique on average power dissipation of 4X1 SRAM cell. The circuit is characterized by using the 180nm technology with the supply voltage. All the simulations done on Microwind tool. The comparison of power dissipation for different combination of cluster technique is shown in table. It can be easily seen that SRAM cell without sleep transistor dissipates more power during different states as compared to SRAM cell with individual sleep transistor .

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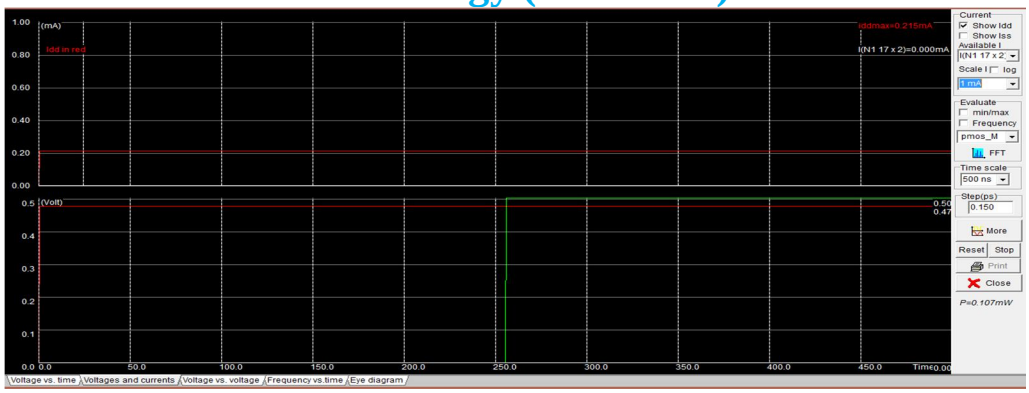


Fig.4 Voltage and current analysis of 8x1 SRAM Cell without sleep transistor

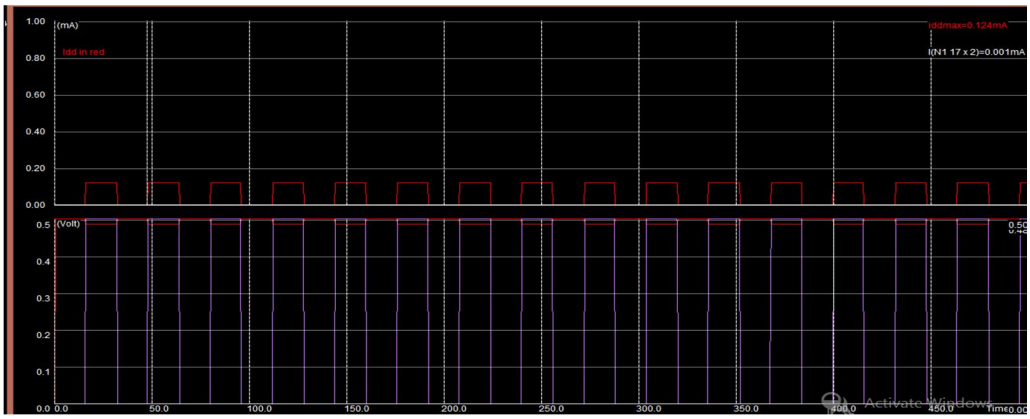


Fig.5 Voltage and current analysis of 8x1 SRAM Cell with sleep transistor

TABLE FOR COMAPARISON

Technology	Power Consumption		% Decrease in Power
	Conventional design	Cluster Technique	
50nm	0.107 mW	2nW	
90nm	0.86 mW	1.92mW	
120nm	1.26mW	3.108mW	
180nm	3.12mW	7.314mW	

IV. CONCLUSION

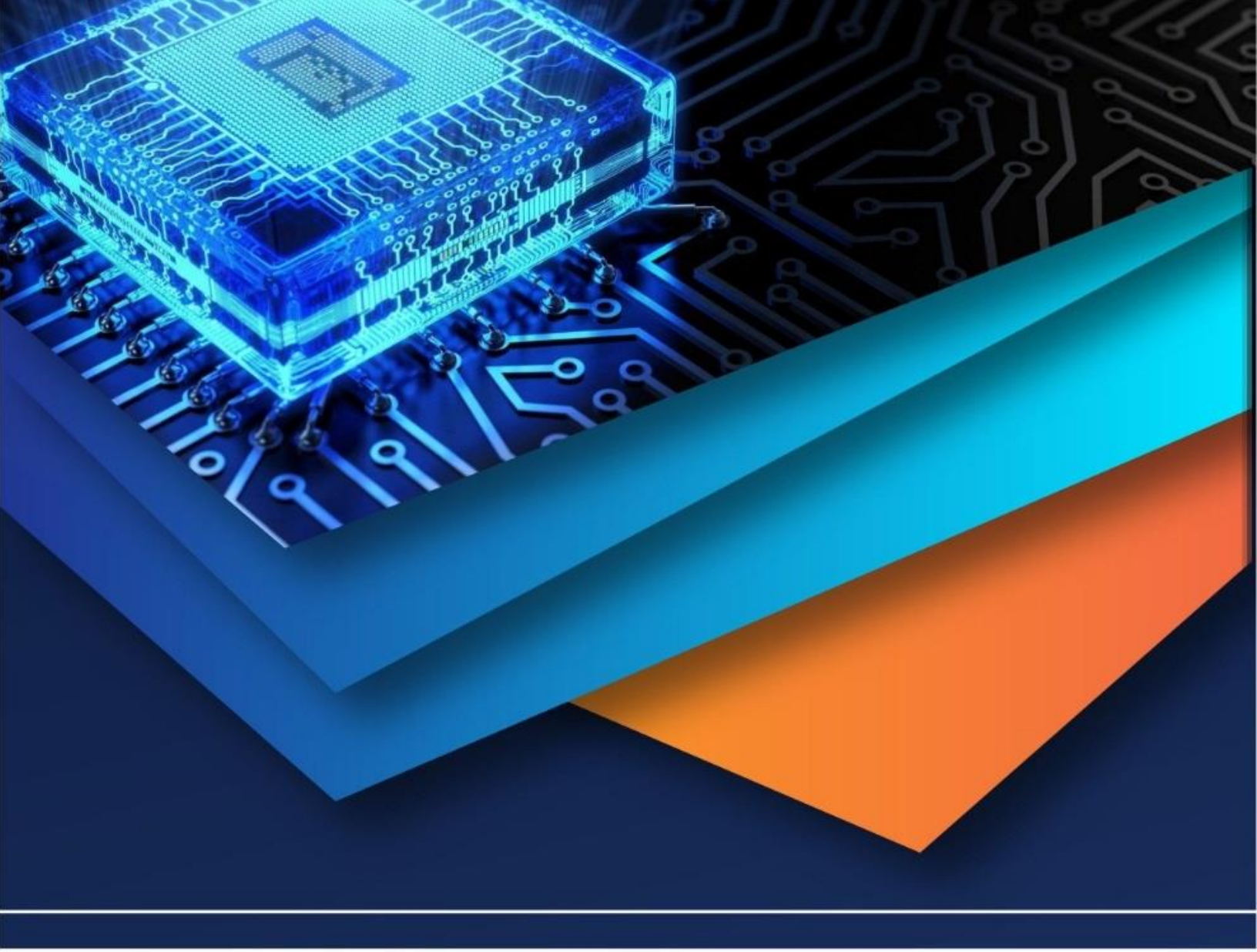
This paper overall reveals that the SRAM cell with sleep transistor dissipates less power as compared to the cell without sleep transistor .The average power dissipation can be further reduced by applying clustering ,in which rather connecting sleep transistor to each cell separately. Then it can be shared by two cells and 4 cells in 16x1 SRAM cell. The reults shown in table with different technology.

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