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Pre-Encoded Multipliers Based on Non-Redundant Radix-4 Signed-Digit Encoding

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Abstract: We present architecture of pre-encoded multipliers for Digital Signal Processing applications based on off-line encoding of coefficients.

The Non-Redundant radix-4 Signed-Digit (NR4SD) encoding technique employs the digit values{-1,0,+1,+2}or{-2,-1,0,+1} .It is effective in designing a multiplier with less complex partial products implementation. Extensive experimental analysis proves that the proposed pre-encoded NR4SD multipliers, including the coefficients memory, are more area and power efficient than the conventional Modified Booth scheme.

Keywords: modified booth scheme, Non redundunt radix-4 signed digit encoding (NR4SD), partial products, encoding.

I. INTRODUCTION

In today's modern wireless communication systems the received signal strength greatly varies. Digital multiplication is mostly included in all of today's DSP processors as it is very common operation and frequently occurring function in all algorithms.

Fig. 1 shows The proposed NR4SD encoding scheme uses one of the following sets of digit values: {-1,0,+1,+2}or{-2,-1,0,+1}. In order to cover the dynamic range of the 2's complement form, all digits of the proposed representation are encoded according to NR4SD except the most significant one that is MB encoded. Using the proposed encoding formula, we pre-encode the standard coefficients and store them into a ROM in a condensed form (i.e., 2 bits per digit). Compared to the pre-encoded MB multiplier in which the encoded coefficients need 3 bits per digit, the proposed NR4SD scheme reduces the memory size. Also, compared to the MB form, which uses five digit values {-1,0,+1,+2}or{-2,-1,0,+1}, the proposed NR4SD encoding uses four digit values.

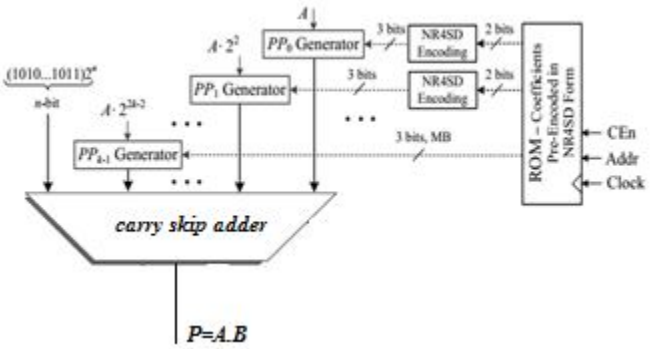

Fig. 1. A System Architecture of the NR4SD Multipliers.

Thus, the NR4SD-based pre-encoded multipliers include a less complex partial products generation circuit. We explore the efficiency of the aforementioned pre-encoded multipliers taking into account the size of the coefficients'ROM.

II. LITERATURE REVIEW

We have studied various papers to "pre encoded multipliers". In "Rom-based logic (rbl)design: A low-power 16 bit multiplier," by B. Paul, S. Fujita, published in IEEE J. Solid-State Circuits, vol. 44, no. 11, pp. 2935–2942, Nov.2009[1] says that The design uses sixteen 4 times 4 ROM-based multiplier blocks followed by carry-save adders and a final carry-select adder (all ROM-based) to obtain the 32 bit output.

In "High-performance fir filter design based on sharing multiplication," by J. Park, K. Muhammad published in IEEE Transaction Very Large Scale Integr. (VLSI) Syst., vol. 11, no. 2, pp. 244–253, Apr.2003[2] says that main idea is to represent the multiplication in FIR filtering operation as a combination of add and shift operations over the common computation results. The

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common computations are identified by decomposing the coefficients of FIR filters.

III. DESIGN OF PRE-ENCODED MULTIPLIER

In the proposed system we reduce delay by involving efficient NR4SD algorithms along with carry skip adder technique.

A. Non-redundant radix-4 signed digit algorithm

In this section, we propose pre encoded multiplier algorithms.As in modified booth, the partial products are reduced to half. When encoding the 2's complement number *B*, digits $b^{NR^-}_j$ take one of four values: $\{-2, -1, 0, +1\}$ or $\mathbf{b}^{NR+}{}_j \in \{-1, 0, +1, +2\}$ at the NR4SD− or NR4SD+ algorithm, respectively. Only four different values are used and not five as in MB algorithm, which leads to $0 \le j \le k-2$. As we need to cover the dynamic range of the 2's complement form, the most significant digit is MB encoded (i.e., $b^{MB}{}_{k-1} \in \{-2,-1, 0, +1, +2\}$). The NR4SD− and NR4SD+ encoding algorithms are illustrated in detail in Fig. 2and 3, respectively.

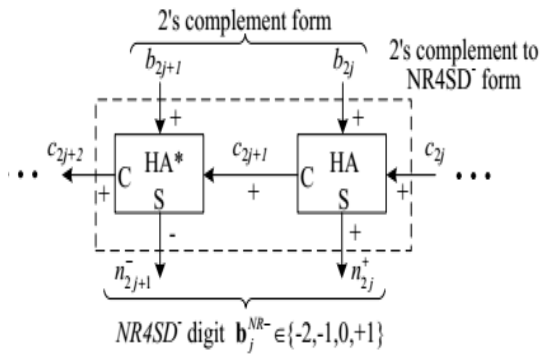

Fig. 2. Block Diagram of the NR4SD− Encoding Scheme at the Digit

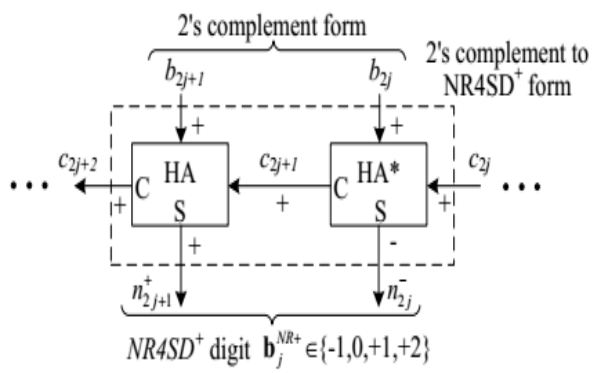

Fig. 3.Block Diagram of the NR4SD+ Encoding Scheme at the Digit

NR4SD− Algorithm

Step 1: Consider the initial values j = 0 and c0=0.

Step 2: Calculate the sum n+2j and carry c2j+1 of a Half Adder (HA) with inputs b2j and c2j Fig. 2. c2j+1 = b2j ∧ c2j, n+ 2j = b2j ⊕ c2j.

Step 3: Calculate the positively signed carry c2j+2 (+) and the negatively signed sum n− 2j+1 (-) of a Half Adder* (HA*) with inputs b2j+1 (+) and c2j+1 (+) (Fig. 3). The outputs c2j+2 and n− 2j+1 of the HA* relate to its inputs as follows: 2c2j+2 − n− 2j+1 = b2j+1 + c2j+1.

Step 4: Calculate the value of the $b^{NR^-}{}_j$ digit.

$$b^{NR-}{}_j = -2n-2j+1 + n+2j. \qquad (1)$$

Step 5: j: = j + 1.

Step 6: If (j < k−1), go to Step 2. If (j = k−1), encode the most significant digit through the MB algorithm and looking upon the three

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consecutive bits to be b_{2k-1}, b_{2k-2} and c_{2k-2} . If (j = k), stop. Table 1 shows how the NR4SD− digits are formed.

2's complement			NR4SD− form			Digit	NR4SD− Encoding		
b_{2j+1}	b_{2j}	c_{2j}	c_{2j+2}	n^-_{2j+1}	n^+_{2j}	$\mathbf{b}_j^{NR-}$	one^+_j	one^-_j	two^-_j
0	0	0	0	0	0	**0**	0	0	0
0	0	1	0	0	1	**+1**	1	0	0
0	1	0	0	0	1	**+1**	1	0	0
0	1	1	1	1	0	**-2**	0	0	1
1	0	0	1	1	0	**-2**	0	0	1
1	0	1	1	1	1	**-1**	0	1	0
1	1	0	1	1	1	**-1**	0	1	0
1	1	1	1	0	0	**0**	0	0	0

Table 1:NR4SD− Encoding

NR4SD+ Algorithm

Step 1: Consider the initial values j = 0 and c0=0.

Step 2: Calculate the carry positively signed c2j+1 (+) and the negatively signed sum n− 2j (-) of a HA* with inputs b2j (+) and c2j (+) (Fig. 3). The carry c2j+1 and the sum n−
2j of the HA* relate to its inputs as follows: 2c2j+1 − n− 2j = b2j + c2j.

The outputs of the HA* are analyzed at gate level in the following equations: c2j+1 = b2j ∨ c2j, n− 2j = b2j ⊕ c2j.

Step 3: Calculate the carry c2j+2 and the sum n+ 2j+1 of a HA with inputs b2j+1 and c2j+1.c2j+2 = b2j+1 ∧ c2j+1, n+ 2j+1 = b2j+1 ⊕ c2j+1.

Step 4: Calculate the value of the bNR j + digit. bNR+ j = 2n+ 2j+1 − n− 2j. (2)

Equation (2) results from the fact that n+ 2j+1 is positively signed and n− 2j is negatively signed.

Step 5: j := j + 1.

Step 6: If (j < k−1), go to Step 2. If (j = k−1),offline encode MSB digit and considering the three consecutive bits to be b2k−1, b2k−2 and c2k−2 . If (j = k), stop. Table 2 shows how the NR4SD+ digits are formed.

2's complement			NR4SD+ form			Digit	NR4SD+ Encoding		
b_{2j+1}	b_{2j}	c_{2j}	c_{2j+2}	n^+_{2j+1}	n^-_{2j}	$\mathbf{b}_j^{NR+}$	one^+_j	one^-_j	two^+_j
0	0	0	0	0	0	**0**	0	0	0
0	0	1	0	1	1	**+1**	1	0	0
0	1	0	0	1	1	**+1**	1	0	0
0	1	1	0	1	0	**+2**	0	0	1
1	0	0	0	1	0	**+2**	0	0	1
1	0	1	1	0	1	**-1**	0	1	0
1	1	0	1	0	1	**-1**	0	1	0
1	1	1	1	0	0	**0**	0	0	0

Table 2: NR4SD+ Encoding

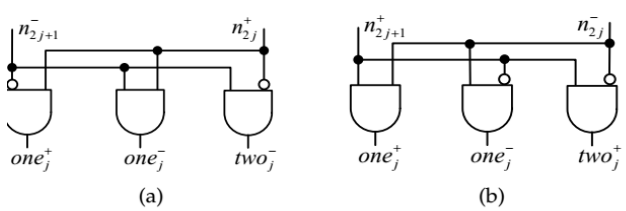

Fig.4.(a) NR4SD− and (b) NR4SD+ Encoding

Compared to the pre-encoded MB multiplier, where the MB encoding blocks are omitted, the pre-encoded NR4SD multipliers need extra hardware to generate the signals for the NR4SD− and NR4SD+ form, respectively. The Fig.5 shows the logical diagram of the PPG unit.

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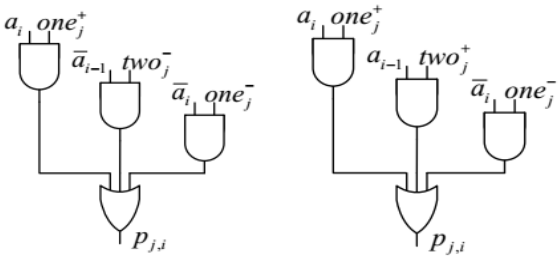


Fig.5.Generation of the ith Bit $p_{j,i}$ of PP_j

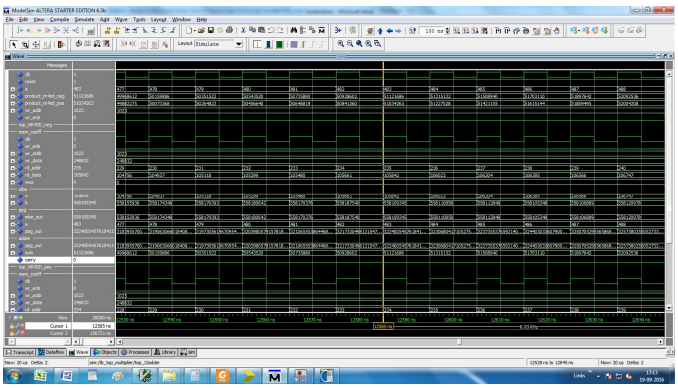
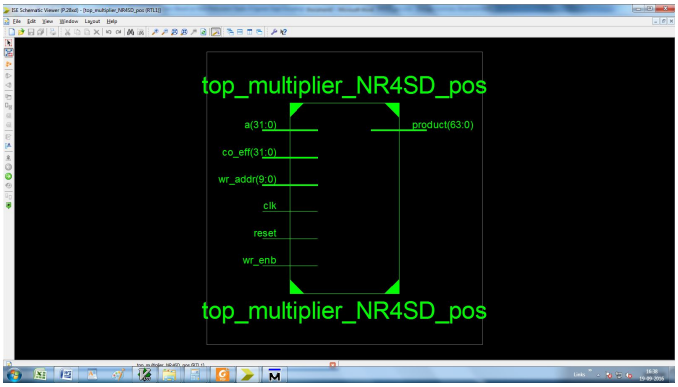
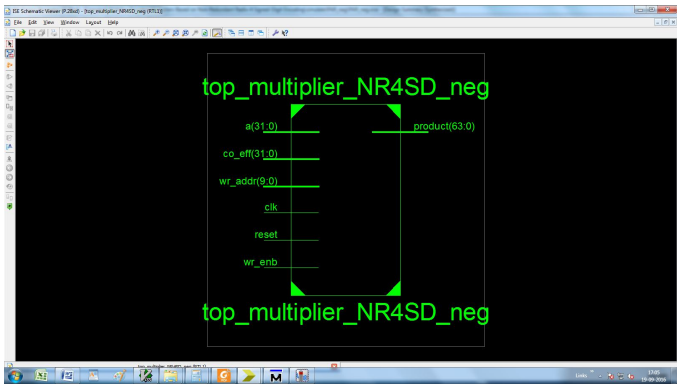


Fig.6 simulation results

RTL VIEW
NR4SD+



NR4SD-



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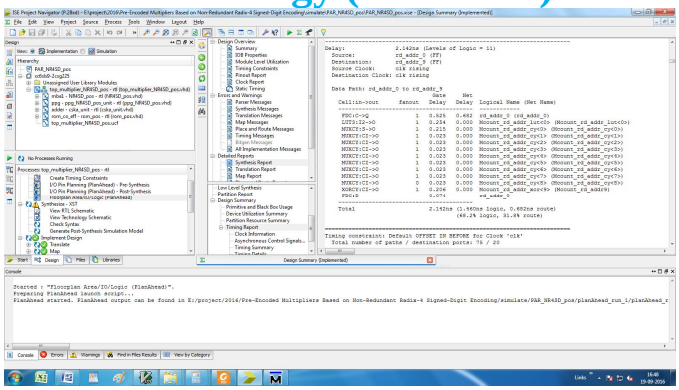
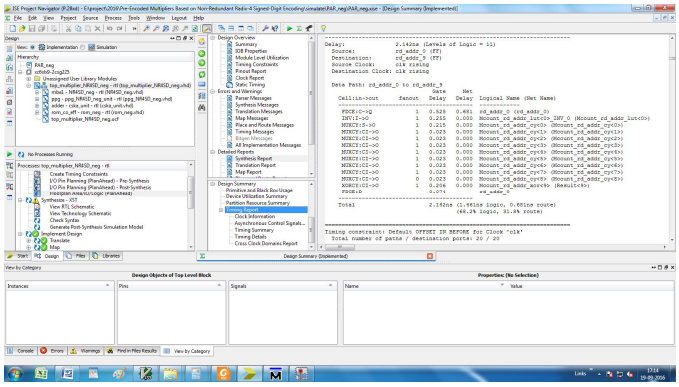
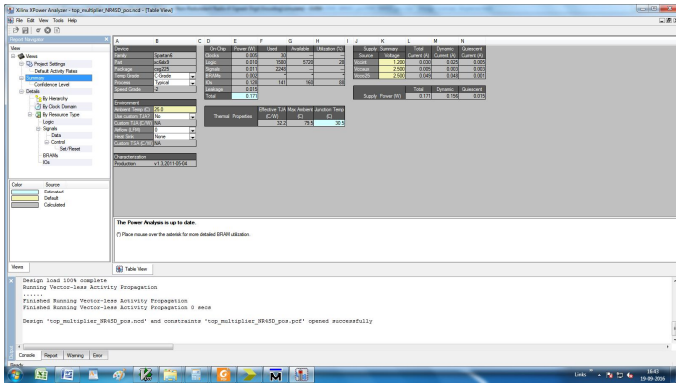


DELAY REPORT NR4SD+



NR4SD-



Power nr4sd+

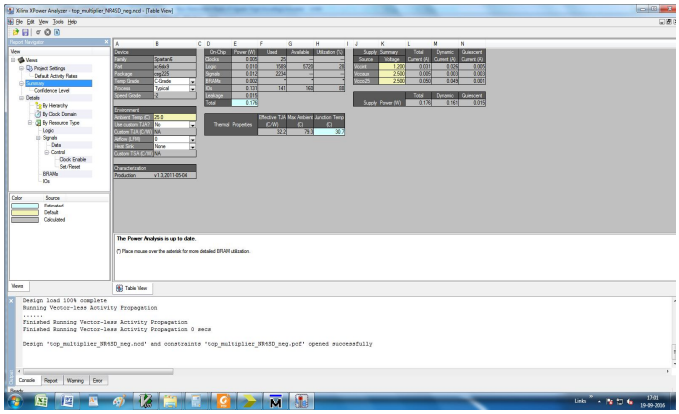


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Fig.4 shows the simulation results when implemented on the Xilinx tool with help of model sim.Fig.5 and fig.6 show the RTL view of both NR4SD+ and NR4SD- algorithms.Fig.7 and fig.8 show the delay report of both NR4SD+ and NR4SD- algorithms.Fig.9 and fig.10 show power report of both NR4SD+ and NR4SD- algorithms.

IV. CONCLUSION

We have discussed about the architecture of pre encoded multiplier offline encoding technique .This involves coefficient offline encoding reduces partial products as far as possible. Then, product is achieved using carry save adder ckts leading to further loss in delay. Delay obtained is around 2.14ns

V. ACKNOWLEDGMENT

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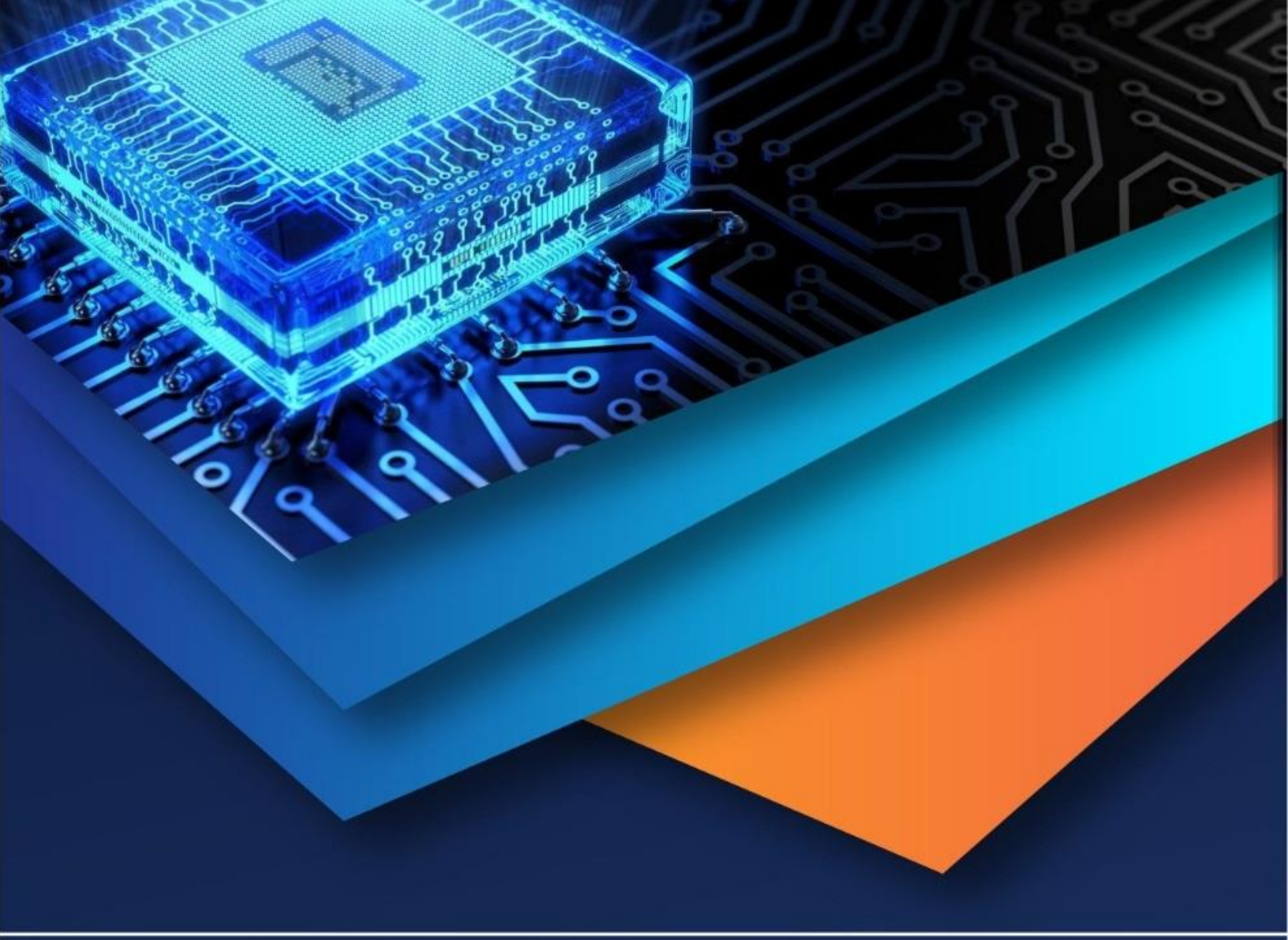

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