iJRASET
International Journal For Research in Applied Science and Engineering Technology



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 5 **Issue:** V **Month of publication:** May 2017

DOI:

www.ijraset.com

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Volume 5 Issue V, May 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

FBMC Modulation Scheme Implemented and Simulated in Verilog HDL for 5G Communications

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Abstract: ***Filter-Bank Multi-carrier (FBMC) is considered by recent research and projects as a key enabler for future 5g air interface. It helps to eliminate the defect of mobility synchronization and reduce the wastage of resource spectrum bandwidth of currently standardised Orthogonal Frequency Division Multiplexing (OFDM) in 4G communication. Therefore to test the FBMC scheme the availability of an efficient hardware becomes a high interest. Due to software based development facility of hardware unit, the rapid design and testing scenario have originated and applied in rapid scale. So in this paper software based environment Verilog (HDL) Hardware Description Language is used to implement and a virtual simulation is performed to verify the FBMC scheme. The implemented structure can be upgraded to increase the complexity of the hardware structure due to which less hardware resource can be used to design prototype hardware for FBMC scheme.***
Keywords— (FBMC) Filter-bank multi-carrier, 5G air interface, Verilog HDL, (QAM) Mapper, (IFFT) Inverse Fast Fourier Transform, Filter-bank, (FIR) Finite impulse response Filter.

I. INTRODUCTION

5G wireless technology is developing at an explosive rate and is currently one of the biggest areas of research within academia and industries. In this rapid development, signal processing technique plays the important role. In 2G, 3G and 4G, the peak service rate was the dominant metric for performance. Each of the previous generation was defined by a standout signal processing technology that represented the most important advancement made. However in the case of 5G there will be no dominant performance matric. Instead, a new signal processing technique will be used to continuously increase the peak service rates, and there will be a new emphasis on greatly increased capacity, coverage, efficiency (power, spectrum, and other resources), flexibility, compatibility, reliability and convergence. In the list of valid candidate the FBMC scheme is a promising technique which has the ability to provide the required specification towards satisfactory objectives. In this paper section II will define the proposed physical layer [1], [2] of FBMC the section III will describe the function of QAM Mapper unit [5] section IV will describe the pre-processing unit [1], [5] section V will describe the function of IFFT unit [3], [4], [10], [11] section VI will describe the Reorder unit [1] and section VII will describe the function of Filter –bank unit [5] and the implementing method for individual units are given in Verilog HDL.

II. FBMC PHYSICAL LAYER

The initial proposed physical layer structure for FBMC scheme [1] is shown in Fig. 1.

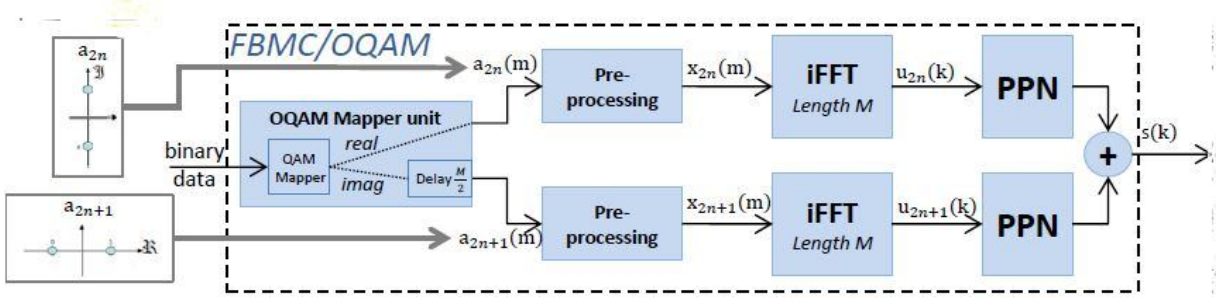


Fig.1. Physical layer for FBMC scheme.

The above physical layer structure is having four standard functional block. Functionality of each block will be explained in further topic of this paper. This block is designed initially for theoretical purpose. But for an efficient hardware unit [5], [2] the next

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Volume 5 Issue V, May 2017
ISSN: 2321-9653
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functional physical layer is proposed as shown in Fig. 2.

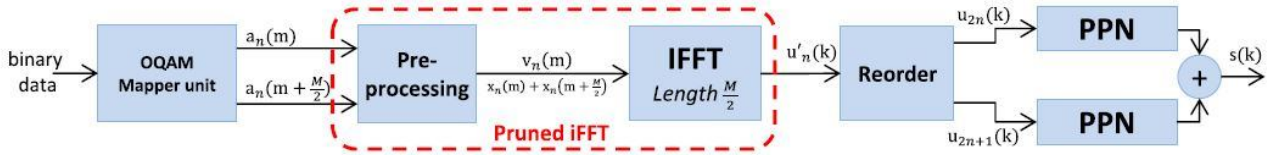


Fig.2. Physical layer for FBMC using Pruned IFFT.

The physical layer proposed in Fig. 2 [1] uses Pruned IFFT which means that it remove the entire un-necessary functional unit. It have removed the two pre-processing unit and combined it into one and it have include a reordering unit for making the data lines perfectly aligned for (PPN) Poly-Phase network [6] which is also called as filter bank. To design the physical unit in Verilog HDL the both proposed structure are been used. The physical layer used to implement in Verilog HDL is shown in Fig. 3.

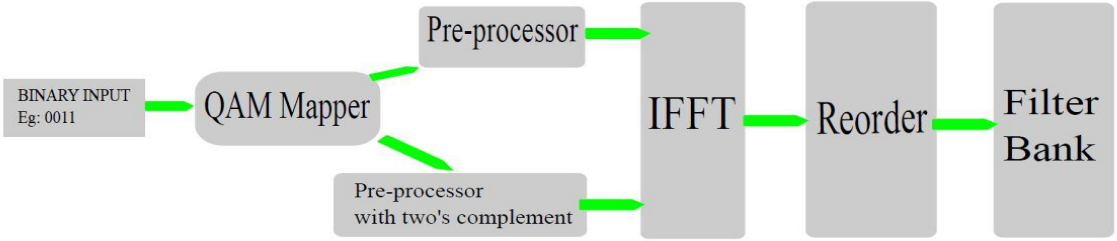


Fig. 3. FBMC Physical layer implemented in Verilog HDL.

The Fig. 3 FBMC physical layer structure is used in implementing the FBMC Physical layer in Verilog HDL. It consists of both the previously proposed physical layer characteristics. One is the two pre-processor units and second is the use of reordering unit. The description of individual unit is provided in next sections.

III.QAM MAPPER

Quadrature amplitude modulation (QAM) [2] is an analog as well as digital modulation scheme. In the case of digital modulation it uses bit streams as input and provides an output of magnitude and phase. The magnitude and phase can be denoted in coordinate axis as shown in Fig.4.

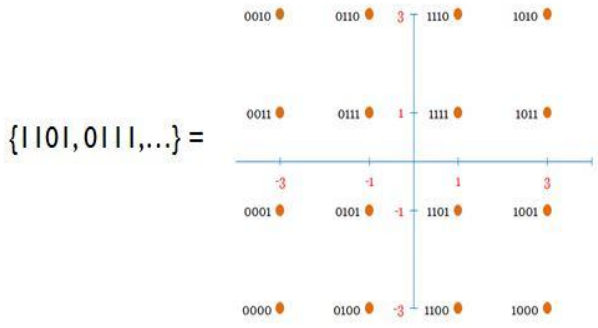


Fig.4. QAM Mapper functionality.

The Fig. 4 is showing a 16QAM Mapper unit. There are many QAM mappers like 4QAM, 8QAM, 16QAM, 32QAM. This QAM are mostly defined by the number of points in the coordinate system. Like in Fig.4 there are 16 points so its 16QAM and the vertical axis denote the magnitude of signal and the horizontal axis shows the phase of the signal. It's a method to convert a binary sequence into a complex sequence.

E.g.: 1101 = {1,-1}

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Volume 5 Issue V, May 2017
ISSN: 2321-9653
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0111 = {-1, 1}

A. QAM Mapper implementation in Verilog HDL

The hardware structure of a QAM Mapper will consist of (LUT) Look-up-Table. The content of the table will be the locos point of the coordinate system. The function of the mapper will be to take a binary stream and the output will be the locos point in the coordinate system. The Verilog format algorithm is shown in Fig.5.

```
case (Binary_Input)
 Binary_Input: begin Out_Magnitude = -8'd3; Out_Phase = -8'd3; end
 Binary_Input: begin Out_Magnitude = -8'd3; Out_Phase = -8'd1; end
.
.
.
.
Binary_Input: begin Out_Magnitude = -8'd1; Out_Phase = -8'd1; end
default: begin Out_Magnitude = 8'd0; Out_Phase = 8'd0 ; end
endcase
```

Fig.5: Algorithm for QAM mapper in Verilog HDL

IV. PRE-PROCESSOR

The pre-processor unit [2] function as FIFO First-in-First-Out. But this unit will not provide output in serial manner. The output should come in multiple outline formats because the output will be provided as input to the IFFT unit. This pre-processor are internally divided into two functions. One is for handling the real or magnitude input and the other for handling imaginary or phase input. The per-processor which handle the imaginary input will add an additional functionality which is the computation of 2's compliment of the input data and then to perform the FIFO function. The both blocks are shown in Fig.6 and Fig.7.

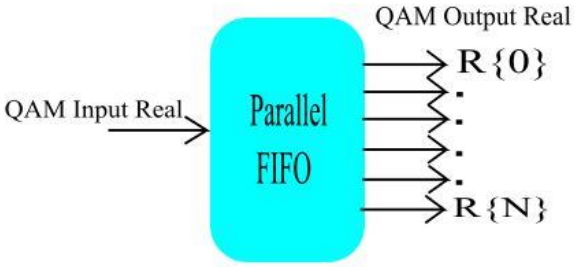


Fig.6: Pre-processor for Real data input.

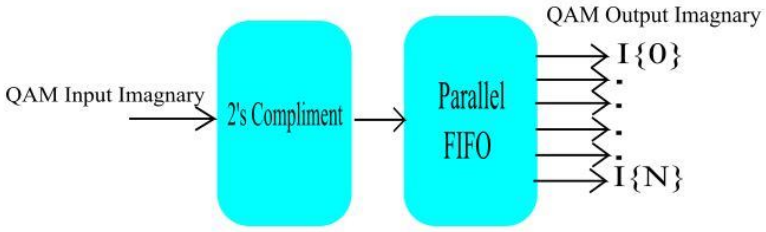


Fig.7: Pre-processor for Imaginary data input.

A. Pre-processor implementation in Verilog HDL

The hardware structure for pre-processor unit will have stacked output. The input will be obtained from single line from the QAM output port and the data will be stored in buffers which are sequenced by the help of an indexed number and with that index number the stack location of the data in the output line of the Parallel FIFO. In the case of imaginary data pre-processor the input data from the QAM mapper unit will be first given to the 2's complement unit and then the data in passed to the parallel FIFO unit. The Verilog format algorithm is shown in Fig.8 and Fig.9. This all process is done to use the algorithm of FFT in the form of decimation of frequency. Theoretically it's applicable to use FFT butterfly structure to obtain the IFFT functionality only when the complex

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Volume 5 Issue V, May 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

input of the FFT unit must be complex conjugate of the actual input which is pre obtained by the FFT process. Then only we can reuse the structure of FFT butterfly unit. So by this the pre-processing unit performs the necessary changes to the complex data. This can be properly processed by the IFFT unit.

```
index i=0;
always @(posedge CLOCK
begin
   if(i==0)
   PROUT-0 = PRINPUT;
.
                    .
                 If(i=N)
  PROUT-N = PRINPUT;
I=i+1
end
```

Fig.8: Algorithm for parallel FIFO

```
input [7:0] IMGDATAIN;
output  reg [7:0]DATAOUT;

DATATOUT=(~IMGDATAIN+ 8'b00000001);
```

Fig.9:Algorithm for 2's compliment

The algorithm in Fig.8 will be used in make the real data per-processor and the 2's complement algorithm in Fig.9 will be added in the parallel FIFO to obtain the pre-processor functional unit for pre-processor for imaginary data.

V. IFFT UNIT

The IFFT Inverse Fast Fourier unit [5], [6], [11] is an fastest way to perform inverse discrete Fourier transform by decreasing the computation requirement from N^2 to N*Log*N where N in the number of computation required. The basic formula of IFFT [6] is given below.

$$x_n = \frac{1}{N}\sum_{k=0}^{N-1} X_k e^{i2\pi kn/N}$$

Equation 1: IFFT or inverse Fast Fourier transform

A. Implementation of IFFT in Verilog HDL.

To implement the IFFT unit a Butterfly unit [7], [10] is been developed. This butterfly unit is the basic building block of the N point IFFT unit. The Fig.10 [7] shows the basic structure of the butterfly unit.

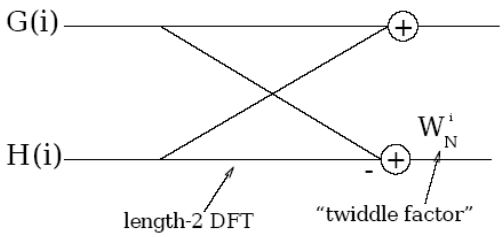


Fig.10: Butterfly unit.

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Volume 5 Issue V, May 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)

In the Fig.10 butterfly unit the two input real and complex data is provided in the G(i) and H(i) and the output in the upper part of the butterfly unit is the sum of the both input and the output of the lower part of the butterfly unit is the subtraction value of the both input followed with multiplying [8],[9] it with Twiddle factor W_n. This butterfly unit is used to build the N-point IFFT unit.

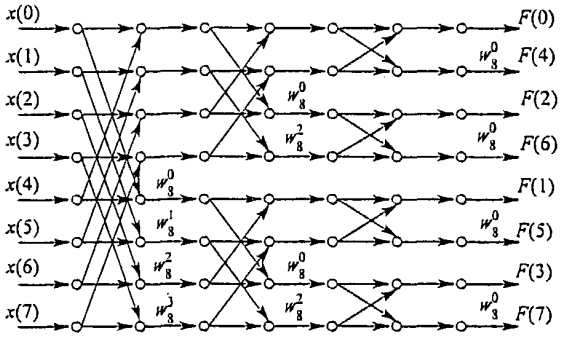


Fig.11: 8 point IFFT format using butterfly unit

In the Fig.11 its shown how one butterfly unit is been used to make a maze of unit which can perform 8 point IFFT.

B. Implementation of IFFT in Verilog HDL

The IFFT algorithm will contain one butterfly unit and that one module will be instantiate number of times with proper input and output with the proper application of the twiddle factor. The computation performed in the process does include a complex multiplication. And the formula used for complex multiplication is given below.

$$(x+yi)(u+vi) = (xu-yv)+(xv+yu)i$$

Equation 2: Complex multiplication

The Verilog HDL algorithm for IFFT unit is given in Fig.12 and Fig.13.

```
REALOUTDATA1=REALINPUTDATA1+REALINPUTDATA2;
IMAGOUTDATA1 = IMAGINPUTDATA1 + IMAGINPUTDATA2;
MEDREALDOUT1 = (REALINPUTDATA1 * REALTWID) - (IMAGINPUTDATA1 * IMAGTWID);
MEDIMAGDOUT1 = (REALINPUTDATA1 * IMAGTWID) + (IMAGINPUTDATA1 * REALTWID);
  MEDREALDOUT2 = (REALINPUTDATA2 * REALTWID) - (IMAGINPUTDATA2 * IMAGTWID);
MEDIMAGDOUT2 = (REALINPUTDATA2 * IMAGTWID) + (IMAGINPUTDATA2 * REALTWID);
REALOUTDATA2 = MEDREALDOUT1 - MEDREALDOUT2;
 IMAGOUTDATA2 = MEDIMAGDOUT1 - MEDIMAGDOUT2;
```

Fig.12: Algorithm of Butterfly unit

```
BUTTERFLY B11(.CLOCK(CLOCK),.REALTWID(W0R),.IMAGTWID(W0I)
              ,.REALINPUTDATA1(REALINP0),.IMAGINPUTDATA1(IMGINP0)
              ,.REALINPUTDATA2(REALINP8),.IMAGINPUTDATA2(IMGINP8)
              ,.REALOUTDATA1(TEMPREALOUT0_1),.IMAGOUTDATA1(TEMPIMGOUT0_1)
              ,.REALOUTDATA2(TEMPREALOUT8_1),.IMAGOUTDATA2(TEMPIMGOUT8_1));
.
.
REALOUT0 = TEMPREALOUT0_1;
IMGOUT0 = TEMPIMGOUT0_1;
REALOUT 8 = TEMPIMGOUT8_1;
IMGOUT8 = TEMPIMGOUT8_1;
```

Fig.13: Algorithm for IFFT

In the Fig.12 the Equation 2 has been implemented to perform the complex multiplication. In Fig.13 the butterfly module is instantiated number of times and the Fig.11 structure is been implemented by the butterfly module.

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ISSN: 2321-9653
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VI. REORDER

The reorder unit is used to make the output obtained from the IFFT unit in proper numerical order. In Fig.11 the output of the IFFT unit is shown. In that output the series are not in order. The output order is followed as 0, 4, 2, 6, 1, 5, 3, and 7. This order is to me made proper order of 0, 1, 2, 3, 4, 5, 6, and 7.

A. Implementation of Reorder in Verilog HDL.

In the reorder algorithm there is only wired connection from the input port to the specific output port. The Fig. 14 shows the algorithm of reorder in Verilog HDL format.

```
REALOUT0 = REALINP0;
IMGOUT0  = IMGINP0;
REALOUT1 = REALINP8;
IMGOUT1  = IMGINP8;
REALOUT2 = REALINP4;
IMGOUT2  = IMGINP4;
REALOUT3 = REALINP12;
IMGOUT3  = IMGINP12;
.
.
```

Fig.14: Algorithm of Reorder using Verilog HDL

This program will consist of all the port involved in the IFFT unit and provide the numerical proper order format needed for further process.

VII. FILTER BANK

The output obtained by the IFFT is actually considered as the magnitude level of a sub-band of a frequency spectrum. The digital bit stream which was provided by the QAM Mapper is converted into frequency sub-band format by the IFFT. In OFDM these sub-band will have a cyclic-prefix to define the difference between each sub band and to remove the possibility of inter-symbol interference. But this strategy of providing the cyclic-prefix comes with the issue of bandwidth wastage. In the case of FBMC the Filter-bank which consist of N number of (FIR)Finite Impulse Response Filter [6], [5], [1] are used for N-point IFFT. The structure of the individual filter is as shown in Fig. 15.

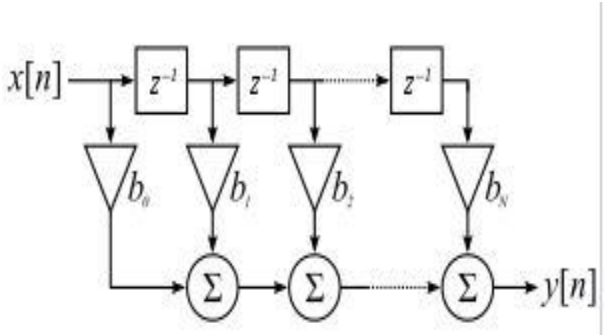


Fig.15: FIRFilter.

The above Fig.15 shows a FIR filter. It consists of delay element which mostly consists of D flip-flop. Each delay element will stop the further steps by duration of one unit. There are coefficients of filter which in Fig.15 are $b_0, b_1, b_2, \ldots, b_n$. These coefficients are multiplied with the input provided by the input of filter and through the delay unit. Further the individual product obtained is added and the resulting output will provide a spectrum structure of a band according to the input bit stream.

A. Implementation of Filter-bank in Verilog HDL.

The Filter-bank will require a D flip-flop and a multiplier and a common adder. In this case we will design a single filter and use the module repeatedly to make a filter-bank. The algorithm of individual filter is given in Fig.17 and for the filter-bank is given in Fig.18. The algorithm of D flip-flop is given in Fig.16.

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ISSN: 2321-9653
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```
always @(posedge CLOCK)
   begin
   begin
   DOUT <= DINP;
   if ( RESET == 1)
   begin
   DOUT <= 0;
   end
   end
   end
```

Fig.16: D Flip-flop Algorithm

```
assign M0 = DATAIN * H0;
   assign DATOUT1[0] = M0;
   DFLIP DF1(.CLOCK(CLOCK),.RESET(RESET),.DINP(DATAIN),.DOUT(D0));
   assign M1 = D0 * H1;
   assign DATOUT1[1] = M0 +M1;
   DFLIP DF2(.CLOCK(CLOCK),.RESET (RESET),.DINP(D0),.DOUT(D1));
   assign  M2 = D1 * H2;
.
assign DATOUT1[7] = M0+M1+M2+M3+M4+M5+M6+M7;
```

Fig.17: Individual FIR Filter

```
FIRFILT F0(.CLOCK(CLOCK),.RESET(RESET),.DATAIN(RINP0),.DATOUT(ABOUT0));
FIRFILT F1(.CLOCK(CLOCK),.RESET(RESET),.DATAIN(RINP1),.DATOUT(ABOUT1));.
.
.
FIRFILT F14(.CLOCK(CLOCK),.RESET(RESET),.DATAIN(RINP14),.DATOUT(ABOUT14));
FIRFILT F15(.CLOCK(CLOCK),.RESET(RESET),.DATAIN(RINP15),.DATOUT(ABOUT15));
```

Fig.18: Filter-bank algorithm

VIII. RESULTS

The simulation is done in Vivado 2016.4 every module is individually simulated and the respective output is shown as follows:

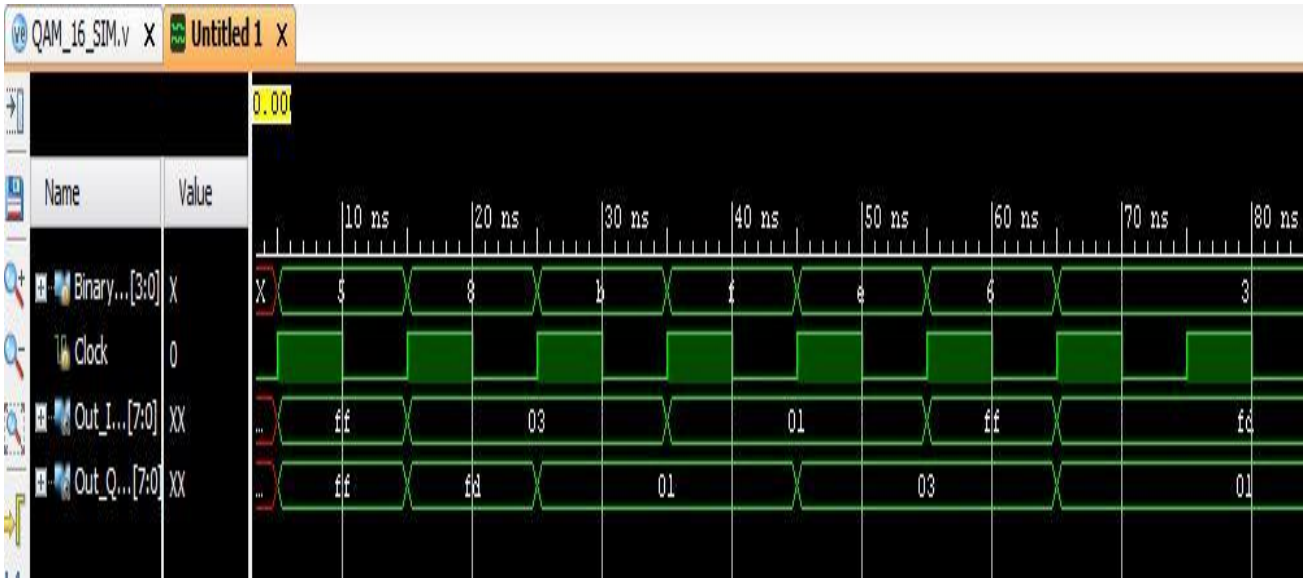


Fig.19: 16-QAM Mapper

Fig.19 shows the 16-QAM mapper design output where the binary series input is provided as 5, 8, 11 (b), 15 (f), 14 (e), 6 and 3. The

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ISSN: 2321-9653
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outputs obtained are two values one is Real or Magnitude and other is Imaginary or Phase which are shown in the Out lines in Fig.19.

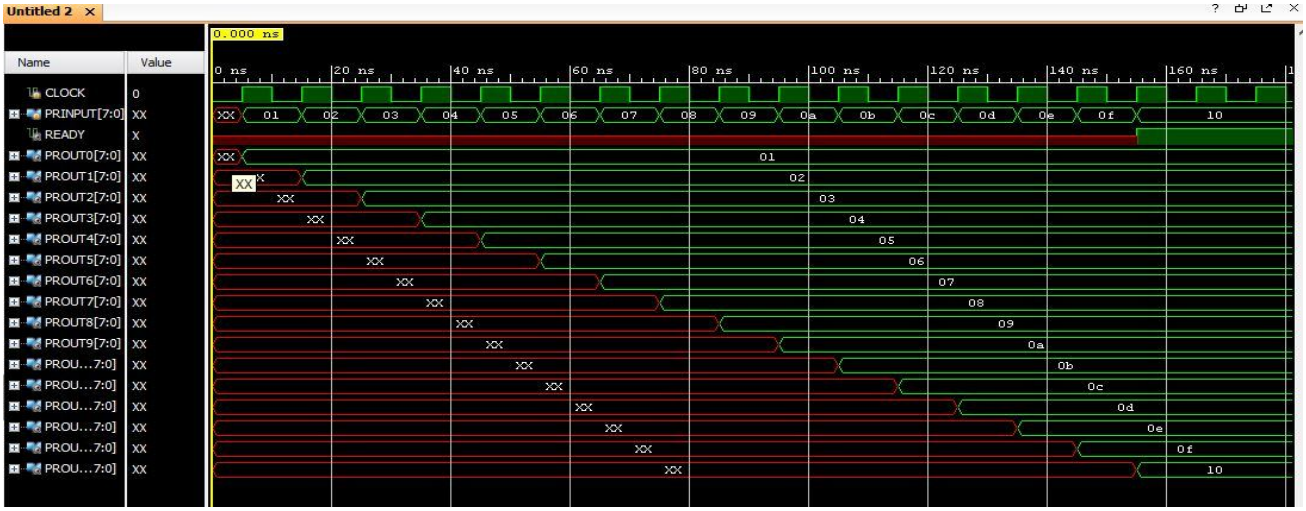


Fig.20: Pre-processor of real data

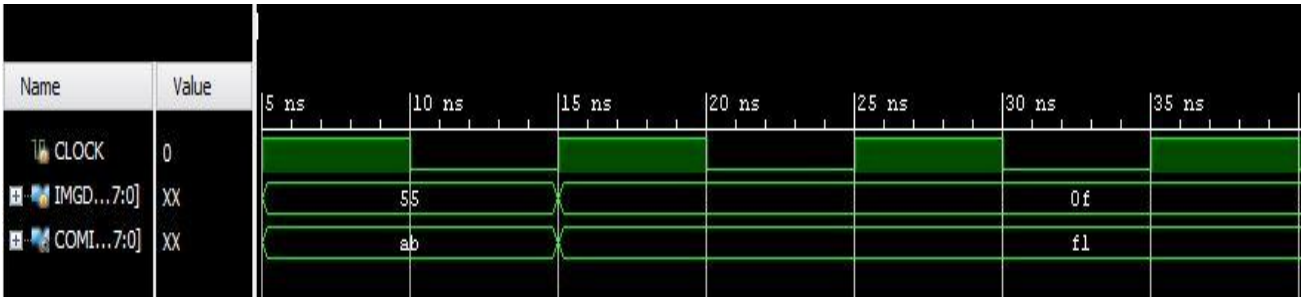


Fig.21: 2's Compliment

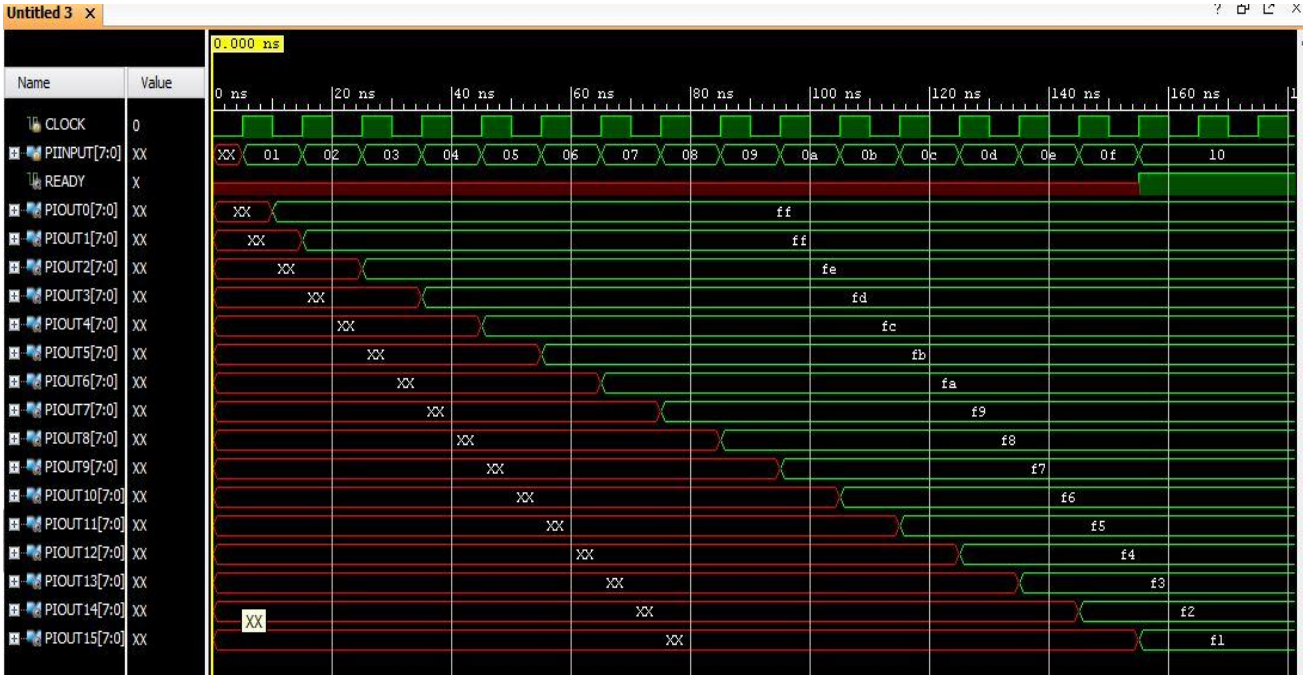


Fig.22: Pre-processor of Imaginary data

In the Fig.20, Fig.21and Fig.22 shows the Pre-processor simulation in the real data pre-processor the data are sequentially added to

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the port lines and when all the data have arrived then the READY signal in provided. In the case of imaginary data first the data are two's complimented and then provided to the pre-processor unit.

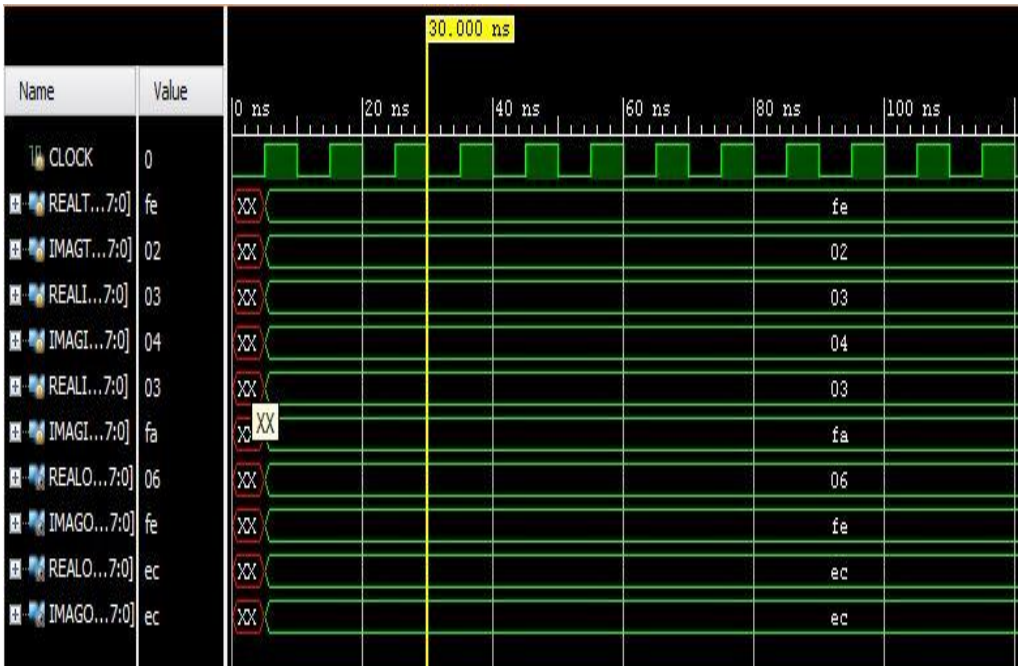


Fig.23: Butterfly unit

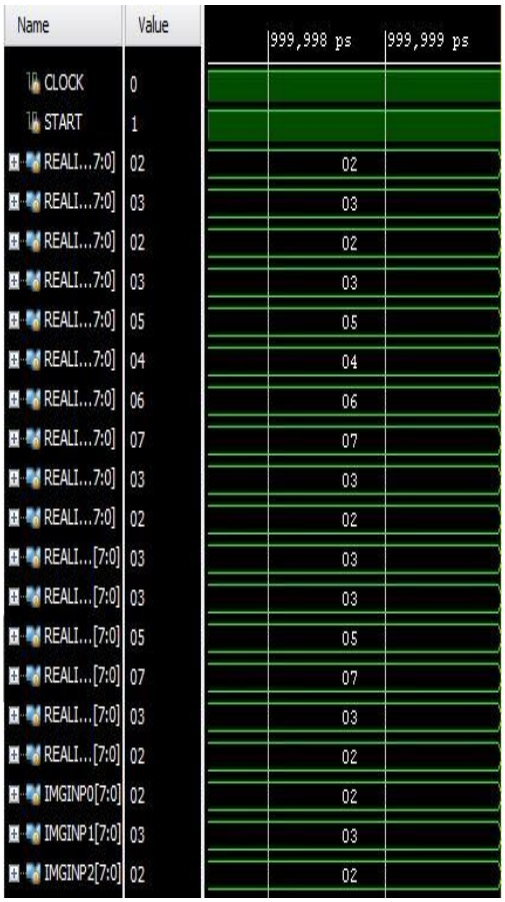


Fig.24: IFFT input real and imaginary data

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ISSN: 2321-9653
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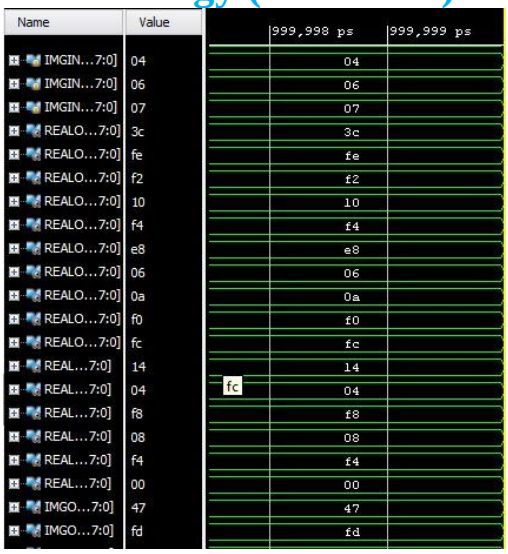


Fig.25: IFFT output real and imaginary data

The Fig.23, Fig.24 and Fig.25 shows the simulation result of butterfly unit first and then this butterfly unit is used a lot number of time according to the IFFT structure shown in Fig.11. The input for IFFT is shown in Fig.24 and the output from IFFT is shown in Fig. 25.

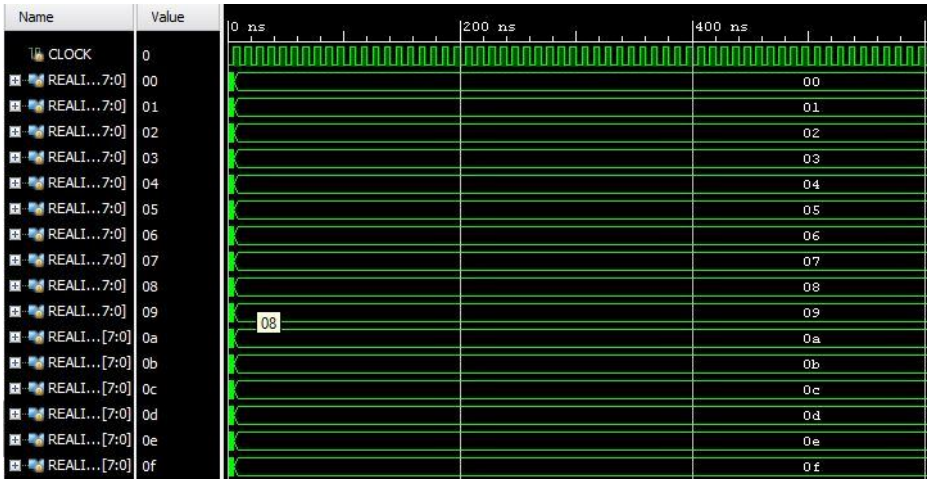


Fig.26: Reorder unit input

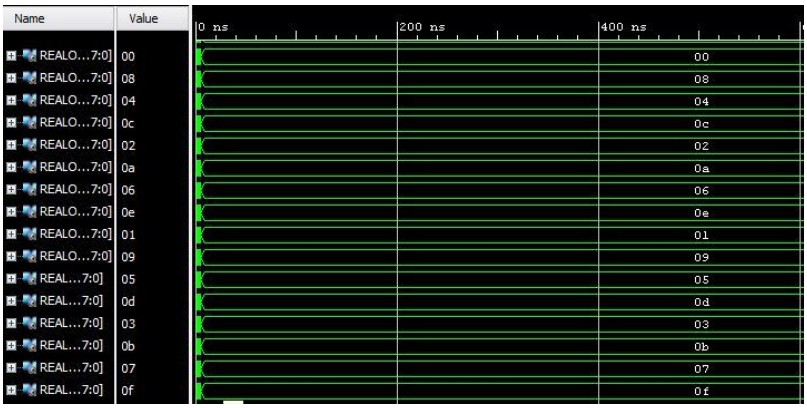


Fig.27: Reorder unit output

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Volume 5 Issue V, May 2017
ISSN: 2321-9653
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The Fig.26 and Fig.27 shows the reorder input and output respectively which is obtained from the previous IFFT unit.

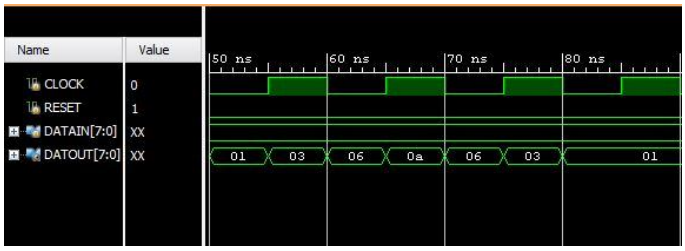


Fig.28: FIR filter

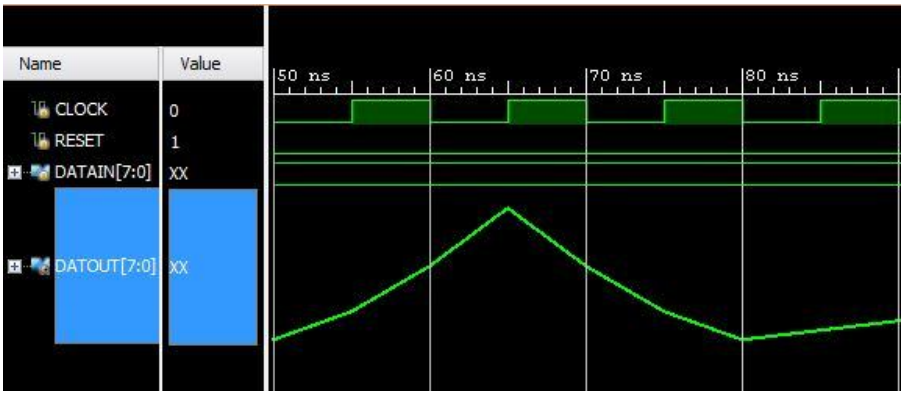


Fig.29: FIR filter analog form

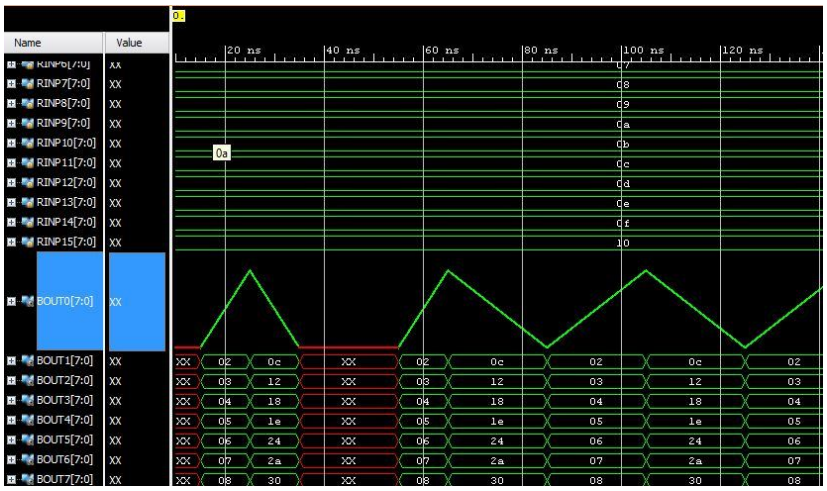


Fig.30: Filter-Bank in both analog and digital form.

The Fig.28 and Fig.29 showed the individual FIT filter output in both digital and analog form. The Fig.30 shows the output of filter-bank in both analog and digital form. The filter bank is made up of a collection of FIR filters.

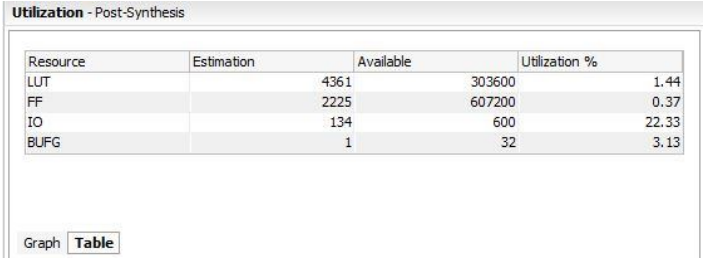


Fig.31: Hardware resource used.

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Volume 5 Issue V, May 2017
ISSN: 2321-9653
International Journal for Research in Applied Science & Engineering Technology (IJRASET)



Fig.32: Power utilised by the implemented device.

At last the whole individual units are combined into one and implemented in which the input will be the binary sequence and the output will be the Filter-bank sub-band value of the spectrum. In Fig.31 and Fig.32 the total number of resource unit used is specified and the power on the chip is analysed.

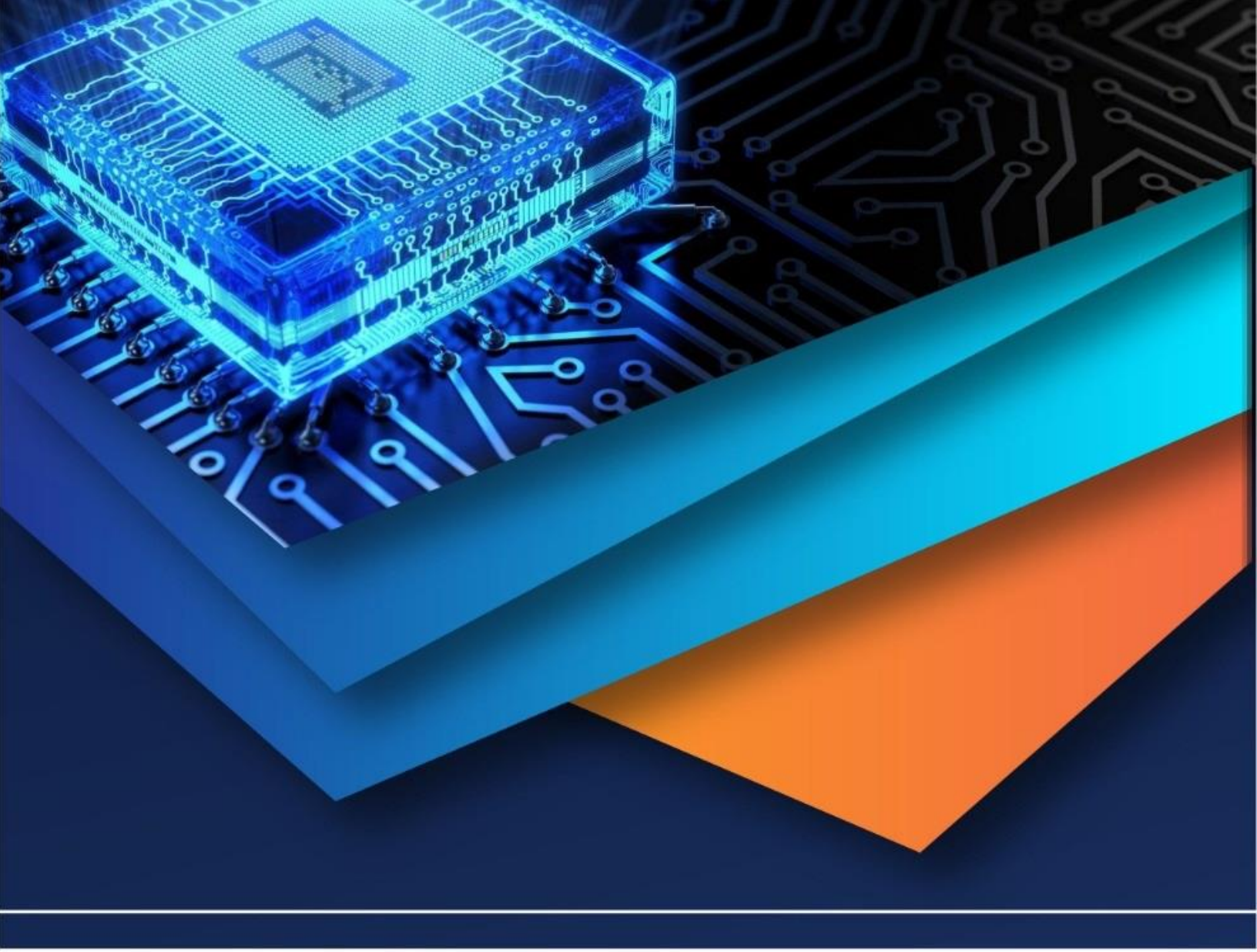
IX. CONCLUSION

The FBMC physical layer which is a contender for future 5G communication technology is defined in this paper. The every unit of the physical layer was properly described and the Verilog HDL format algorithm is shown in the figures above. By this simulation we can decide that the FBMC physical layer hardware structure does work. For the future scope we can make the working architecture more complex by using parallel IFFT which can reduce the use of Input and Output ports in large manner.

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