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Implementation of High Speed Vedic Multiplier for Digital Signal Processing Using Multiplexer Based Adder

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Abstract: ***Digital signal processors (DSPs) are very important in various engineering disciplines. Fast multiplication is very :important in DSPs for convolution, Fourier transforms, etc. A fast method for multiplication based on ancient Indian Vedic mathematics is proposed in this paper. The whole of Vedic mathematics is based on 16 sutras (word formulae) and manifests a unified structure of mathematics. Among the various methods of multiplication in Vedic mathematics, Urdhava tiryakbhyam is discussed in detail. Urdhava tiryakbhyam is the general multiplication formula applicable to all cases of multiplication. The coding is done in Verilog and synthesis is done using Xilinx ISE 14.5. The combinational delay obtained after the synthesis is compared with existing multiplier. Further, this Vedic multiplier is used in matrix multiplication. This Vedic multiplier can bring great improvement in the DSP performance.***

Keywords: ***Vedic multiplier,Urdhava tiryakbhyam, Verilog HDL, DSP.***

I. INTRODUCTION

Multipliers are frequently used in DSP, image processing architectures and microprocessors. It plays an important fundamental function in arithmetic operations. These days in modern VLSI design delay in data path is considered as a critical parameter. In present time designers are demanding high speed of operation, so it is essential to minimize the delay. There has been lot of researches and work to reduce the delay and now designers have shifted their focus on making a multiplier circuit which are efficient and considerably faster.

A high speed processor performance greatly depends on the multiplier, in most digital signal processing systems as well as in all-purpose processors which is one of the essential hardware components also its consumed area is more. Vedic multiplier gives the fast speed of operations than the conventional multiplier and requires less system memory. As compared to existing multiplier design this multiplier requires very small area. Here in this work we use MUX based adder for designing Vedic multiplier, this adder minimize the delay and reduced consumed area. In this paper 16- bit Vedic multiplier using MUX based adder has been designed The results shows that the proposed 16- bit Vedic multiplier is faster than 16- bit Vedic multiplier with normal adder. The reduction in the delay is approximately 30.6%. The main purpose of this work is to design and implement a high speed 16 X 16 bit Vedic multiplier by combining the best technique in Vedic mathematics named Urdhva Tiryagbhyam and MUX based adder.

II. VEDIC MATHEMATICS

The ancient Indian Vedic mathematics is now currently used in our global silicon chip technology for easier and faster calculations. The proposed Vedic multiplier is based on the Vedic multiplication formulae (Sutras). By using three sutras of Vedic mathematics the complex number multiplication can be done, which are Urdhva Tiryakbhyam sutra, Ekadhikena Purvena, and Nikhilam Navatascaraman Dasatah or simply Nikhilam. The Nikhilam sutra of Vedic mathematics can only be applied to large number multiplication. While the Urdhva Tiryakbhyam method of Vedic mathematics can be efficiently applied to all cases of multiplication. This is a universal method for obtaining fast multiplication which can be applied everywhere. It is very simple and easy to implement. For the multiplication of two numbers in the decimal number system these Sutras have been traditionally used. In this present work, we apply the same ideas to the binary number system for making the proposed algorithm compatible with the digital hardware.

A. Urdhva Tiryagbhyam

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Urdhva Tiryakbhyam Sutra is a general multiplication formula which is applicable to all cases of multiplication. It literally means "Vertically and crosswise". This Sutra has been conventionally used for multiplication of two numbers in the decimal number system. The same idea has been applied for binary multiplication in this work. By breaking into smaller sizes, this can solve the multiplication of larger number (N X N bits). The 2 x 2 Vedic multiplier are basic building module through which higher multiplier are designed by splitting into smaller sizes.

This algorithm can be implemented into three steps which are as follows:

Step-1: The first step is vertical multiplication of LSB of both multiplicands.

Step-2: Second step is crosswise multiplication and additions of the partial products.

Step-3: Third step is vertical multiplication of MSB of the multiplicand and addition with the carry propagated from step 2.

For better understanding consider 2-bit two binary number are a1a0 and b1b0. The below figure 1 shows the 2 bit multiplier.

The expression of two bit Vedic multiplier is:

s0 = a0 and b0
s1 = (a1 and b0) XOR (a0 and b1)
c1 = (a1 and b0) and (a0 and b1)
s2 = c1 XOR (a1 and b1)
c2 = c1 and (a1 and b1)
sum = {c2,s2,s1,s0}

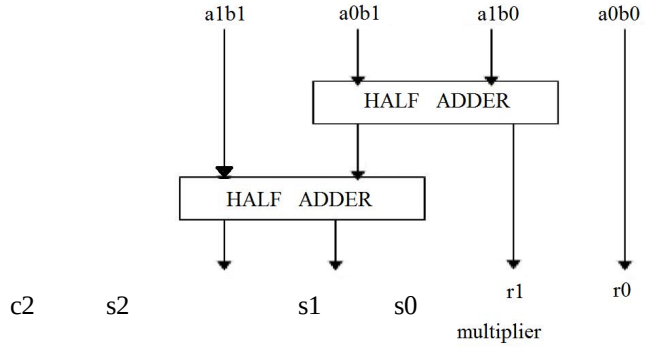

Figure 1: Line Diagram for 2 X 2 Bit binary multiplication using Urdhva Tiryagbhyam Sutra

B. Algorithm for 16 X 16 Bit binary numbers Multiplication Using Urdhva Tiryagbhyam:

A=A15A14A13A12A11A10A9A8 A7A6A5A4A3A2A1A0
X1 X0
B=B15B14B13B12B11B10B9B8 B7B6B5B4B3B2B1B0
Y1 Y0

X1 X0
* Y1 Y0

F E D C

CP = X0 * Y0 = C
CP = X1 * Y0 + X0 * Y1 = D CP = X1 * Y1 = E
Where CP=Cross product

C. Nikhilam Sutra

Nikhilam Sutra literally means "all from 9 and last from 10". Although it is applicable to all cases of multiplication, it is more efficient when the numbers involved are large.

To perform multiplication with Nikhilam Sutra, compliment of the numbers from the nearest base is required, larger is the original number, lesser the complexity of the multiplication. So this method is more efficient for large numbers which are nearer to the base. We first illustrate this Sutra by considering the multiplication of two decimal numbers (97 * 94) where the chosen base is 100 which is nearest to and greater than both these two numbers.

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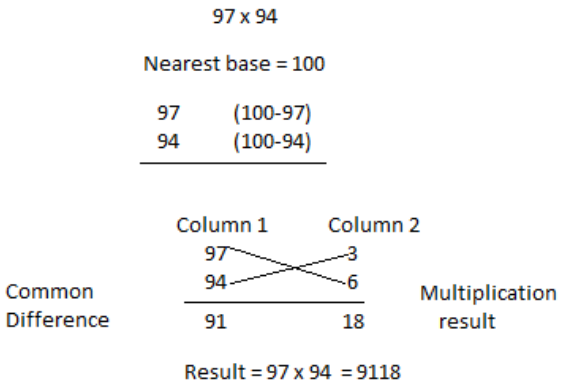

Figure 2: Multiplication Using Nikhilam Sutra

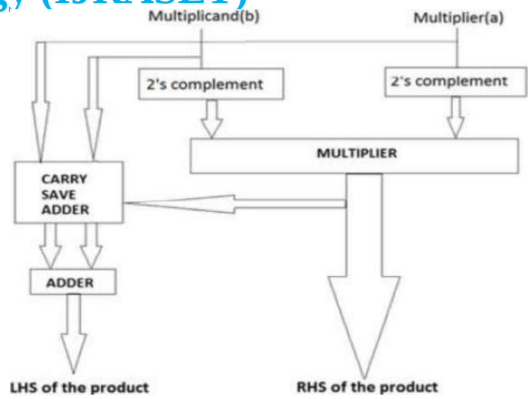

Figure 3: Architecture of Nikhilam Sutra

The right hand side (RHS) of the product can be obtained by simply multiplying the numbers of the Column 2 (3*6 = 18). The left hand side (LHS) of the product can be found by cross subtracting the second number of Column 2 from the first number of Column 1or vice versa 97 - 6 = 91 or 94 - 3 = 91. The final result is obtained by concatenating RHS and LHS (Answer = 9118).

III. MUX BASED ADDER

For efficient implementation adders become a critical hardware unit of multiplier. The speed of multiplier ultimately increased when the delay of the adder is reduced. In terms of delay and power dissipation, it is observed that full adder with multiplexer and XOR gate gives best performance, especially. It consists of two XOR gates and one 2xl MUX as shown in Fig. 4.

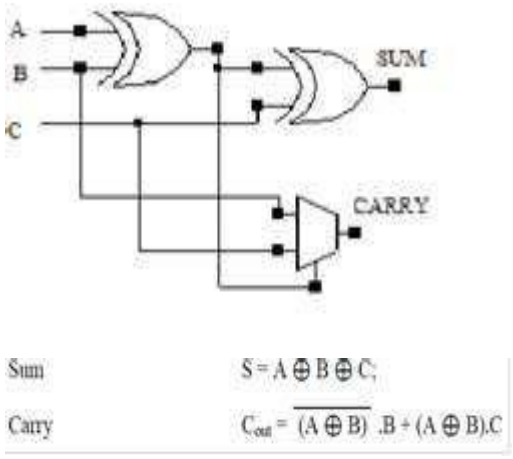

Figure 4: Architecture of MUX based adder

By using logical effort method we can calculate delay mathematically instead of using simulation tools. It gives a simple method to select best logical topology. Let us assumed ‘d’ is the delay for a single stage network in term of is logical effort ‘g’, electrical effort ‘h’ and parasitic delay ‘p’, than the delay can be calculated by the equation (1) as given below

$$d = g*h+p; \quad (1)$$

where 'g 'represents logic gate's ability to produce output current (Compared to inverter, how much worse it is in producing output current), 'h' gives ratio of output capacitance to input capacitance and p gives delay of gate due to internal capacitance.

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IV. DESIGN OF 16 X 16 VEDIC MULTIPLIER USING MUX BASED ADDER

The 2 x 2-bit Vedic multiplier is the basic building section for the system. Two Half adders are required in designing 2 x2 Vedic Multiplier, Figure 5 gives the architecture of 2 x 2 bit Vedic multiplier.

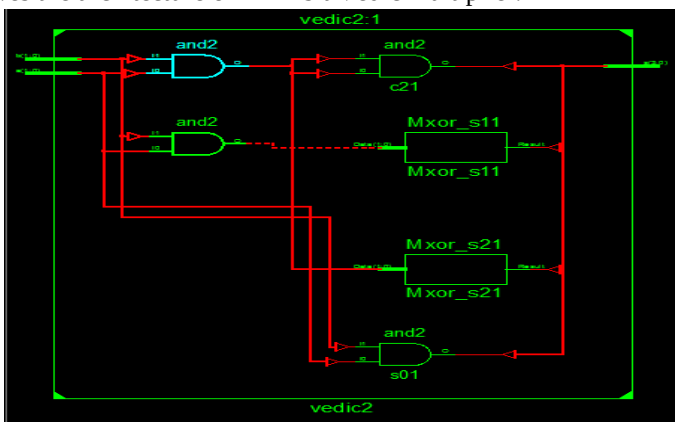

Figure 5 architecture of 2 x 2 bit Vedic Multiplier

The 4 x 4-bit multiplier is designed by using four 2 x 2-bit Vedic multiplier . The 8 x 8 bit Vedic multiplier is designed by using four 4 x 4 bit Vedic multiplier building blocks. The approach applied for designing a 16 x 16-bit Vedic multiplier by using four 8 x 8 bit multiplier blocks and two 24-bit and one 16-bit MUX based adder blocks is shown in figure 6.

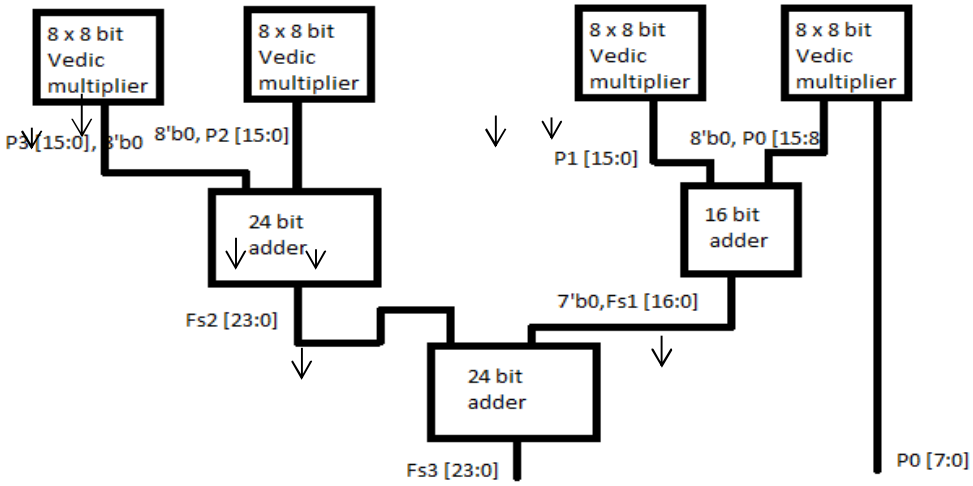

Figure 6 Block diagram of 16 x 16 bit Vedic Multiplier using MUX based adder

V. RESULT

A. Synthesis

The Verilog code of proposed Vedic multipliers (using MUX based adder) and conventional Vedic multiplier are synthesized using XILINX ISE 14.5. The figure 7 & 8 shows the RTL diagrams of both multipliers.

The functionality of Vedic multiplier is verified and confirms the operation of the design from the simulated waveforms. The combinational delay is reduced drastically with a little bit of trade off in terms of area. ISim simulator is used for simulation purpose. Figure 9& 10 shows the Simulation result for 16 bit Vedic multiplier in which 'P1' and 'P2'are same set of inputs and 'out' is their product and table 1 gives the delay and number of slice LUTs comparison between these two design architecture.

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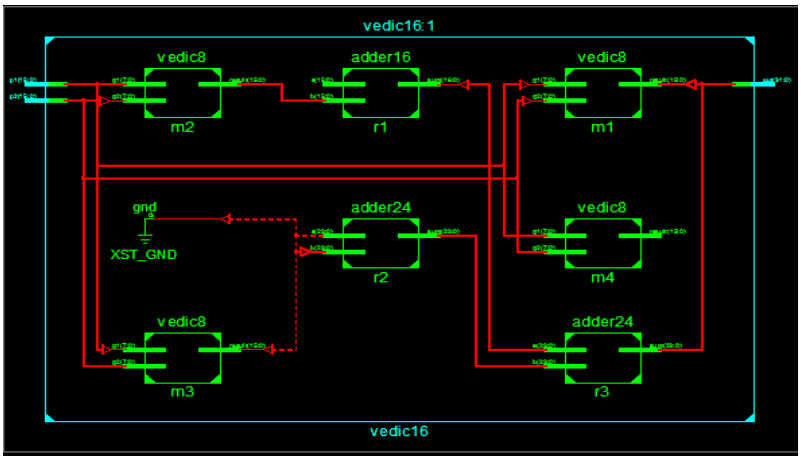

Figure 7: RTL view of 16x16 conventional Vedic multiplier

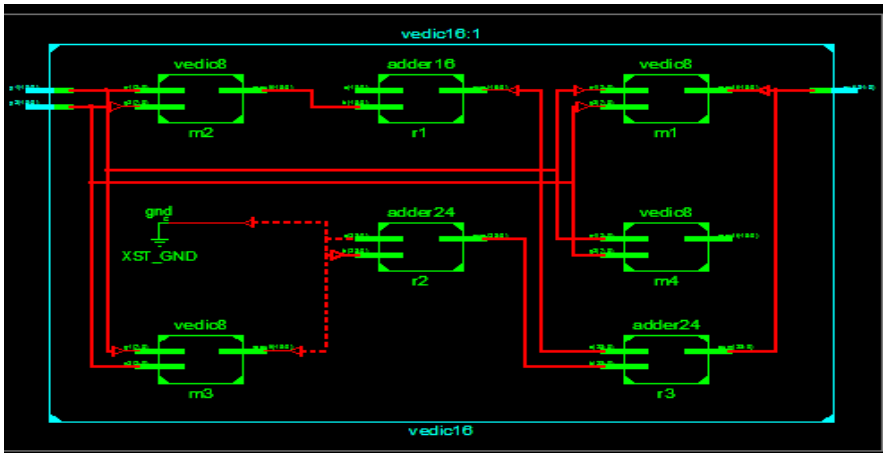

Figure 8**:** RTL view of 16x16 Vedic multiplier using MUX based adder

B. Simulation

Simulation of 16 X 16 bit Vedic Multiplier using MUX based adder: The Simulation Result of 16X 16 bit Vedic Multiplier using MUX based adder are shown in figure 9 and Simulation result for 16 X 16-bit conventional Vedic multiplier is shown in figure10 in which P1= 1111000000000000 and P2= 1000111111111111 is taken and result out =10000111000000000000000000000000 is obtained.

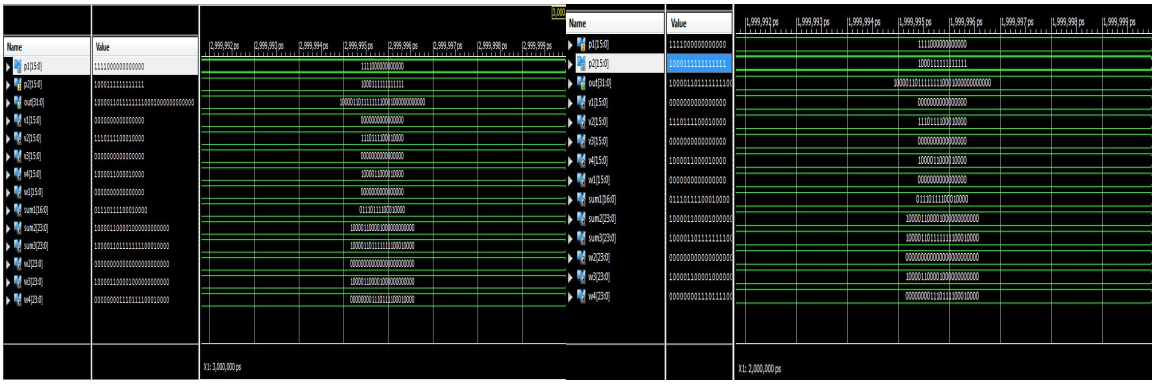

Figure 6: Simulation Result of 16X 16 bit
Conventional multiplier Figure 7: Simulation Result of 16X 16 bit Vedic multiplier using MUX based adder

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using Brent Kung adder

Table 1:

Type	No. of Bits	No. of bonded IOs	Delay (ns)	Level of logic	Number of Slice LUTs
	16	64	20.347	23	623
Vedic multiplier using MUX based adder	16	64	16.142	23	513

Conventional Vedic multiplier

V. CONCLUSION AND FUTURE WORK

This paper work presents a high performance design for multiplication by combining the feature of Vedic mathematics and MUX based adder. When we compared our purposed design with conventional Vedic multipliers proposed design gives much less delay. We conclude that the proposed Vedic multiplier is approximately 30% faster from conventional Multiplier. The multiplier architecture and fast performance makes this particularly attractive for VLSI implementations. For future work, its performance within MAC unit and ALU can be tested and compared with other conventional and Vedic designs. This 16 bit Multiplier can be further extended to 32 bit or 64 bit multiplier.

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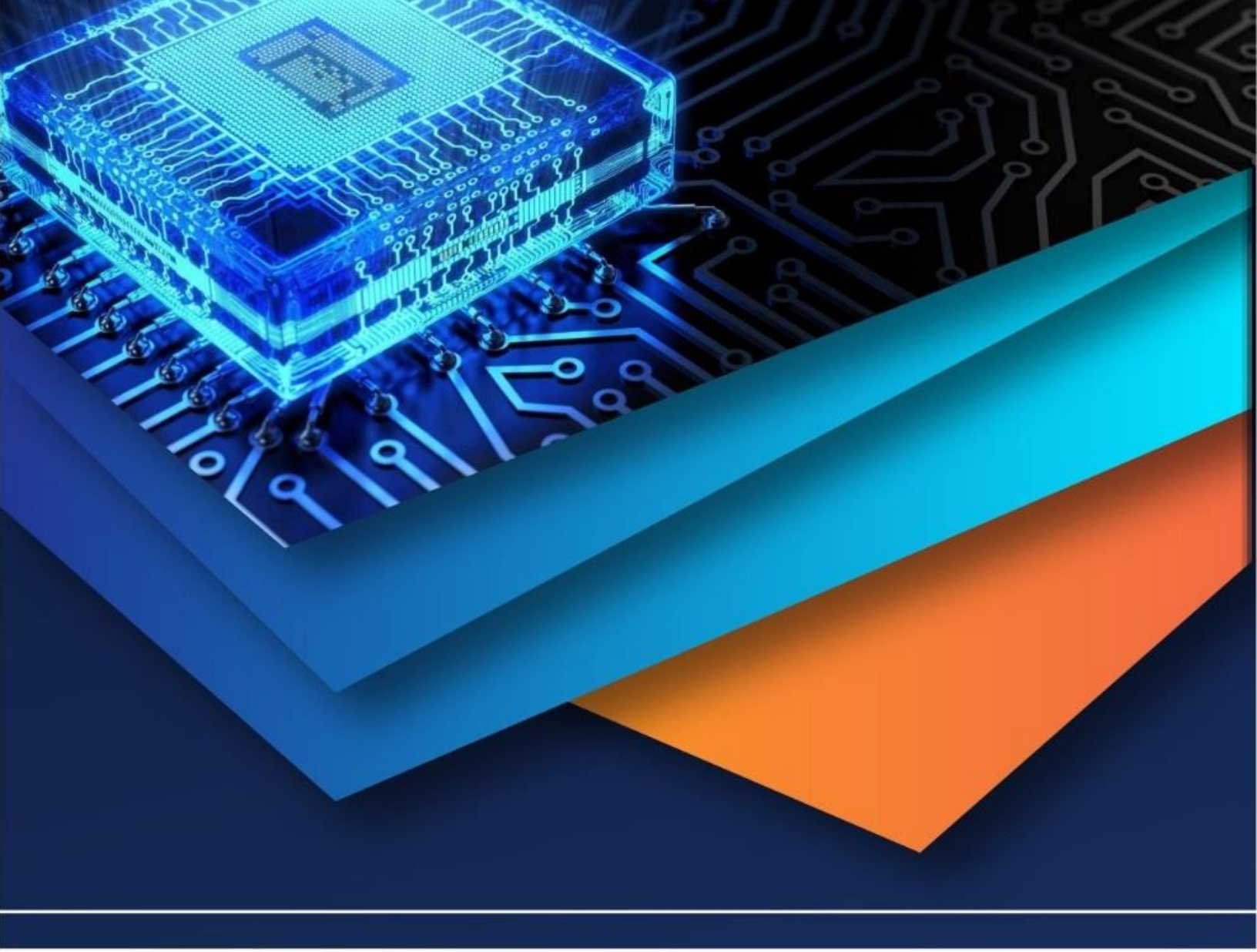

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