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Design A Power Efficient Compressor Using Adders

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Abstract*:This paper explore the design of different types of Adder and see the comparison between the result with previous work already done. By using Full Adder cell we design the Compressor circuit for the various application of the DSP systems. The modern VLSI design it is very important and the main field to concern about is the area, power and the power delay product. Use of the approximate Adder circuit is reduce the complexity of the circuit and also suitable for the field of reducing power and the switching complexity of the arithmetic circuits. Various type of 4:2 Compressors are compared with their respective designs and see the accurate result in term of better performance and the better output.
Keywords— Adders, CMOS technique, compressor, Tanner EDA.

I. INTRODUCTION

In the field most of these structure implementations, compressor are directly within the complex path describing the overall circuit, due to which the demand for high-speed and low-power compressors is continuously increasing. This paper presents new compressor architectures that the use of multiplexers in place of XOR gates to expeditiously use the outputs from the previous stages and enhance the overall performance .The bring forth need of designing low power VLSI circuits has been increased vastly due to increased demand of portable devices like palmtops, cellular and mobiles. Further to integrate more number of devices on chip, scaling of device size is required. But there are number of problems in scaling of bulk MOSFETs. Multiplication is a basic arithmetic operation important in applications like digital signal processing which trust on efficient implementation of generic arithmetic logic units (ALU) and floating point units to carry out dedicated operations like convolution and filtering. In the implementation of multipliers, the main phases are generation of partial products, reduction of partial products using CSA and a carry propagation adder for the computation of the final result. It is obvious that the second phase, that is, the reduction of the partial products contributes most to the overall delay, area and power. It is because the use of multiplexers improves the speed when placed in the critical path. Many of the Compressor circuit use adder as the base component to design. Multiplier architectures used manly compressor. Multipliers are functioned into three case: partial-product generation, partial-product accumulation and final addition. In the first stage, the multiplicand and the multiplier are multiplied bit by bit to get the partial products. The second stage is the most important, as it is the most complicated and determines the speed of the overall multiplier. The 4-2 and 5-2 compressors have been widely employed in the high speed multipliers to lower the latency of the partial product accumulation stage. The main source of consumed power, over all delay and area came from the partial-product accumulation stage in DSP System. Compressors usually implement this stage because they contribute to the reduction of the partial products (reducing the number of adders at the final stage) and also contribute to reduce the critical path which is important to maintain the circuit's performance. Compressors are formed basically of two types of modules: XOR-XNOR complex gates and multiplexers (MUX) and also using Adder which consist this modules.

II. CMOS TECHNIUQE

It is the technology for constructing the integrated Circuits .The MOS Field Effect Transistor (MOSFET) is the fundamental building block of MOS and CMOS digital integrated circuits. CMOS consist of NMOS and PMOS type, 3 terminal transistor. Each transistor having their own W/L ratio according to the technology used. The symbol of the Nmos & Pmos are shown below.

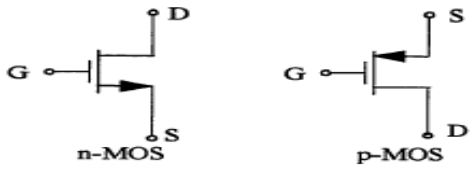

Fig.1: symbol of Nmos &Pmos

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III. ARCHITECTURES

A. *Full Adders*

An adder is a digital circuit that performs addition of numbers binary number in digital circuits. In most of computers and different kinds of processors, adders are used in the arithmetic logic units (ALU).

A full adder adds binary numbers and accounts for values carried in as well as out. A full adder adds three numbers, often represent as A, B, and Cin; A and B are the operands, and Cin is a bit carried in from the previous lower-significant stage. The full adder is usually a component in a cascade of adders, which add 8, 16, 32, etc. bit binary numbers. The circuit produces a 2bit output. Output is generated in the form of carry and sum which are represented as the signals Cout and S.

Sum = (A XOR B) XOR Cin
Cout = A AND B + Cin (A AND B)

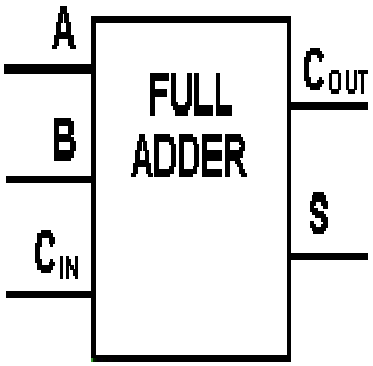

Fig.2 Block diagram of Full Adder Circuit.

B. *8t Full Adder*

The circuit of 8T Full Adder cell is shown below. The Sum output is basically arranged by a cascaded exclusive OR of the three inputs. Cout is designed using multiplexer. The circuit of eight transistor full adder cell shown in Fig 3. The Sum output is basically taken from a cascaded exclusive OR of the three inputs. Cout module is designed using multiplexer. It is just designed using the CMOS technology, the sum output and at most two stage delays are required to obtain the carry output .Where VTp is the threshold voltage of the PMOS transistor and VTn is the threshold voltage of the NMOS transistor. The 8T full adder Figure 3, is seems like serious problems especially when Cin=0. The outputs have good logic level for only a four input vectors. For the remaining input vectors, there is a major abasement in output voltage that may guide to functional failure as well as enhance power consumption. As the voltage is scaled down, the signal integrity deteriorates and the speed decreases staggeringly.

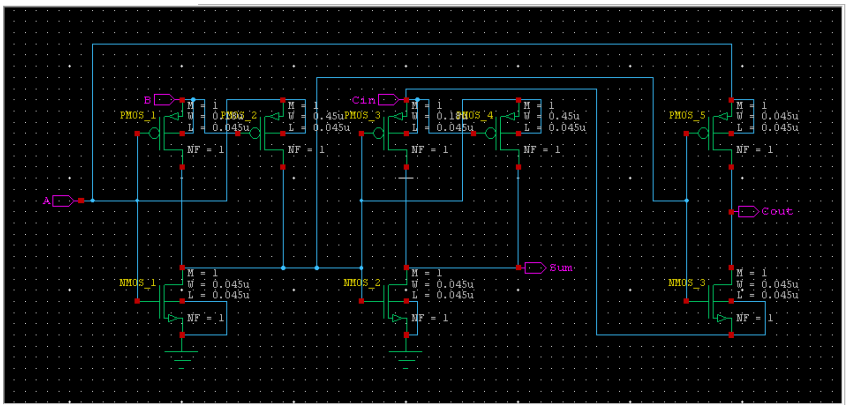

Fig.3: 8T Full Adder CMOS Design.

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C. 9T FULL ADDER

9T full adder design is shown in fig.4. The proposed design is more authentic in terms of power consumption, Power Delay Product (PDP) and temperature regularity as compared to the previous full adder designs. In this paper, the comparison of performance in basis of power is done. It is designed by using CMOS technology, by modifying the previous 8T Adder. Then the existing 9T full adder design is discussed which has additional transistor to improve the performance of the 8T full adder design. The problems in the 8T full adder circuit for certain input vectors were overcome in the existing 9T full adder. But the power consumption is reduced, the existing 8T full adder circuit. Hence the proposed 9T full adder design is presented where the sum output is implemented by a cascaded 3T XOR and 2T MUX and the carry output is implemented by XOR and MUX.

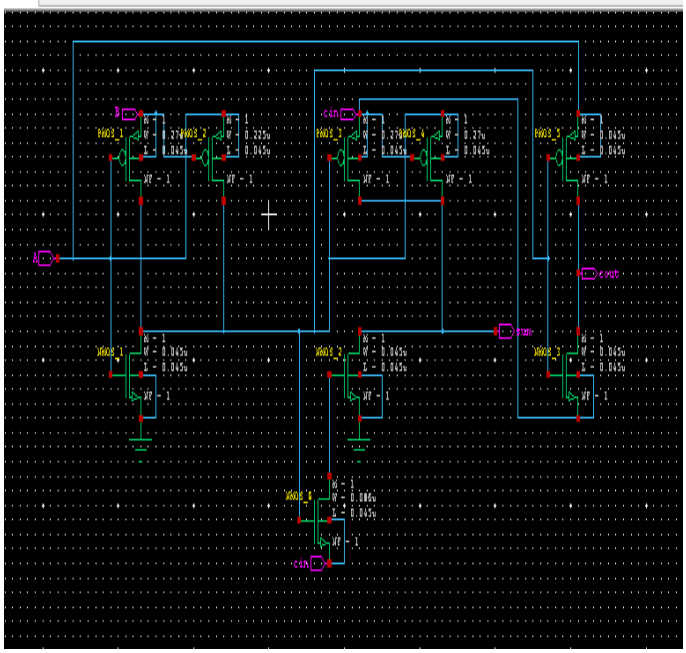

Fig.4: 9T Full Adder CMOS design

D. Compressor

Compressor is the most used component in the DSP system, with the help of inxact compressor we simplify the complexity of the circuits.In the modwrn VLSI design the muliplecation and Addition is performed by the help of varoius multipliers , the main function of the multipliers is thepartial product multiplication, partial product reduction and partial product Additions. In this paper we represent the 4:2 Compressor circuit .

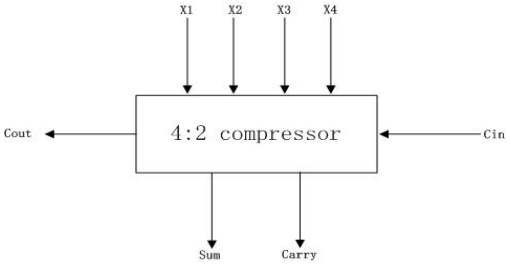

Fig.5: Block diagram of 4:2 compressor circuit.

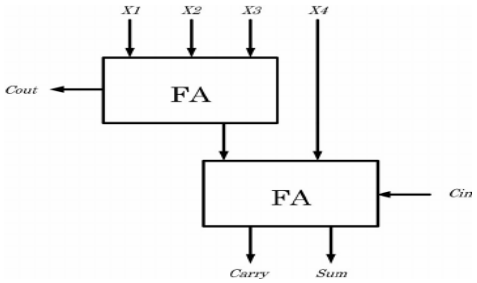

Fig.6: 4:2 Compressor using Two Full Adder.

$$Sum = x1 \oplus x2 \oplus x3 \oplus x4 \oplus Cin$$

$$Cout = x1 \oplus x2\ x3 + x1x2$$

$$Carry = (x1 \oplus x2 \oplus x3 \oplus x4)\ Cin + (x1 \oplus x2 \oplus x3)\ x4$$

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Inputs				Cin 0		Cin 1		Cout
A	B	C	D	Carry	Sum	Carry	Sum	
0	0	0	0	0	0	0	1	0
0	0	0	1					
0	0	1	0	0	1	1	0	0
0	1	0	0					
1	0	0	0					
0	0	1	1					
0	1	1	0	0	0	0	1	1
1	1	0	0					
0	1	0	1					
0	1	1	1					
1	1	1	0	0	1	1	0	1
1	1	0	1					
1	1	1	0					
1	1	1	1	1	0	1	1	1

Fig7.: Truth Table of 4:2 Compressor circuit.

IV. PROPOSED DESIGN & METHEDOLOGY

The paper present the lower order Compressor which is designed by using the different kind of Adder circuit. Using the CMOS technique the Adders are designed in 1v in different technology for better performance of the proposed circuit. Here the 4:2 Compressor is design using two Full Adder, connected in series. Compressor gives the 5 input and 3 output as the result at the end.

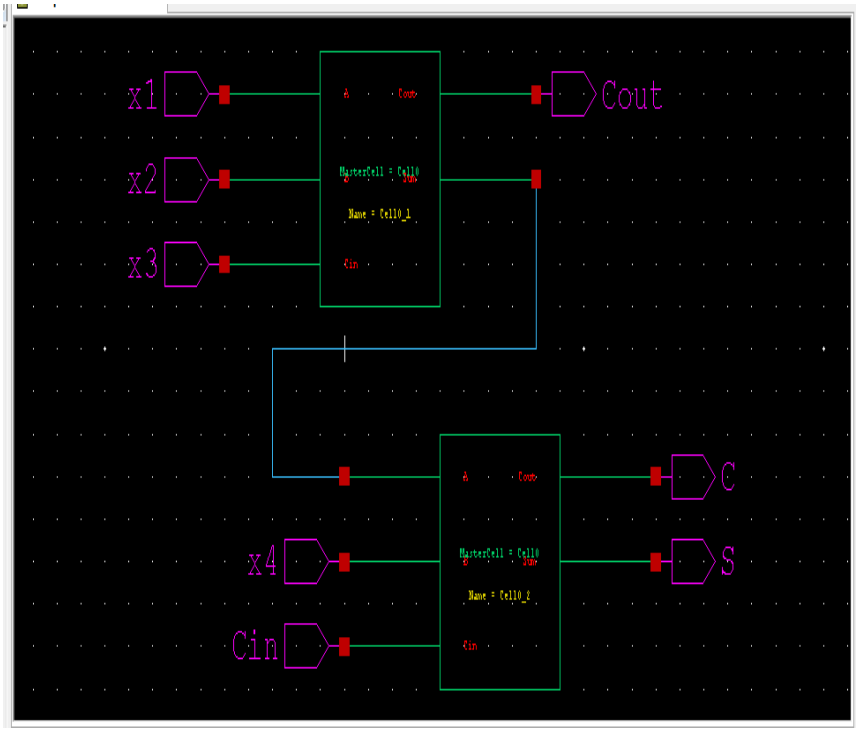

Fig.6: Block diagram of 4:2 Compressor circuit.

In the above Fig. we can see that the 5 input which are represented as x1,x2,x3,x4 and Cin respectively in design ,and the 3 output Cout ,S,C respectively. The design is generated using S-edit in Tanner EDA tool, provide the voltage value 1v. Using the T-edit we simulate the design and get the result at W-edit as wave form of the circuit, which show the result according to the value provided in the input.

V. RESULTS & DISCUSSION

In this paper various types of adders are used to design compressor using low power adder are shown above.

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Here the wave form of the 4:2 Compressor is shown below.

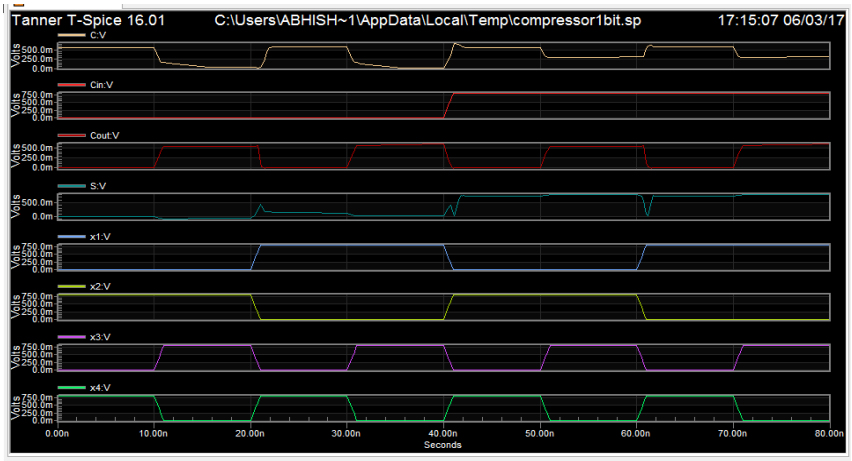

Fig.8: Wave form of the 4:2 Compressor ciruit.

As the result we calculate Consumed Power and Delay of the circuit, using different technology and the various Adder.

Compression Table of Adders designed

TYPE OG LOGIC	NO. OF TRANSISTORS	POWER CONSUMPTION(uW)	DELAY(ns)
9T	9	49.09	25.7
8T	8	42.97	16.7

The above table show the comparison between the two parameters Power and Delay the proposed design is consume less power than other designs.

Comparison table proposed compressor design

Design Compressor	No. of Transistors	Power (uW)	Delay (ns)
Using 9T	9	88.88	19.88
Using 8T	8	66.98	19.68

The above table shows the comparison between the compressor design using Adders. In the form of power and delay the 8T Adder is better than 9T Adder circuit, which give the less power consumption. The area reduced by using less number of transistor.

VI. CONCLUSION

This paper represent the performance of CMOS compressor using Full Adder. As the field of less area use less number of transistors. Using Tanner EDA Tool for calculation of the power consumption and overall delay. By using the different Adder, the technology and the less number of transistors we get the better result, by designing the various low power Full Adder for construction of 4:2 compressor has the les number of transistor which reduces the power consumption in design by using less voltage source .The power consumption will less and also reduce the overall Delay in the circuit. Adders are mostly used in arithmetic circuit because of their reliability and durable for the DSP systems. By reducing the number of transistor in circuit reduce the overall delay and also consume less power.

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REFERENCES

[1] Ajit Pal, "Low Power VLSI Circuits and systems" Springer India 2015.
[2] Sreehari Veeramachaneni, Kirthi Krishna M, Lingamneni Avinash, Sreekanth Reddy Puppala , M.B. Srinivas Centre for VLSI and Embedded System Technologies. International Institute of Information Technology Gachibowli, hyderabad-500032, India. "Novel Architectures for High-Speed and Low-Power 3-2, 4-2 and 5-2 Compressors" 20th International Conference on VLSI Design 0-7695-2762-0/07 $20.00 © 2007.
[3] Mayur Agarwal, Neha Agrawal, Md. Anis Alam "A New Design of Low Power High Speed Hybrid CMOS Full Adder" 2014 International Conference on Signal Processing and Integrated Networks (SPIN).Jorge Tonfat, Ricardo Reis, "Low Power 3-2 and 4-2 Adder Compressors Implemented Using ASTRAN" XXVII SIM - South Symposium on Microelectronics 2014.
[4] R. Menon and D. Radhakrishnan, "High performance 5: 2 compressor architectures" IEE Proc.-Circuits Devices Syst., Vol. 153, No. 5, October 2006.
[5] D. Radhakrishnan Department of Electrical and Computer Engineering State University of New York, A.P. Preethy, School of Computer Engineering, Nanyang Technological University, "Low Power CMOS Pass Logic 4-2 Compressor for High-Speed Multiplication" Proc. 43rd IEEE Midwest Symp. On Circuits and Systems, Lansing MI, Aug 8-11, 2000 0-7803-6475-9/00/$10.00 ©IEEE 2000.
[6] Jiangmin Gu and Chip-Hong Chang School of Electrical and Electronic Engineering, Nanyang Technological University, "low voltage, low power (52) compressor cell for fast arithmetic circuits" ICASSP 2003, Proc. IEEE In: CO$ on Application-Specific Systems, Architectures, and Processors, 2000. pp. 235 - 243, 2000.
[7] Karuna Prasad Keshab K. Parhi Morphics Technology Inc. Campbell, California, USA Department of Electrical and Computer Engineering University of Minnesota, Minneapolis, USA, "Low-Power 4-2 and 5-2 Compressors".
[8] Richa Singh, Anjali Sharma, Rohit Singh," Power Efficient Design of Multiplexer based Compressor using Adiabatic Logic", International Journal of Computer Applications, November 2013, pp. 45-5
[9] Momeni, J. Han, Member, P.Montuschi, Senior Member and F. Lombardi," Design and Analysis of Approximate Compressors for Multiplication", Transactions on Computers, pp.1-13
[10] Jorge Tonfat, Ricardo Reis, "Low Power 3-2 and 4-2 Adder Compressors Implemented Using ASTRAN", South Symposium on Microelectronics, pp.1-6.

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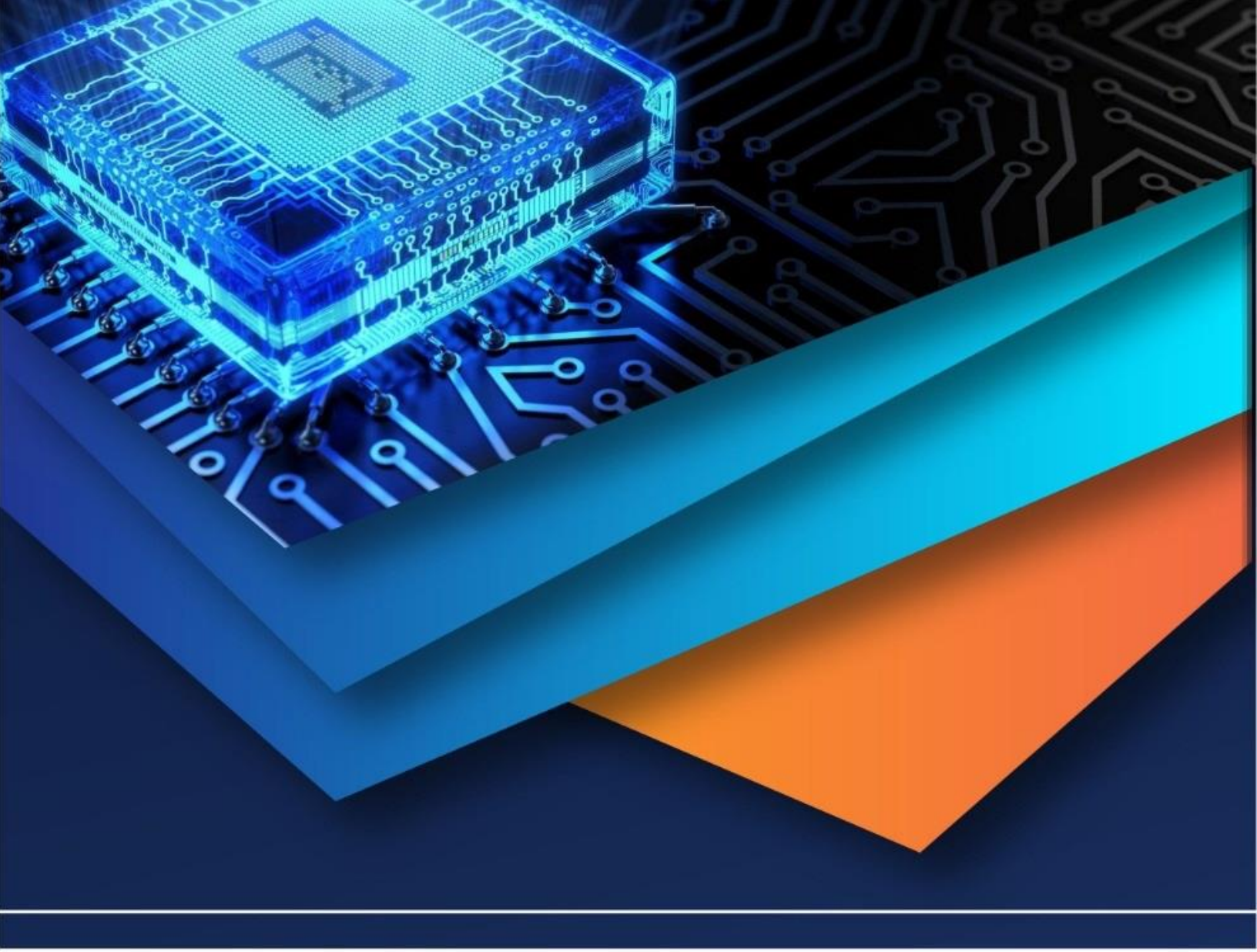

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