iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 5 **Issue:** VII **Month of publication:** July 2017

DOI:

www.ijraset.com

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor:6.887
Volume 5 Issue VIII, July 2017- Available at www.ijraset.com

Implementation of Full Adder using Cmos Logic

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Abstract: ***this paper gives an insight into the use of Complementary Metal Oxide Semiconductor (CMOS) logic which can be made use of to implement various circuits, both combinational and sequential. In this paper, full adder, having three inputs is simulated with the help of P Spice software, and the output waveforms are recorded. CMOS ICs have gained recognition all over the world ,due to its power handling capacity, small size and increased speed.***
Keywords: ***CMOS, Full Adder, MOSFET, Net-list, P Spice***

I. INTRODUCTION

Very Large Scale Integration (VLSI) Technology has significantly reduced the size of the circuits and now, billions of transistors can be fabricated onto a single chip or an IC. This has in turn, been very advantageous to the industry in terms of increased speed and greater reliability. Logic circuits, both combinational and sequential can be simulated with the help of Personal Simulation Program with Integrated Circuit Emphasis, more commonly abbreviated as P Spice. The waveforms are obtained with the help of probes as per the three inputs given to the circuit in the form of AC voltages.

CMOS logic basically encompass of p-MOS and n-MOS logic, which are complementary to each other. A basic CMOS inverter, which consists of two MOSFETs, is shown in Fig 1. N-MOS is build with n-type source and drain and p-type substrate and p-MOS is build with p-type source and drain and n-type substrate. The majority charge carriers in n-MOS in electrons and that in p-MOS is holes. Due to this, the n-type MOSFETs are usually faster than p-type MOSFETs, since electrons are twice as fast as holes. This also makes n-MOS IC's smaller in size and less immune to noise than p-MOS IC's. While simulating any circuit design, MbreakP and MbreakN models are used for n-MOS and p-MOS respectively.

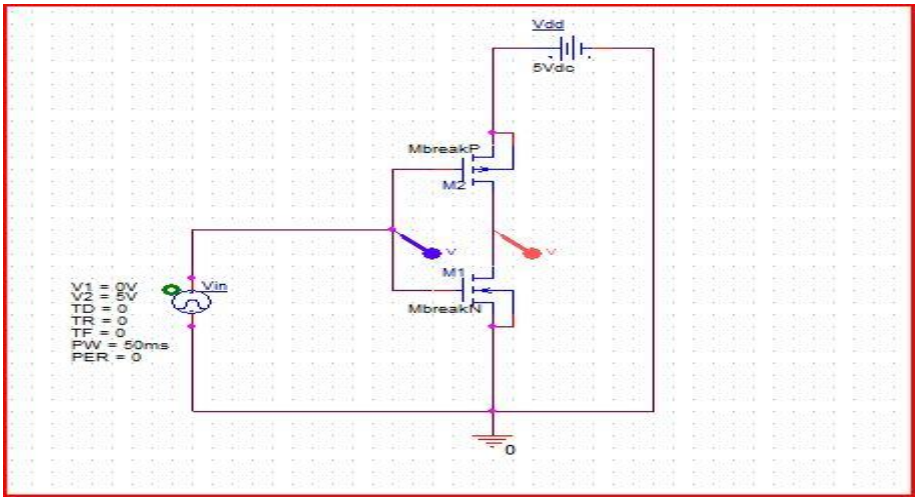

Fig. 1 Circuit diagram of CMOS Inverter

Drain to Source current equation in n-MOS is given by:

$$I_{DS} = \beta V_{DS} (V_{GS}-V_T-V_{DS}/2)$$

II. WORKING AND FUNCTIONALITY

The p-MOS circuit is also known as 'pull-up' network and the n-MOS circuit is called 'pull-down' network. When the input is high, i.e. when V_{in}= 1, p-MOS acts as an open circuit and when V_{in}= 0, n-MOS acts as an open circuit. This is the reason why p-MOS is efficient to transfer strong logic-1 and n-MOS is efficient to transfer strong logic-0. Also, since no static current flows and there is no such static power dissipation, CMOS can be efficiently used for higher density packages.

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III. P SPICE SOFTWARE

Cadence P Spice simulation technology offers its users a single, unified design environment for both, simulation and PCB Design. It offers a vast variety of models that are available for simulation purpose. It is quiet efficient software as it is easy to debug and identify the errors in the model. The components can be dragged and dropped to the design or can be added via the Net-list or the library. This property of rectifying the errors is useful to the designers as it saves a lot of their precious time as well as is cost effective.

A. Pseudo n-MOS Logic

In high density circuits, complex CMOS gates may face a problem due to the large area requirements. To reduce the number of transistors, a single p-MOS transistor with its gate terminal connected to the ground, is used as the load device. The gate terminal of the p-MOS is grounded in order to keep it permanently in ON state. Hence, with a simple pull up arrangement, the complex circuit can be implemented with much fewer transistors. Therefore, in comparison with the CMOS Logic, which consisted of 2N transistors, only N+ 1 transistor are required in Pseudo n-MOS Logic.

Although it reduces the number of transistors, the primary disadvantage of using pseudo n-MOS is the non zero static power dissipation, due to the always ON p-MOS load device conducts a steady state current when the output voltage is less than $V_{DD.}$

B. Full Adder

Full adder is a combination circuit that adds three 1-bit binary numbers, and outputs two 1-bit binary numbers, representing sum and carry respectively. All the desired components are selected from the library and three AC inputs (0-5V) are provided in terms of AC voltages, all components are wired and the simulation results are compared to the truth table of Full Adder to verify.

INPUTS			OUTPUTS	
A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	1

Fig. 2 Truth Table of Full Adder

The Boolean equation for full adder is given as:

Sum = $\bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$

= $A(\bar{B}C + B\bar{C}) + C(\bar{A}B + AB)$

= A (B xor C) + C (A xnor B)

= A xor B xor C

Carry = AB + BC + CA

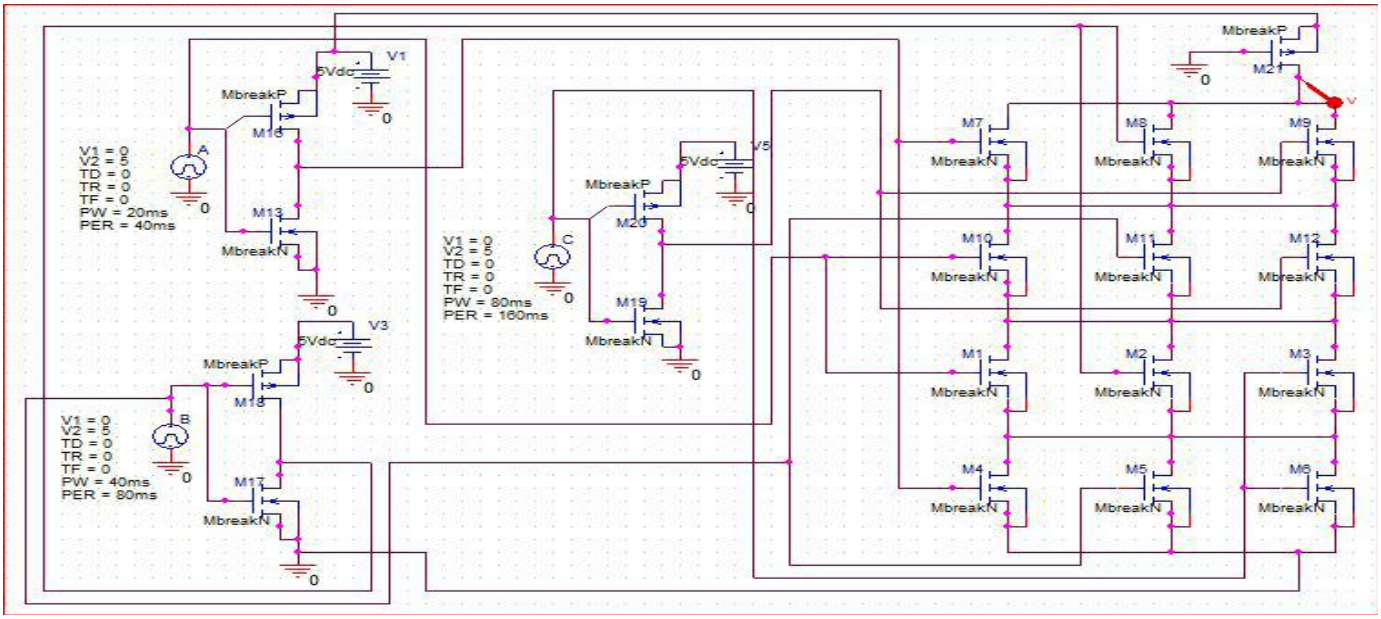
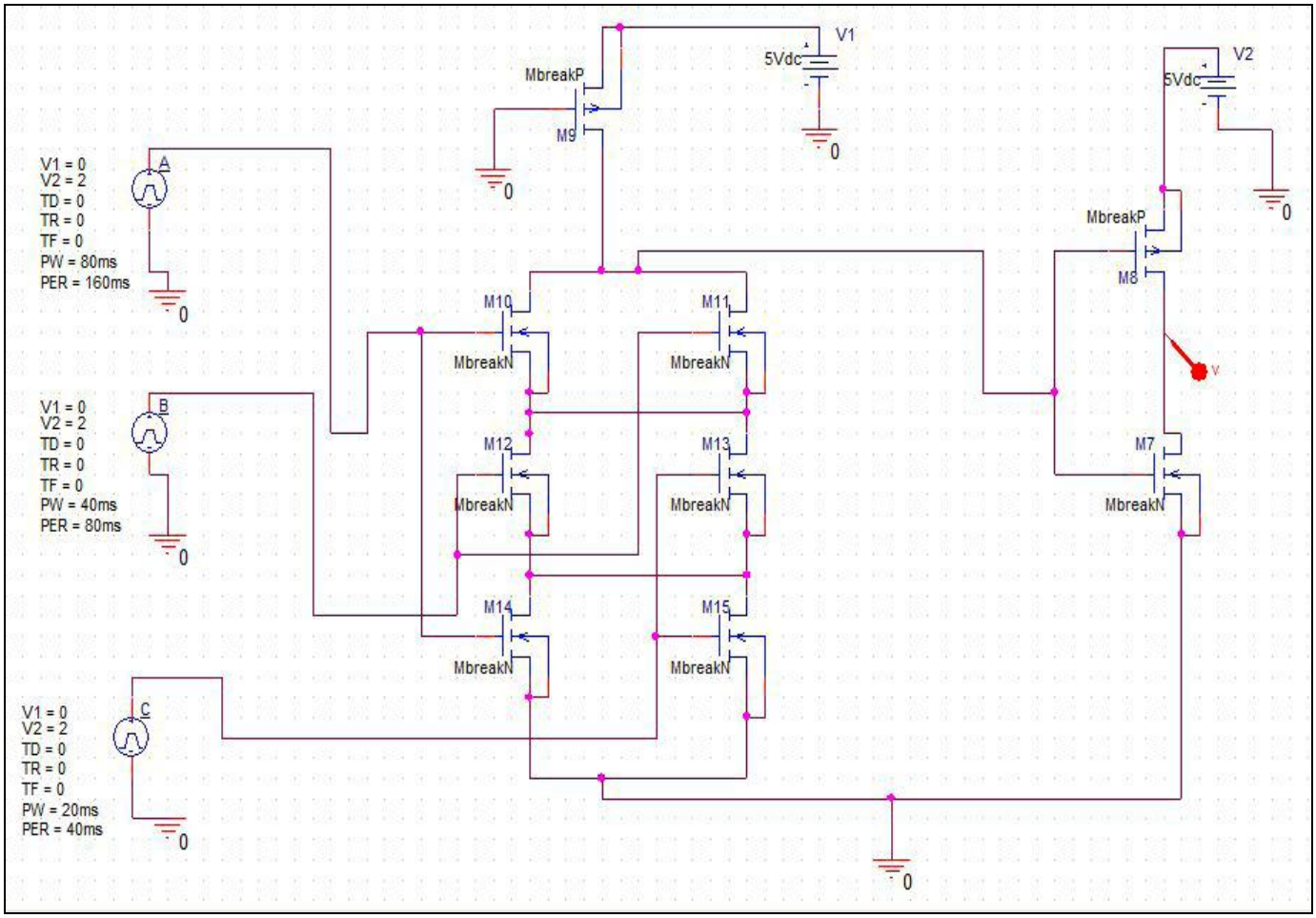


Fig. 3 Design of Full Adder on P Spice (SUM)



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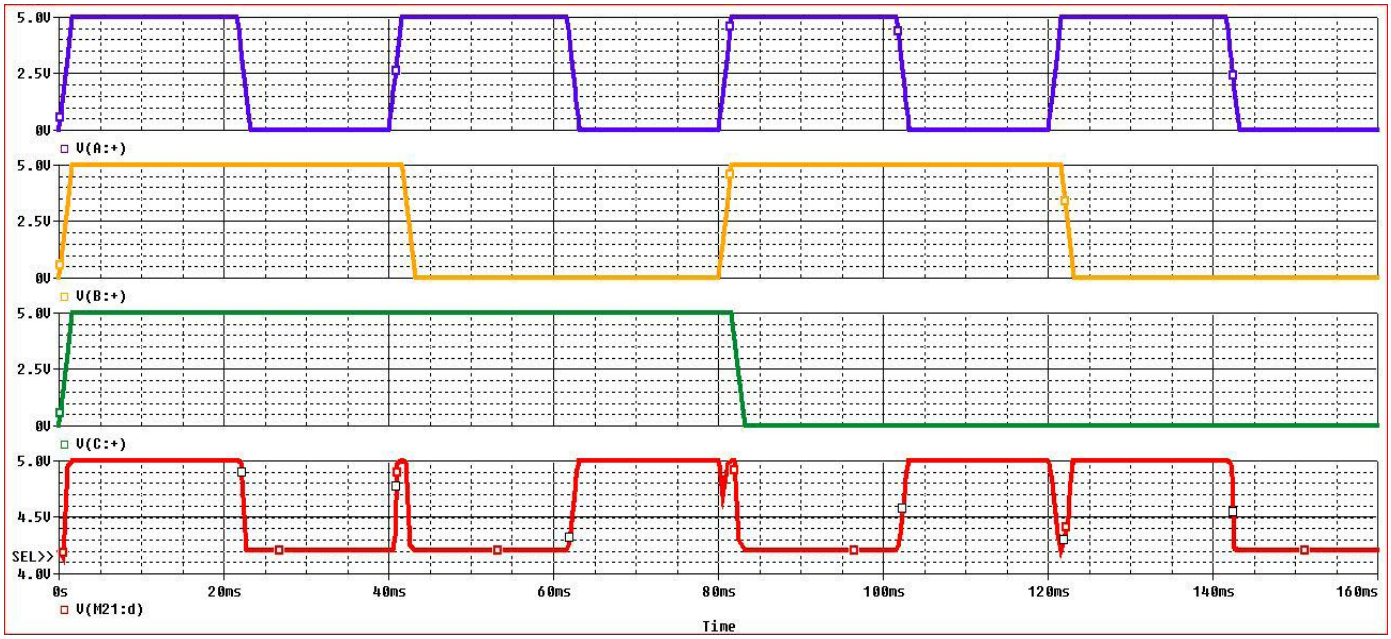

Fig. 4 Output waveform (SUM)

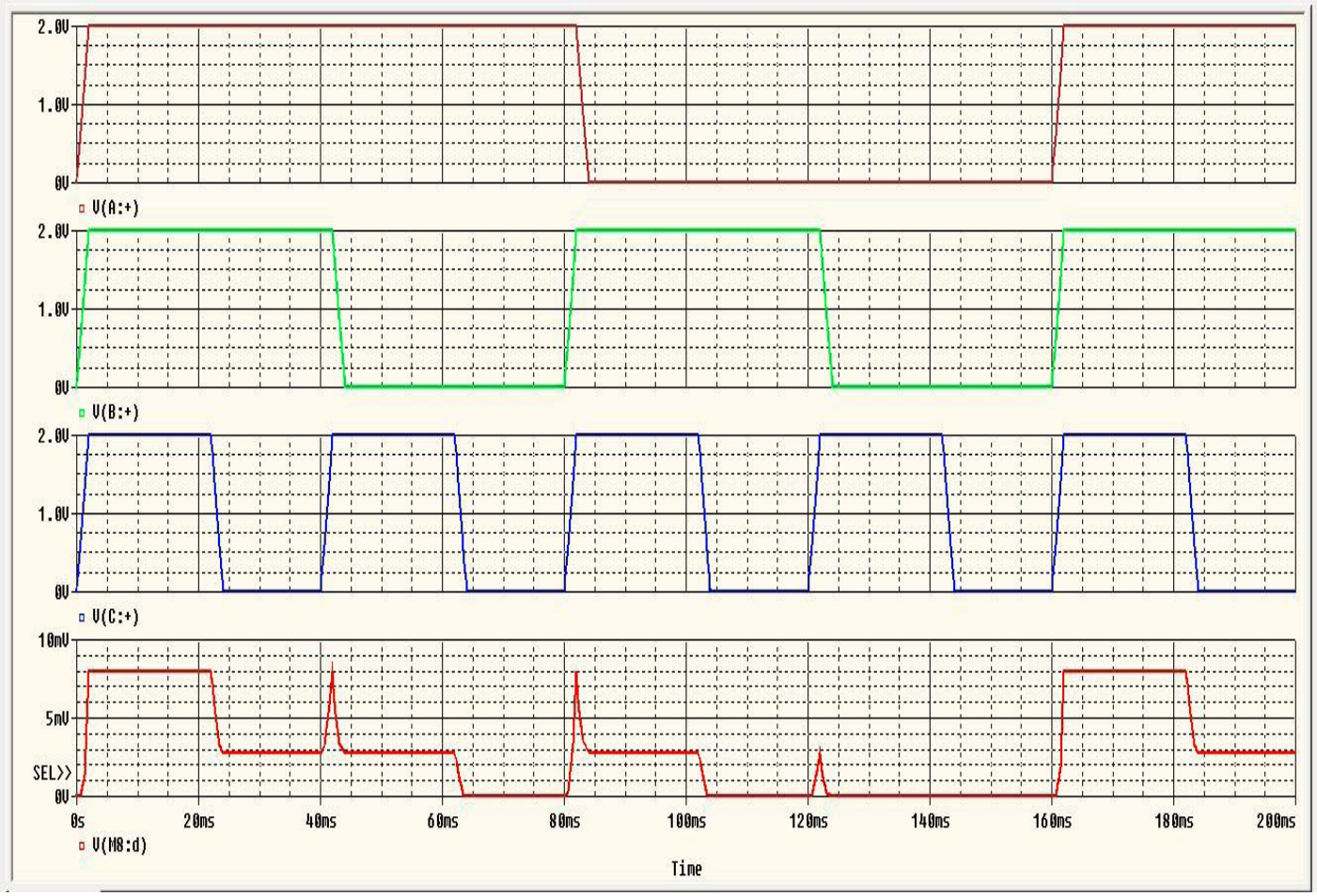

Fig. 4 Output waveform (CARRY)

```
* source FULLADDER1
M_M12          N30668 N31362 N30672 N30672 MbreakN
V_A           N31042 0
+PULSE 0 5 0 0 0 20ms 40ms
M_M8           N30718 N31218 N30668 N30668 MbreakN
V_C           N31402 0
+PULSE 0 5 0 0 0 80ms 160ms
M_M5           N30680 N31316 0 0 MbreakN
M_M2           N30672 N31218 N30680 N30680 MbreakN
V_V5           N31358 0 5Vdc
V_B           N31316 0
+PULSE 0 5 0 0 0 40ms 80ms
V_V1           N31030 0 5Vdc
M_M18          N31218 N31316 N31184 N31184 MbreakP
M_M9           N30718 N31362 N30668 N30668 MbreakN
M_M7           N30718 N31034 N30668 N30668 MbreakN
M_M3           N30672 N31402 N30680 N30680 MbreakN
M_M16          N31034 N31042 N31030 N31030 MbreakP
M_M21          N30718 0 N31030 N31030 MbreakP
M_M17          N31218 N31316 0 0 MbreakN
M_M11          N30668 N31316 N30672 N30672 MbreakN
V_V3           N31184 0 5Vdc
M_M4           N30680 N31034 0 0 MbreakN
M_M10          N30668 N31042 N30672 N30672 MbreakN
M_M13          N31034 N31042 0 0 MbreakN
M_M19          N31362 N31402 0 0 MbreakN
M_M6           N30680 N31402 0 0 MbreakN
M_M1           N30672 N31042 N30680 N30680 MbreakN
M_M20          N31362 N31402 N31358 N31358 MbreakP
```

(a)

```
* source CARRY
M_M7          N00417 N00509 0 0 MbreakN
M_M8          N00417 N00509 N00567 N00567 MbreakP
M_M9          N00509 0 N00396 N00396 MbreakP
V_V1          N00396 0 5Vdc
V_A          N00930 0
+PULSE 0 2 0 0 0 80ms 160ms
V_B          N00968 0
+PULSE 0 2 0 0 0 40ms 80ms
V_C          N05164 0
+PULSE 0 2 0 0 0 20ms 40ms
V_V2          N00567 0 5Vdc
M_M10          N00509 N00930 N04958 N04958 MbreakN
M_M11          N00509 N00968 N04958 N04958 MbreakN
M_M12          N04958 N00968 N04927 N04927 MbreakN
M_M13          N04958 N05164 N04927 N04927 MbreakN
M_M14          N04927 N00930 0 0 MbreakN
M_M15          N04927 N05164 0 0 MbreakN
```

(b)

Fig. 5 Net-list (a) Sum (b) Carry

IV. CONCLUSIONS

Full adder circuit was implemented with the help of P Spice, by using the pseudo n-MOS logic design. Output waveforms, were recorded and the Netlist was obtained which depicts the connection between any two nodes in the circuit. Further it was observed that the circuit worked more efficiently as less number of transistors needed was less as compared to the CMOS logic design. In order to further improve the performance of the circuit, domino and dynamic logic can be used.

V. ACKNOWLEDGMENT

The author wishes to acknowledge the faculty at the institution and her friends and family, without whose support and guidance, it was not possible to complete this paper.

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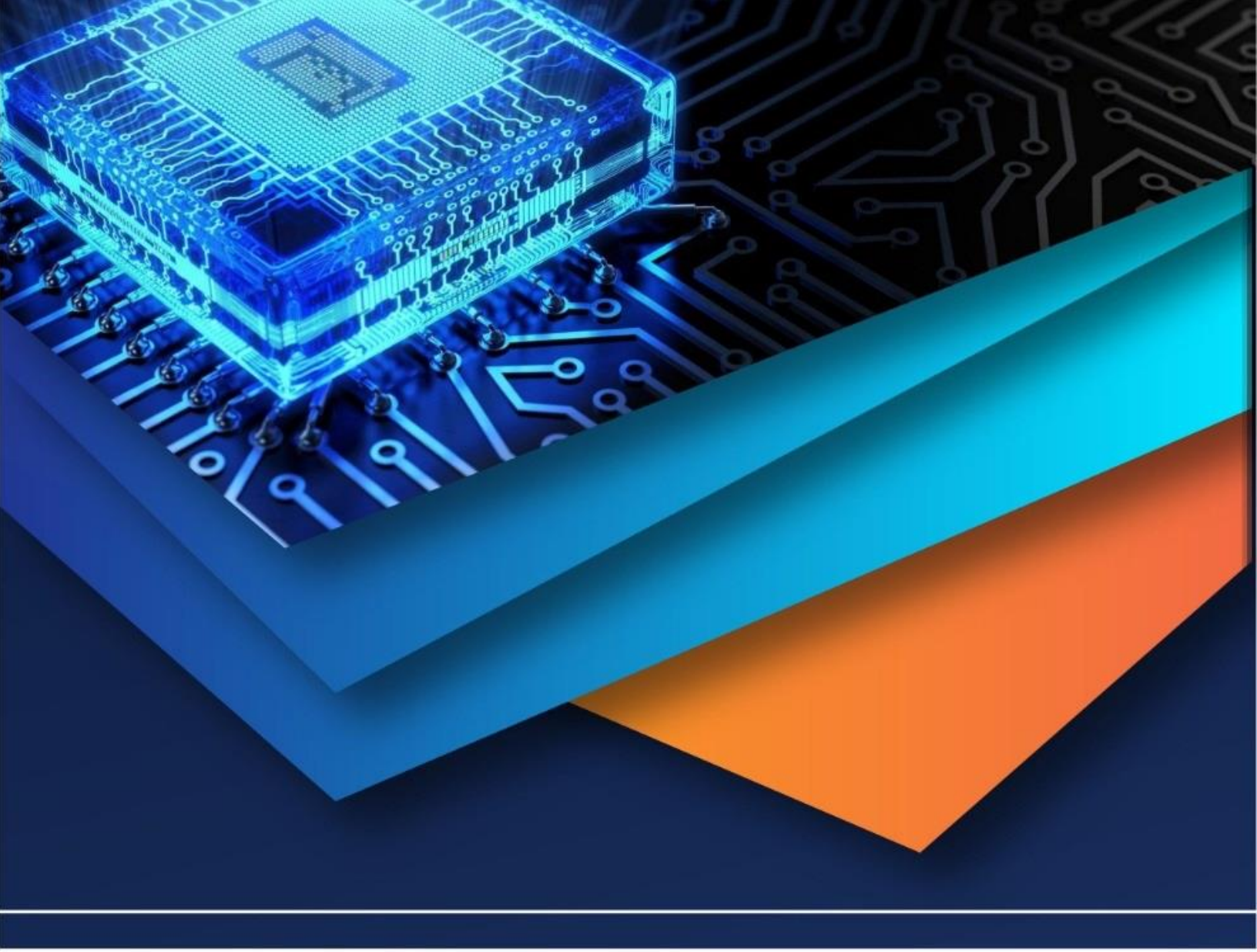

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