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# Implementation of Modified Decimal Matrix Code for Multiple Cell Upset

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***Abstract :*** ***The reliability of memory cells is becoming an essential issue today. Transient single bit errors and multiple bit upsets (MBUs) are responsible to limit the reliability of memory which causes due to radiation environment. To maintain good reliability of memory cell some codes are used to correct these single and multiple bit errors. But the main issue with these codes is that they require large area and delay overhead. The codes like hamming code are used to remove single bit upsets (SBUs) are simpler than multiple bit upsets (MBUs), but can correct single error and detect double or triple adjacent error. So to improve the memory reliability with lesser area and delay overhead, a new method Decimal Matrix Code (DMC) has been presented based on divide symbol and arrange in matrix logically which can detect and correct multiple errors. In this paper, 32-bits MDMC is proposed to enhance the memory reliability based on divide symbol which can detect and correct up to 16 errors. To reduce the area overhead of extra circuit's encoder-reuse technique (ERT) is used in which same circuit used for encoding and decoding process. Verilog HDL used for low power design and simulation and implementation can be done using Xilinx Vivado.***
***Keywords: Single Bit Upsets (SBUs), Multiple Bit Upsets (MBUs), Error Correction Code (ECC), Modified Decimal Matrix Code (MDMC), Encoder-Reuse Technique (ERT)***

## I. INTRODUCTION

As the scaling technology increases, the reliability of memory cell becomes limited due to radiation environment and territorial environment. Error produce in memory cell because of radiation environment called soft error which may cause of falling rate of reliability of memories [1]. These soft errors may be single cell upset or multiple cell upset. These errors can be removed using error correction code like Hamming codes, Reed Solomon, CRC technique, matrix code and decimal matrix code etc.

Hamming codes are simpler coding technique which can only detect and correct single error so double error can be mistaken and mis-corrected for a single error [2]. To remove this problem hamming codes are extended which can correct single error but detect up to double and triple adjacent error through selective shortening and bit replacement. Reed Solomon code is used to correct the multiple errors, specially the burst type errors in storage devices like DVD, hard disk drives, barcode tags, mobile communications and wireless units, digital TV, modem technologies, digital video broadcasting (DVB), and satellite links [3]. But the drawback of this code is that they can correct two or burst error and require large area and delay overhead. To improve the memory reliability new technique Matrix code has been proposed which is based on parity detection method. The correct- capability of matrix code is determined based on the width of error in MCU.

In this paper, Decimal Matrix Code is modified to increase the memory reliability with lesser delay and area. The proposed Modified DMC utilize the decimal integer subtraction to detect the errors. Proposed MDMC increase the error detection and correction capability which leads to enhance the memory reliability. Using the encoder reuse technique (ERT) the area of extra circuits can be diminished because encoder circuit also used as decoder circuit without interrupting the complete encoding and decoding process.

The paper is organized as follows; in section 2 the literature survey of different technique is presented. The Proposed Modified DMC and its Encoder, Decoder architecture is presented in section 3. Implementation and results of proposed technique is shown in section 4. Finally in Section 5 the conclusion of paper and ideas for future work is presented.

## II. LITERATURE SURVEY

Soft errors occur in memories due to cosmic rays etc are protected with Error Correction Codes (ECCs). Simple error correction codes used to minimize the impact of the ECC on memory complexity. For example, Single Error Correction (SEC) codes, like Hamming codes are much simpler than codes used to protect multiple corrupted bits. Hamming codes are mostly used for single error correction with reduce power consumption. These codes can identify double error but correct only single error. To prevent the

occurrence of multiple bit errors Reed Solomon, Bose–Chaudhuri –Hocquenghem (BCH), Built in current sensor (BICS) and Interleaving techniques are used. But these codes have more power consumption, delay and area overhead. To overcome these problems Decimal Matrix Code (DMC) is presented with better memory reliability and reduced power consumption and area.

Hamming codes are also called Forward Error Correction code can correct single error and identify up to double bit errors. The minimum distance of the hamming code should be equal to 3. The hamming codes have the following parameters:

$$n=2^m-1 \quad (1)$$

$$k=n-m \quad (2)$$

$$d_{min} = 3 \quad (3)$$

Where n represents the code size, k is the number of data bits, m is the number of check bits and $d_{min}$ is the minimum distance of the code [2]. The position of check bits gives different error present in stored data. The parity bits are calculated using parity generator and decoder used to calculate a syndrome value. Zero value of syndrome bit indicates no error. If the value of syndrome bit is non-zero, it means error is present. The main drawback of Hamming codes is that a double error generates a syndrome assigned to a single error correction which leads to a mis-correction and can be cause of wrong decoding. To overcome this drawback SEC-DED extended Hamming codes were proposed. To increase memory reliability more than one error such that double and triple adjacent error can be detect using enhanced hamming code by reordering the code bits.

Extended Hamming codes can be implemented by adding the Triple-Adjacent Error detection capability which includes an additional check bit. Selective shortening is performed on original hamming matrix and the main objective to identify triple adjacent error is to get an even weight syndrome.

Shortened Hamming codes can detect some multiple errors, but does not provide a given kind of errors systematically [2]. Reed-Solomon codes are mainly used to correct the burst errors. These codes have its own error correcting capability so useful in saving time for identification and correction of error. Reed Solomon code can detect and correct multiple random symbol errors by adding t check symbols to the data [3]. An RS code can identify any combination of up to t erroneous symbols and can correct up to $\lfloor t/2 \rfloor$ symbols. The main problem of RS codes is that they require more power and area overhead. Interleaving technique has also been used to deal with multiple bit errors in memory cell. Interleaving technique rearrange cells into different physical positions to separates the different bits of different physical words from the same logical word. Interleaving technique has tight coupling of hardware structure from both cells and circuit structure so may not be used in content-addressable memory (CAM). Built-in current sensors (BICS) are proposed to provide protection against multiple corrupted bits with correction of single error and identification of double-error. However, BICS technique can correct only two errors in a word [7].

To correct the multiple corrupted bits 2-D matrix codes (MCs) are proposed which require low decoding delays. In this code, data word is divided into multiple rows and multiple columns logically. Hamming code are used to protest the bits per row, while bits per column are protected by Parity code. The 2-D Matrix codes can correct only two errors which are identified by Hamming code and can be correct when the vertical syndrome bits are activated [9]. As different error correction coding techniques used to prevent the occurrence of multiple bit error, however the main problem is that they require complex encoder and decoder circuit, power, area and delay overhead. To minimize these drawbacks compared to existing codes, Decimal matrix code is proposed which increase the memory reliability by improving the error correction capability [9].

Decimal matrix code (DMC) is based on divide symbol method and use decimal algorithm to obtain the maximum error identification capability. DMC use the encoder- reuse technique (ERT) in which DMC encoder used as a part of decoder, soreduce the area overhead. ERT technique is proposed in fault tolerant memory.

## III. METHODOLOGY

The Modified DMC method is proposed to decrease the number of check bits so that more number of information bits can be stored in memory cell. The parallel check bits “H” and vertical check bits “V” are calculated to identify and correct the corrupted bits present in memory cells. To increase the reliability of memory cells with lesser area the Modified DMC is presented with same circuit for encoder and decoder using encoder- reuse technique. The fault tolerant system is used to reduce the possibility of faults in encoder and decoder circuit.

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### *A. Fault Tolerant System of Proposed MDMC*

The fault tolerant system schematic includes DMC encoder, SRAM to store the data and redundancy bits and DMC decoder as shown in figure 3.1. Firstly, the data bits X are provided to encoder and obtained the parallel and vertical redundancy bits H and V respectively. After the end of encoding process these redundant bits are stored in memory. If any radiation particle hits the memory cells, MBUs happen in memory and these corrupted bits can be corrected in decoding process. To reduce the area overhead ERT technique is proposed.

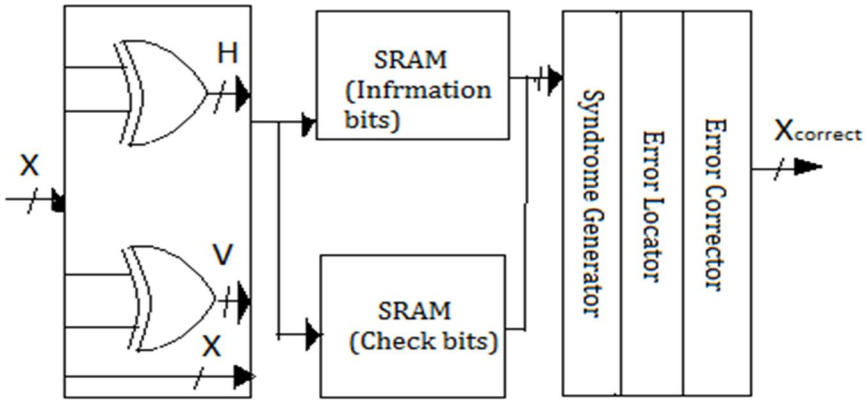


Figure3.1 Schematic of fault tolerant system of Modified DMC [4].

### *B. Proposed MDMC Encode*

Proposed MDMC is performed on the basis of divide the symbol and arrange in matrix form ideas where matrix is implemented logically so changes in physical structure of memory do not require. In this proposed method the N-bit data word is divided into m symbols of n bits where N= m × n, and these m symbols are arranged in $m_1 \times m_2$ 2-D matrix (m=m1 × m2) where values of $m_1$ represent the number of rows and values of $m_2$ represent number of columns in the logical matrix [4]. 32-bit ($X_0$-$X_{31}$) codeword divided into 8 symbols ($S_0$-$S_7$) of 4 bits and arranged in matrix form is shown in figure 3.2.

The parallel (horizontal) check bits H are obtained by implementing the decimal integer subtraction of sort out symbols per row and vertical check bits V are achieved by implementing the binary operation among the bits per column. In the presented paper, 32-bit binary codeword is taken as example. The information bits $X_0$-$X_{31}$ directly stored in memory while the $H_0$-$H_{15}$ parallel check bits and $V_0$-$V_{15}$ vertical check bits are calculated using decimal integer subtraction and then stored in memory. The parallel and vertical check bits in encoder called as Write Redundant.

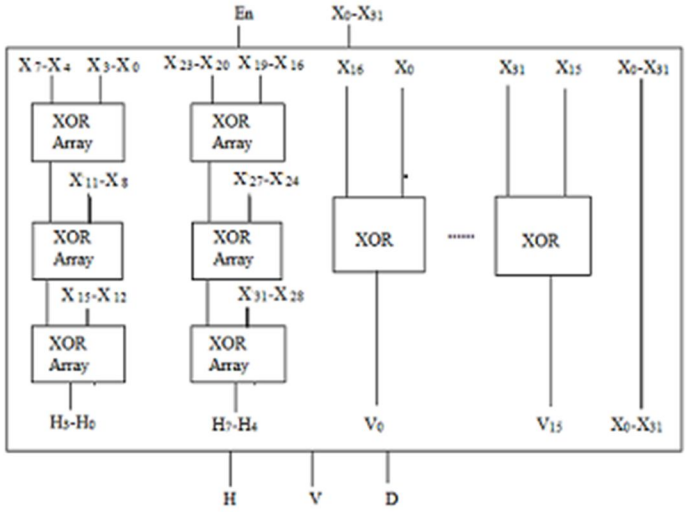


Figure3.2 32-bit encoder circuit of Modified DMC [5].

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1) *Parallel Check Bits Calculation:* 32 bit data word is divided into 8 symbols $S_0$-$S_7$ of 4 bits. The symbols $S_0$-$S_3$ are applied to XOR array to get the parallel check bits [$H_3H_2H_1H_0$]. Similarly symbol $S_4$-$S_7$ are applied to XOR array to generate their check bits [$H_7H_6H_5H_4$]. Equation1 and 2 are used to calculate the parallel check bits.

$$X_{15}X_{14}X_{13}X_{12}\text{^}\ X_{11}X_{10}X_9X_8\text{^}\ X_7X_6X_5X_4\text{^}\ X_3X_2X_1X_0 = H_3H_2H_1H_0$$
$$X_{31}X_{30}X_{29}X_{28}\text{^}\ X_{27}X_{26}X_{25}X_{24}\text{^}\ X_{23}X_{22}X_{21}X_{20}\text{^}\ X_{19}X_{18}X_{17}X_{16} = H_7H_6H_5H_4 \quad (2)$$

2) *Vertical Redundant bits Calculation:* Vertical check bits are acquired by XOR operation performed on the bits per column. For example Vertical bit $V_0$ is calculated by XOR operation of bit $X_0$ and $X_{16}$. Similarly all other vertical check bits are evaluated as follows:

$$X_0\text{^}X_{17} = V_1 \quad (3)$$
$$X_1\text{^}X_{18} = V_2 \quad (4)$$

The generalized form to calculate vertical parallel bits can be given as –

$$X_n\text{^}X_{n+16} = V_n$$

### C. *Proposed MDMC Decode*

MDMC decoder used the same circuit as encoder using encoder- reuse technique (ERT). Decoding process is done to get the original data. Table1 explain how same circuit can be used for both encoder and decoder circuits where En (enable) signals distinguish the encoder from the decoder.

Table1
Encoder circuit behavior in MDMC [4]

| Extra Circuit | En Signal | | Function |
|---|---|---|---|
| | Read | Write | |
| Encoder | 0 | 1 | Encoding |
| | 1 | 0 | Decoding |

The proposed technique detect all possible errors in codeword, therefore it increase the error detection capability from all other related techniques and enhance the memory reliability. MDMC decoder includes Syndrome calculator, Error locator and Error corrector as shown in figure3.4. Each module of proposed MDMC decoder executes their specific job. In MDCM decoder the data in each row decoded to recalculate the parallel and vertical check bits for detection and correction of corrupted bits.

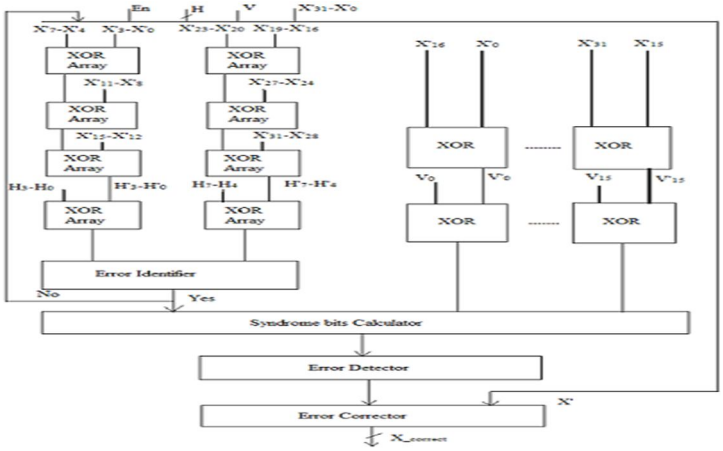


Figure3.4. 32-bits decoder circuit of Modified DMC

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Redundant bits are recalculated from received information bits to calculate the syndrome bits. Computation of these redundant bits in decoder is called as RR (Read Redundant). The difference between stored check bits and re-evaluated check bits provide the horizontal syndrome bits $H_{syn}$ and vertical syndrome bits $V_{syn}$ as shown in figure 3.5 and figure 3.6. The difference between stored check bits and re-evaluated check bits gives the syndrome bits.

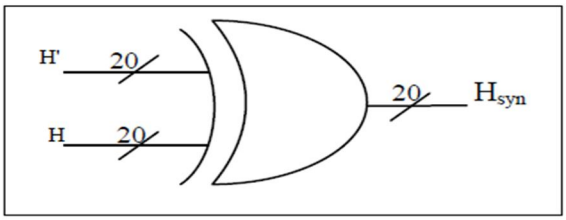


Figure3.5 Horizontal Syndrome bits using XOR operation [11].

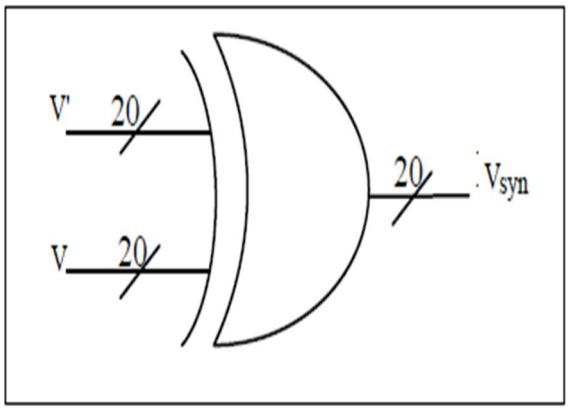


Figure3.6 Vertical Syndrome bits using XOR operation [11].

Parallel syndrome bits can be calculated as-

$$\Delta H_3H_2H_1H_0 = H_3'H_2'H_1'H_0' \wedge H_3H_2H_1H_0$$
$$\Delta H_7H_6H_5H_4 = H_7'H_6'H_5'H_4' \wedge H_7H_6H_5H_4$$

Vertical syndrome are calculated as

$$V_{syn,0} = V_0' \wedge V_0$$

Error locator locates the error using the syndrome bits which can be become error-free by flipping the values of corrupted bits. The horizontal syndrome bits and vertical syndrome bits with same length are grouped to locate the corrupted bit in any symbol. The grouping of these syndrome bits is shown as

$$H_{syn}\ (8\text{-bits}) \begin{cases} H_{syn,3-0} \\ H_{syn,7-4} \end{cases}$$

$$V_{syn}\ (16\text{-bits}) \begin{cases} V_{syn,3-0} \\ V_{syn,7-4} \\ V_{syn,11-8} \\ V_{syn,15-12} \end{cases}$$

Similarly other vertical syndrome bits can be calculated. If the value of syndrome bit is equal to zero, no error occurs in stored data otherwise error is present. Error locator locates the error using the syndrome bits which can be become error-free by flipping the values of corrupted bits.

The error corrector corrects the corrupted bits by inverting the corrupted bits. The bits are inverted using the XOR operation.

$$D_{0\_correct} = D_0 \wedge S_0$$

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In the presented MDMC technique, the area of extra circuit is minimized by reusing its encoder circuit as decoder known as ERT. The En signal used to decide whether the encoder circuit will act as decoder so mainly used to distinguish the encoder and decoder under manage of write and read signal.

## IV. IMPLEMENTATION AND RESULTS

### *A. RTL View of Modified DMC*

RTL view of proposed Modified DMC is shown in figure 4.1 which includes the two blocks. The first block provide the parallel and vertical check bits of stored data and received data word and the second block provide the syndrome bits by comparing these parallel and vertical check bits.

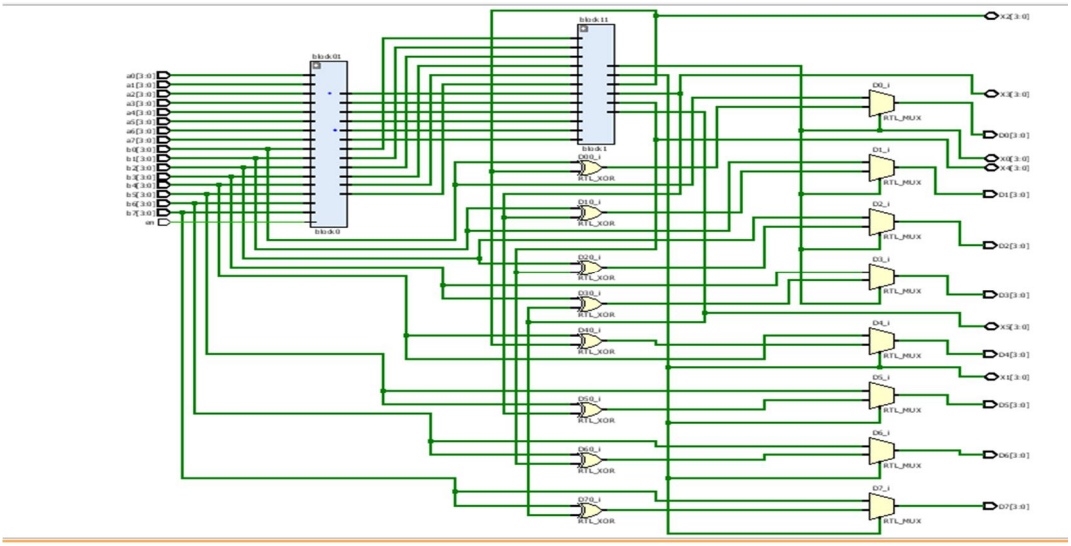

Figure4.1. RTL View of 32-bit Modified DMC

### *B. Simulation Result*

Simulation result of 32-bit Modified DMC is shown in figure 4.2. The output waveform shows the data same as the data word stored in memory during encoding process.

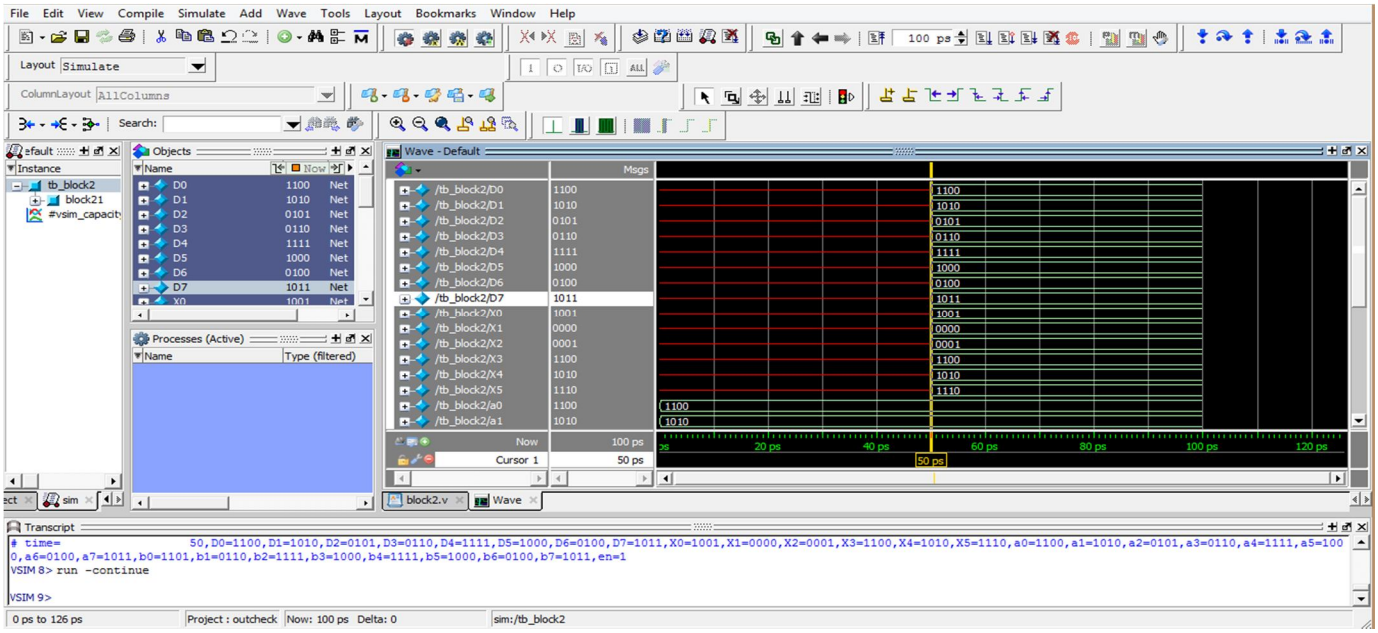


Figure4.2. Simulation Result of 32-bit Modified DMC

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*C. Synthesis Result*

The synthesis result of 32-bit Modified DMC is shown in figure 4.3.

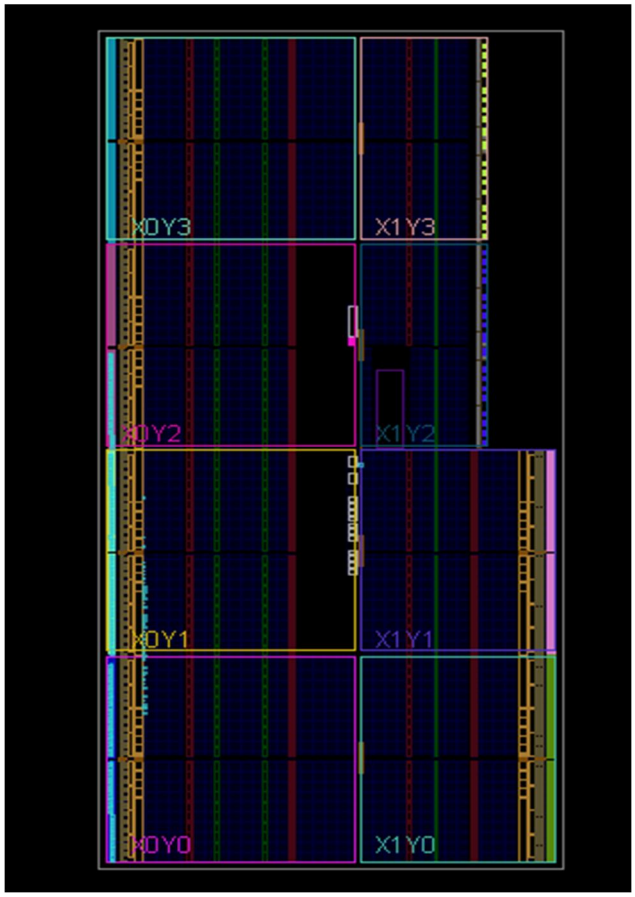


Figure4.3. Synthesis result of Modified DMC.

## V. CONCLUSION AND FUTURE WORK

The proposed paper presents the detection and correction of corrupted bits stored in memory cells using the Modified Decimal Matrix Code. Decimal integer subtraction used to calculate the horizontal check bits and XOR operation is used to calculate the vertical check bits. These check bits are calculated from the original data word stored in memory during encoding process and from received data in decoder. The proposed Modified DMC technique enhances the memory reliability with less number of redundancy bits. The number of redundant bits is 24 and corrects up to 16 multiple bits error in 32 bit data word.

In the future, more number of corrupted bits can be identify and correct to increase the memory reliability. The number of check bits also can be decrease with less area and delay so that more number of information bits can be store in memory cell.

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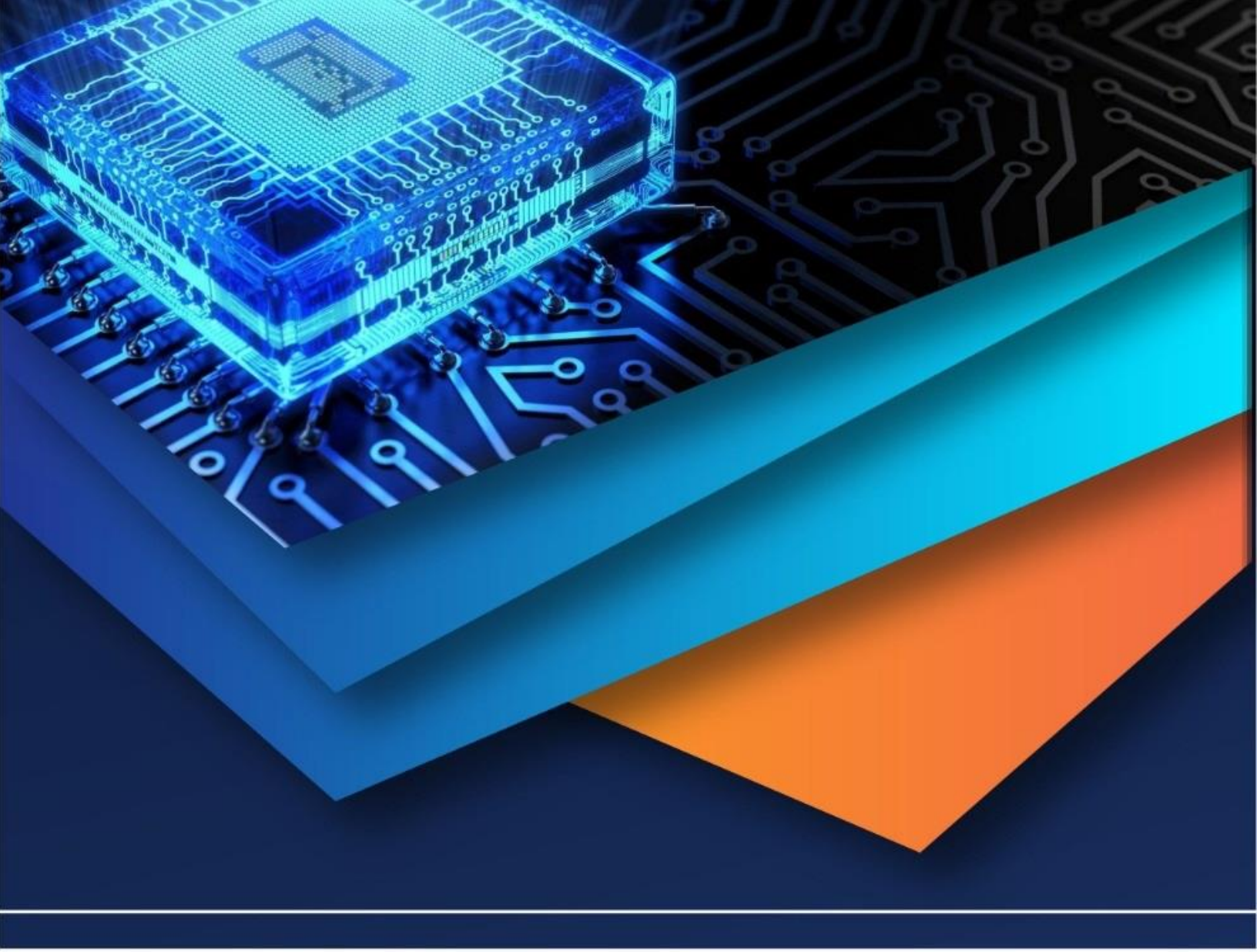

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